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SUPERTHEME

ICT Project no. 318458

**SUPERTHEME**

Circuit Stability Under Process Variability and Electro-Thermal-Mechanical Coupling

# D6.2: First report on simulation support provided to the ITRS

| | Name | Organisation | Date |
|---|---|---|---|
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## Abstract

In this deliverable the first step of simulation studies carried out in SUPERTHEME to support the extraction of ITRS device specifications is described. Whereas the work performed so far referred to nominal devices, these results and the development of the SUPERTHEME software made so far now enable to extend these studies to the impact of process variations. Details of the results have been submitted for publication elsewhere.

# 1. Introduction

Process variations belong to the most critical challenges for the further development of advanced nanoelectronic devices and circuits, as highlighted among others in various sections of the International Technology Roadmap for Semiconductors ITRS [1]. They do not only critically affect devices with smallest feature sizes *("More Moore")* but also various "*More than Moore*" devices, with relaxed features sizes, e.g. in the analog or high voltage area.

In order to meet this challenge, the sources of variability must be identified, their size must be quantified, and their impact on devices and circuits assessed and compared to the specifications of the products in terms of variations or performance: E.g. a too large variation of the threshold voltage of a device would result in malfunctioning of the circuit and the overall product, and must in consequence be avoided.

The impact of process variations on device and circuit performance cannot be studied mainly by experiments: This would require the capability to sufficiently control the process variations, in order to study the impact of one varying process parameter while all other parameters are kept at their nominal value. Besides the required unacceptably large experimental effort, this approach is mostly not possible at all, because variations like Line Edge Roughness can due to physical reasons not be fully suppressed. Moreover the variations can hardly be measured in-situ and non-destructively during the fabrication of a device, which means that it is not possible to identify for a specific device in question how large the process variations actually were which occurred during the fabrication of this specific device.

In contrast to the experimental approach, this direct link between process variations occurring during the fabrication of a device and the performance of the final device or circuit could very well be established and quantified by the use of process, device and circuit simulation: If the simulation tools used employ sufficiently accurate physical models and are well calibrated to match and reproduce the "nominal" process (which means a fabrication process without variations), one can easily introduce intentional variations of one or more process parameters, simulate the impact of the variations on the fabrication process in question, and then trace the impact of that modified process through all following process steps to the final devices and circuit. Device and circuit simulation can then be applied to extract the parameters determining the device and circuit performance, like threshold voltage, on- and off-current, operating frequency, and to quantify the variations of such device or circuit parameters caused by the process variations being studied.

However, existing simulation programs still have critical shortcomings which strongly limit their applicability for the study of process variations. Simulation mostly starts from assumed values for variations as results of the fabrication process, e.g. dopant fluctuations in the transistor channel or gate length variations, derive from these the variations of the device or circuit performance, and partly try to transfer the data obtained to design. In consequence, it cannot be assessed with this approach whether the assumptions made on the size and distribution of the process variations are realistic. Moreover, it cannot be derived which process steps introduce the most critical variations and should therefore be improved. In addition, the impact of the fabrication steps on the reliability of devices and interconnects is not investigated. In short, this approach does not help to realistically assess the available semiconductor process technology and to further improve it. Another immanent problem is that variability is currently hardly characterized at its source, which is largely at the equipment level.

The key objective of the SUPERTHEME project is to close these critical gaps, by focusing on the simulation of process variations and their impact on device and circuits, including device reliability. To this end, a hierarchical simulation approach is being employed which allows for the holistic simulation of the impact of process variations from their source (largely at equipment level) through the sequence of process steps needed for device and circuit manufactur-

ing up to the performance and reliability of the device and circuits. Furthermore, typical process variations are being characterized at their source.

The approach described above is generic in the way that it is applicable to all devices which are affected by variability from the fabrication with a top-down technology, which means by patterning and modifying bulk material (including SOI and other thin layers). Within SUPERTHEME, it will especially be developed and applied for advanced More than Moore devices and systems, as specified by the project partner ams. This is in line with the focus of the Framework 7 call [2] of the European Union from which SUPERTHEME is being funded. However, the use for aggressively scaled CMOS devices should not be hidden and will be demonstrated among others through a cooperation with the International Technology Roadmap for Semiconductors ITRS.

Whereas benchmarks for More than Moore applications are carried out by the SUPERTHEME partner ams and are only reported on a confidential basis internally within the project, benchmarks on More Moore applications are being carried out by the SUPERTHEME partners Fraunhofer, Gold Standard Simulation and University of Glasgow. In this deliverable first results obtained at Fraunhofer on the assessment of advanced CMOS devices, linked to the ITRS, are summarized.

## 2. Device specifications in the ITRS

Within the PIDS (Process Integration, Devices and Structures) chapter of the ITRS specifications are given among others for the performance of extended bulk CMOS, fully depleted SOI (Silicon-on-Insulator) and multigate SOI transistors. Key technological quantities which define the scaling of these devices include especially the physical gate length $L_g$, the equivalent oxide thickness *EOT*, junction depth (for bulk transistors) and (silicon) body thickness for SOI transistors. These values obviously and directly link to the capabilities of the available semiconductor technology. For some other quantities like the “Mobility Enhancement Factor due to Strain” or various electrical capacities and parasitic resistances the link to technology is although existing more indirect and complicated: These values cannot be adjusted directly within the technology, but itself result from various aspects of technology and device architecture. In turn, although several predictions made in the ITRS depend to some extent on the values assumes for such quantities, it is frequently necessary to question whether these assumptions are realistic: E.g. values and trends of electrical capacitances which were obtained and measured at existing devices might not be realistic in case of further scaling or changes in materials and device architectures.

Historically, in the ITRS the MASTAR [3] tool was used to forecast the performance of future scaled devices based on the assumptions. MASTAR largely uses physical motivated analytical equations and simple models to assess the performance of new devices based on data obtained from measurement (or simulation) of existing devices. This procedure is very reliable and reasonably accurate if the specifications of the devices are not too far from those of the devices from which the data base of MASTAR was built. However, this approach cannot cope with new effects which are not sufficiently included in that data base, like quantum-mechanical or ballistic effects. Using MASTAR several Figures of Merit were forecasted for future scaled devices in the ITRS and especially in the PIDS chapter, such as saturation threshold voltage, drive current (for a given leakage current), the transistor intrinsic delay *CV/I*, or ring-oscillator delay per stage. Whereas the efficiency of the MASTAR approach enables the conduction of broad forecasts for the performance of scaled devices for the next 15 years as given in the ITRS, the limitations in the data base and the relative simple models used challenge the accuracy of the results. This can be visualized with a simple approach from mathematics: Interpolation of a function is mostly rather accurate within the interval from which the supporting points were taken, but extrapolation beyond that interval is in case of non-smooth functions usually increasingly inaccurate.

In view of this problem, some members of the ITRS PIDS and/or the ITRS Modeling and Simulation (M&S) team, including the SUPERTHEME coordinator who has also chaired the M&S team since 2002, suggested to use process and device simulation to forecast the performance of future scaled devices. Whereas this allows for the more or less rigorous inclusion of physical effects and especially of those which gain importance with device scaling, the effort needed is much higher than when using MASTAR. Furthermore it should be noted that appropriate calibration using measurements of existing devices is as well an indispensable requirement as the usage of appropriate values for all parameters which are used in the simulation. Especially, parasitics must either be appropriately included in the simulation or the results clearly classified to exclude parasitics.

For the 2013 ITRS, for the first time the attempt was made to replace or at least to complement MASTAR with the application of TCAD tools. These activities are largely carried out by two PhD students at Purdue University in the USA, employing the Purdue tools PADRE and NEMO5. The SUPERTHEME partner and M&S chair Fraunhofer IISB strongly took part in the discussions on this work. Especially, two problems were addressed: First, although the tools used were calibrated on available experiments of existing devices, several assumptions had to be made on quantities like carrier mobility, capacitances and parasitics, which critically affect the results obtained. Second, some of the results obtained did considerably deviate from the expectations of industry which are based on existing experimental data and MASTAR calculations. Because the ITRS activity of Purdue University is external to SUPERTHEME these aspects cannot be discussed further in this document.

## 3. Assessment of ITRS specifications within SUPERTHEME

In task 6.3 “Support action to the ITRS“ Fraunhofer IISB and GU will apply the SUPERTHEME systems for the assessment of the variability and the ETM coupling of advanced devices below 22nm. Work carried out so far has been based on the overall situation in the ITRS where in 2013 the emphasis for modeling has been put on the prediction of the behavior of nominal devices. To this end Fraunhofer IISB calibrated Sentaurus Device [4] from Synopsys using experimental data for 20 nm CMOS transistors published by Samsung [5]. The following approach was then used for the assessment of the scaling of nominal bulk, single-gate (SG) fully-depleted (FD) SOI, and multigate (MG) FD NMOS FETs:

- Geometrical sizes and channel doping of the transistors were used as specified in the 2011 issue of the ITRS [1].
- For simplicity, a uniform doping of $3 \cdot 10^{20}$ $cm^{-3}$ was used for the source and drain regions, which were aligned to the edges of the gate with zero overlap.
- Appropriate physical models were selected, as detailed elsewhere [6]

Different scaling scenarios were considered and simulated for all three device architectures in question and compared with the 2011 ITRS specifications for the device performance, namely:

- For bulk NMOS: a) Standard ITRS scaling; b) channel doping fixed to $5 \cdot 10^{18}$ $cm^{-3}$ instead of increasing from $4.5 \cdot 10^{18}$ $cm^{-3}$ in 2011 to $9 \cdot 10^{18}$ $cm^{-3}$ in 2017; c) in addition to the fixed channel doping a scaling of *EOT* more aggressive than foreseen in the ITRS was assumed. This latter scaling plan led to a good agreement with the ITRS specifications for the drain current. Furthermore, with this scaling plan especially for smaller channel lengths significantly lower DIBL and inverse subthreshold swing were predicted.
- For SG FD SOI NMOS: a) Standard ITRS scaling; b) channel doping fixed to $1 \cdot 10^{17}$ $cm^{-3}$ instead of increasing from $6 \cdot 10^{18}$ $cm^{-3}$ in 2013 to $9 \cdot 10^{18}$ $cm^{-3}$ in 2017 and then decreasing to $1 \cdot 10^{17}$ $cm^{-3}$ in 2019; c) channel doping fixed to $1 \cdot 10^{17}$ $cm^{-3}$; d) in addition to a fixed channel doping of $2.5 \cdot 10^{18}$ $cm^{-3}$ a scaling of *EOT* more aggressive than foreseen in the ITRS was assumed. This latter scaling plan led to a good agreement

with the ITRS specifications for the drain current. Furthermore, with this scaling plan DIBL stayed below the tolerable value of 100 mV/V, and the inverse subthreshold swing for smaller channel length gets somewhat lower that specified by the ITRS.

- For DG FD SOI NMOS: a) Standard ITRS scaling; b) silicon body thickness adjusted to 40% of the channel length, instead of using more than twice the value for the single-date fully depleted SOI transistor; c) additionally, *EOT* was adapted (higher than ITRS specifications at large channel lengths, lower at small channel lengths), see Fig. 1. This latter scaling plan led to a good agreement with the ITRS specifications for the drain current, see Fig. 2. Furthermore, with this scaling plan DIBL was strongly reduced and significantly stayed below the tolerable value of 100 mV/V. Also the inverse subthreshold swing was strongly reduced.

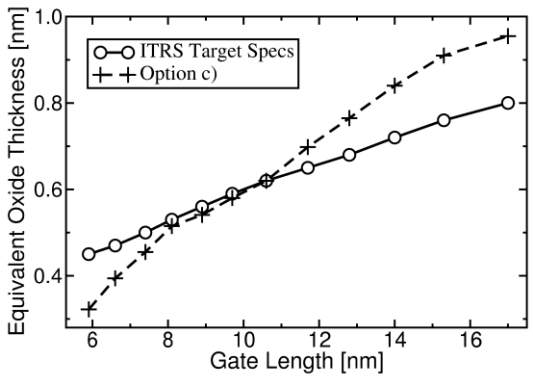


Fig. 1: Equivalent oxide thickness *EOT* as used in the scaling option c) for the DG DG FD SOI NMOS transistor, compared with original specifications for EOT from the 2011 ITRS

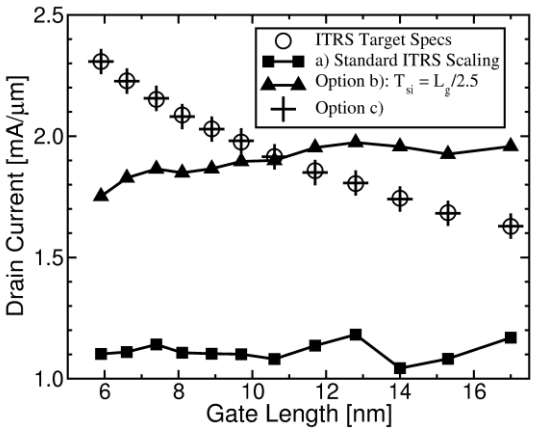


Fig. 2: Drain current specifications for the DG FD SOI NMOS transistor compared with simulation results using a) original ITRS scaling specifications; b) silicon body thickness adjusted to 40% of $L_g$; c) additionally, *EOT* adjusted as shown in Fig. 1

In the 2011 ITRS bulk NMOS was specified for channel lengths down to 14 nm, and SG FD SOI NMOS down to 11.7. For these values the drain current of both architectures was simulated to be rather similar to that of the DG FD SOI NMOS.

The simulation study performed in this work has demonstrated that all three MOSFET architectures suggested by the ITRS have the potential to achieve the electrical performance specified by the ITRS for the channel lengths in question, however with significantly modified scaling of EOT, channel doping, and/or silicon body thickness. More details of the work are given in a paper [6] submitted for publication and acknowledging SUPERTHEME. Because this deliverable is a public document this means that we should refer the reader to that publication, which will also be made available in the non-public EC and ISAB part of the SUPERTHEME WWW.

## 4. Conclusions and outlook

The work in task 6.3 “Support action to the ITRS“ was adapted to the status of the discussions in the ITRS and therefore in the reporting period referred to the scaling of nominal devices. Based on these results, the calibration work performed and the progress in the development and integration of the SUPERTHEME software system these activities will now be extended to study the impact of variations using SUPERTHEME software and results on process and device level.

## References

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