This project has received funding from the European Union's Seventh Framework Programme for research, technological development and demonstration under grant agreement no 318458.

SUPERTHEME

ICT Project no. 318458

SUPERTHEME

Circuit Stability Under Process Variability and Electro-Thermal-Mechanical Coupling

D1.9: Public Workshop on Variability

	Name	Organisation	Date
Edited	J. Lorenz	Fraunhofer IISB	Oct. 30, 2015
Reviewed	J. Park	ams	Nov. 11, 2015
Final approval	M. Nedjalkov	TU Wien	Nov. 12, 2015

Contents

Abstract

As part of its dissemination actions SUPERTHEME organized a workshop on Friday September 18, 2015, in Graz, linked to the ESSDERC and ESSCIRC conferences held there from September 15 to 17. During the last years it has developed as a standard practice that several workshops are held at the day directly following these conferences, either at or close to the conference venue. Usually some of these workshops are directly linked and/or organized by European projects. This time, there were eight full-day or half-day workshops held, up to six of which were running in parallel.

The workshop organized by SUPERTHEME was named “Variability – from equipment to circuit level”, which reflected well the scope of the project. It consisted of six presentations from SUPERTHEME, one external industrial keynote presentation on variability as an industrial challenge, and one external presentation each from the EC projects MORDRED and MORV. In total it was attended by about 20 people.

1 Introduction

For several years now, on the day after the combined ESSDERC and ESSCIRC conferences several workshops are held, covering areas addressed by either of these two conferences, in order to reach conference participants and to give them the opportunity to attend the work-shops with minimum extra travelling costs. Usually a large fraction of these workshops is organized by European RTD projects.

Following the announcement that ESSCIRC/ESSDERC 2015 will be held at Graz, close to the site of the SUPERTHEME partner ams, it was decided to postpone the SUPERTHEME workshop originally scheduled for June/July 2015 and to hold it linked to ESSCIRC/ ESSDERC.

2 Goals, agenda and outcomes of the SUPERTHEME Workshop

The objective of the workshop was twofold: First to present the concept and selected results of the project to the public, second to exchange information with related complementary projects, in this case the FP7 projects MORDRED and MORV. In view of this, besides the welcome presentation given by the SUPERTHEME project coordinator J. Lorenz five presentations were made by representatives from SUPERTHEME, namely an overview of the project, three topical presentations dealing with SUPERTHEME work at process, device and circuit level, and one on the benchmarking work carried out at the SUPERTHEME partner ams. The technical presentations were started with a talk from ST on variability as a challenge for industry. ST is one of the members of the Industrial and Scientific Advisory Board of SUPERTHEME. Two further presentations dealt with the scope and selected result of the complementary FP7 projects MORDRED and MORV.

The workshop was attended by about 20 people. Assuming this as an average attendance of the up to six parallel workshops (8 workshops in total) estimated 120 total attendees would amount to 20 – 25% of the total number of the attendees of ESSCIRC and ESSDERC, a quite reasonable number on a Friday at the end of a conference week.

All presentations enjoyed large interest by the audience. The discussions were not only held between presenters and external participants without own talks, but especially also between

speakers from SUPERTHEME and the three external ones. This has opened up the scene for some follow-up exchange of further information and actions.

3 Summary of workshop presentations and its dissemination via the WWW

This section gives a very brief summary of some aspects of the presentations and furthermore outlines the dissemination path and action.

3.1 Key messages from presentations

Some key messages from the presentations are listed in the order of the agenda:

- J. Lorenz, Fraunhofer IISB: Welcome and Orientation

  This short introduction referred to the EC funding and presented both the SUPERTHEME consortium and the agenda for the workshop.

- A. Juge, ST: Variability at all levels – a challenge for the semiconductor industry

  The presentation included a wealth of industrial requirements and experimental results, showing among others data from ST, from literature and simulations partly from GU / GSS.

  Among others A. Juge pointed out that at transistor level random variations are dominant for devices at critical dimension, while random variations are averaged out at circuit level, and systematic variations are revealed here. The example shown was a ring oscillator with 99 stages, and the conclusion of course depends on the complexity of the circuit. This is a good additional argument for the combined treatment of random (=statistical) and systematic variability in SUPERTHEME.

  Part of the conclusion was that variability effects “must be addressed concurrently by dedicated developments in Technology, Characterization, Modeling, CAD tools, and Circuit design.”

- J. Lorenz, Fraunhofer IISB: Overview of the SUPERTHEME project

  He introduced variations and the SUPERTHEME objectives, shortly presented background work as the baseline of the project, showed project data and project structure, and presented an example for the simulation of the combined effect of three systematic and three statistical process variations on nominal 23.5 nm bulk transistors

- A. Shluger, University College London: Defects responsible for BTI in CMOS devices: MORDRED perspective

  He introduced the MORDRED project and highlighted the need and objective to link atomistic modeling of various defects with continuum device modeling. A key result of MORDRED is the development of a “multi-scale methodology for determining defects in the gate oxide and interface layer responsible for fixed charge and BTI”. MORDRED and SUPERTHEME are apparently linked by the involvement of GSS, GU and TU Wien in both projects.

- E. Bär, Fraunhofer IISB: Variability-aware process simulation in SUPERTHEME

  E. Bär summarized the scope of the process simulation work in SUPERTHEME, described the software components developed and/or used, and discussed an example on plasma-enhanced chemical vapor deposition, e.g. concerning variations of the ion and neutral fluxes leading toacross-wafer variations of thicknesses of deposited lay-

ers and DC capacitances of TSV structures. Finally he discussed variations in Spacer Patterning for FinFET SRAM cells.

- S. Amoroso for A. Asenov, GU / GSS: Variability-aware device simulation in SUPERTHEME.

  A. Asenov could on short notice not give the presentation himself, and sent S. Amoroso instead. In the presentation he among others differentiated between the various kinds of variations and outlined the variability simulation approaches employed in the GSS tool GARAND. He outlined the combined simulation of systematic and statistical variability within SUPERTHEME and the GSS toolset. The two main conclusions were 1) VARIABILITY is a maker or breaker of advanced MOSFET technology, and 2) Accounting for both PROCESS and STATISTICAL variability (and their interplay) is mandatory for optimizing design margins and developing predictive early-stage PDKs.

- R. Minixhofer, ams: Covering variability from unit process up to circuit level for mixed-signal circuits

  Overview of the results obtained in the benchmarks run in the project: Four on circuit component level, two on circuit level

  Key conclusion: “The established causalities between system behavior and underlying processing variability will enable new much higher optimized integrated systems in future.”

- C. Millar, GSS: Variability-aware SPICE modeling and circuit simulation in SUPERTHEME

  Outline of the overall simulation system developed in SUPERTHEME and especially of the method established in GSS software for the extraction of process-aware compact models. Exemplary presentation of variations in an SRAM circuit.

  Key conclusion: The developed process and statistical variability aware compact modelling methodology and the ModelGEN SPICE model generator enable a true TCAD Design/Technology Co-Optimisation (DTCO) flow.

3.2 Publication at the WWW pages of ESSCIRC/ESSDERC and of the SUPERTHEME project

In the appendix, printouts of the material presented at the internet are shown, as follows:

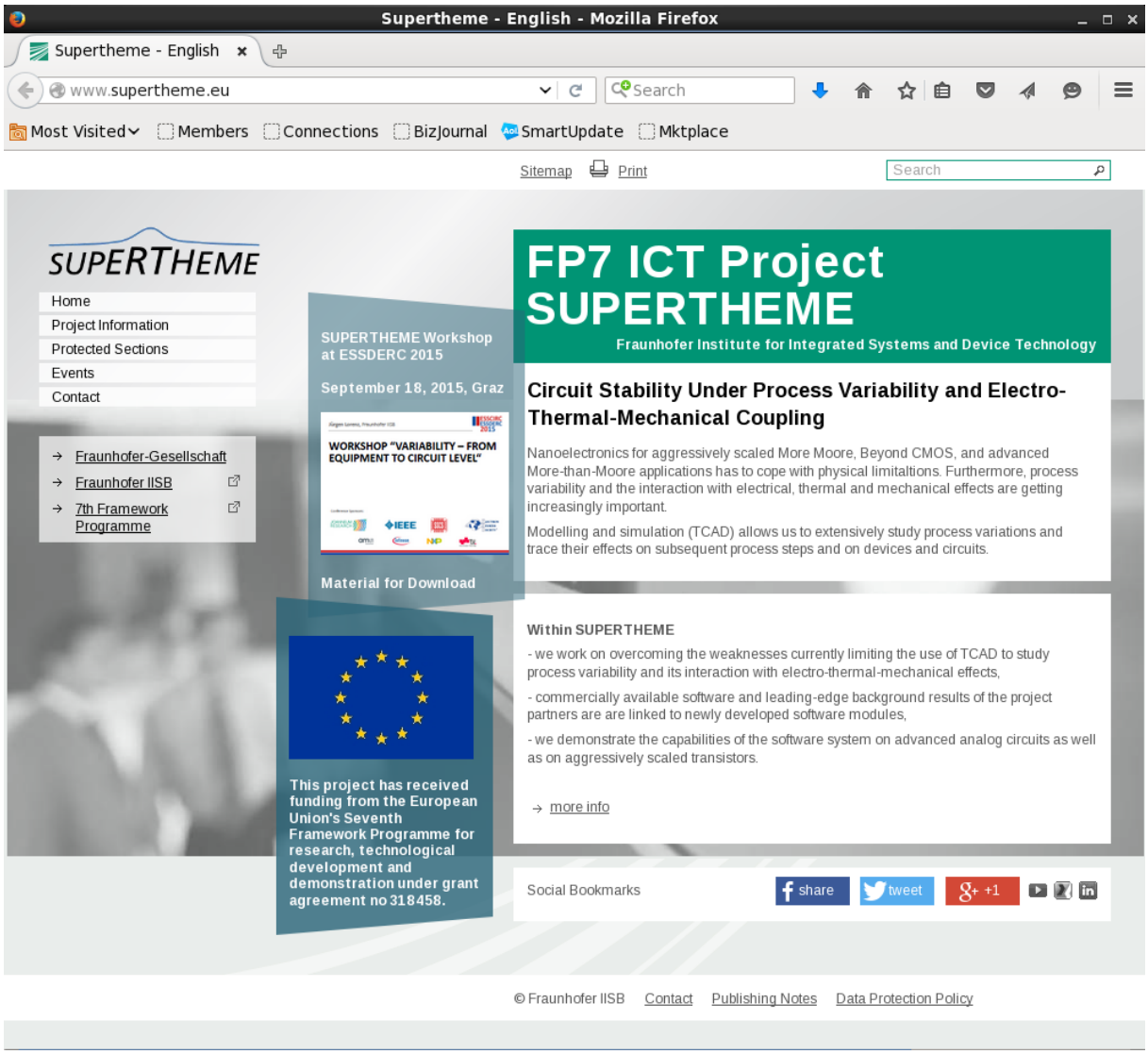
- Reference given at the public SUPERTHEME WWW page (as of October 28, 2015). The workshop presentations can be downloaded here.
- References given at the WWW pages of ESSCIRC/ESSDERC 2015 (http://www.essderc2015.org/en/sistemacongressi/european-solid-state-device-conference-2015/website/home/workshops/ and http://www.esscirc2015.org/en/sistemacongressi/european-solid-state-circuits-conference-2015/website/home/workshops/. The link provided by SUPERTHEME was only implemented by the ESSCIRC/ESSDERC organizers on Oct. 30, enabling the finalization of the deliverable and the start of its quality assurance process.
- Agenda and CV of the presenters as accessible from the ESSCIRC/ESSDERC WWW page
- The full set of the presentations given, as shown on the WWW pages of ESSCIRC/ESSDERC and of SUPERTHEME. Two presentations had been slightly modified during the internal release procedures at ams and ST.

4 Conclusions

The SUPERTHEME project organized the workshop “Variability – from equipment to circuit level” linked to ESSCIRC/ESSDERC 2015 in Graz, Austria. The workshop consisted of presentations from the project plus three external ones, and was attended by about 20 people. All presentations enjoyed large interest by the audience. The discussions were not only held between presenters and external participants without own talks, but especially also between speakers from SUPERTHEME and the three external ones. This has opened up the scene for some follow-up exchange of further information and actions. The presentations have been made available to the broad audience after the workshop via the ESSCIRC/ESSDERC WWW and the public SUPERTHEME WWW page.

Appendix: WWW presentations

The page numbers given below are the **pdf file page numbers**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Fraunhofer IISB
7th Framework Programme
SUPERTHEME Workshop at ESSDERC 2015
September 18, 2015, Graz
WORKSHOP "VARIABILITY – FROM EQUIPMENT TO CIRCUIT LEVEL"
Material for Download
This project has received funding from the European Union's Seventh Framework Programme for research, technological development and demonstration under grant agreement no 318458.
FP7 ICT Project SUPERTHEME
Fraunhofer Institute for Integrated Systems and Device Technology
Circuit Stability Under Process Variability and Electro-Thermal-Mechanical Coupling
Nanoelectronics for aggressively scaled More Moore, Beyond CMOS, and advanced More-than-Moore applications has to cope with physical limitaltions. Furthermore, process variability and the interaction with electrical, thermal and mechanical effects are getting increasingly important.
Modelling and simulation (TCAD) allows us to extensively study process variations and trace their effects on subsequent process steps and on devices and circuits.
Within SUPERTHEME
- we work on overcoming the weaknesses currently limiting the use of TCAD to study process variability and its interaction with electro-thermal-mechanical effects,
- commercially available software and leading-edge background results of the project partners are are linked to newly developed software modules,
- we demonstrate the capabilities of the software system on advanced analog circuits as well as on aggressively scaled transistors.
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ESSDERC 2015

45th European Solid-State Device Conference

September 14-18, 2015 - Graz, Austria

Workshops

A Workshop Day will be organized on Friday, 18 September, 2015
and will take place at the Graz University of Technology, Campus Inffeldgasse.

On-site Registration: 8:00 to 18:00

Inffeldgasse 25 D

The venue can easily be reached per tram:

Get on **line 6** (direction St. Peter), station Schulzentrum.

There is free parking at the Campus Inffeldgasse:

Workshop 1 (Room 1, Inffeldgasse 25d, 9:00 to 16:00)

MOS-AK: Enabling Compact Modeling R&D Exchange

Lead Organizer: Dr.-Ing. Wladek Grabinski, MOS-AK (EU)

The specific workshop goal will be to classify the most important directions for the future development of the electron device models, not limiting the discussion to compact models, but including physical, analytical and numerical models, to clearly identify areas that need further research and possible contact points between the different modeling domains. This workshop is designed for device process engineers (CMOS, SOI, BiCMOS, SiGe) who are interested in device modeling; ICs designers (RF/Analog/Mixed-Signal/SoC) and those starting in that area as well as device characterization, modeling and parameter extraction engineers. The content will be beneficial for anyone who needs to learn what is really behind the IC simulation in modern device models.

Agenda:
09:00 Morning MOS-AK Session
11:00 CM Standardization Panel

Organizer and Regional Partners

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12:00 Lunch
13:00 **Afternoon MOS-AK Session**
16:00 End of Workshop

Find all the PRESENTATIONS of the workshop at: http://www.mos-ak.org/graz_2015

Workshop 2 (Room 2, Inffeldgasse 25d, 8:45 to 16:00)

SINANO Workshop "New Materials for Nanoelectronic" (Full day)

Lead Presenter: Prof. Enrico Sangiorgi, University of Bologna

Presentations at the conference

Program

This Workshop is supported by the European Institute of Nanoelectronics SINANO (www.sinano.eu) and aims at discussing state-of-the-art results and disruptive achievements in the field of New Materials for Nanoelectronics. The integration of new materials (e.g. III-V compound semiconductors) on silicon platforms is foreseen as the next major evolution of advanced CMOS technology nodes. The introduction of such a disruptive innovation is a long term process where complex technological experiments must be matched by accurate Technology Computer Aided Design (TCAD) in order to reduce cost and to explore in a timely manner the available engineering options. In this workshop, leading experts in the field will report on the most recent results in fabrication, characterization and modelling of nanoelectronic devices based on new materials. Workshop highlights include a demonstration and hands-on tutorial of atomic-scale simulation that will give the audience the possibility of running examples on their own computers.

Agenda:

8:45 **Introduction** Enrico Sangiorgi, SiNANO Institute

9:00 **Integration of III-V Devices on a Si Platform** Nadine Collaert, IMEC

9:40 **TCAD Device Simulation Frame for III-V MOS Device, Synopsy Representatives** Axel Erlebach, Fabian Bufler and Martin Frey, SYNOPSYS

10:20 **III-V Heterostructures and Transition Metal Dichalcogenides for Tunnel-FETs** Marco Pala, IMEP-LAHC, Grenoble INP, NRS

11:00 Coffee Break

11:30 **Graphene and Two-Dimensional (2D) Materials for Nanoelectronics** Vikram Passi, University of Siegen

12:00 **Investigating the High-k/InGaAs MOSSystem for Future Logic Applications** Paul Hurley, Tyndall

12:30 Lunch

13:45 **Demonstration and Hands-on Tutorial of Atomic-Scale Simulation with ATK**
Troels Markussen, Umberto Pozzoni, QuantumWise

16:00 Coffee Break and End of Workshop

Workshop 3 (Room 5, Inffeldgasse 25d, 8:45 to 15:30)

"Variability – From Equipment to Circuit Level" (Full day)

Lead Presenter: Dr. Jürgen Lorenz, Fraunhofer IISB

Presentations at the conference

Program

CVs of presenters

This workshop deals with process variability which is one of the key physical limitations which challenge progress in nanoelectronics. Effects from various sources of process variations, both systematic and stochastic, influence each other and lead to variations of

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ChipDesign
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ECSEL Joint Undertaking
GTS
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TOSHIBA Leading Innovation

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the electrical, thermal and mechanical behavior of devices, interconnects and circuits. Correlations are of key importance because they drastically affect the percentage of products which meet the specifications. Whereas the comprehensive experimental investigation of these effects is largely impossible, modelling and simulation (TCAD) offers the unique possibility to predefine process variations and trace their effects on subsequent process steps and on devices and circuits fabricated, just by changing the corresponding input data. This important requirement for and capability of simulation is among others highlighted in the International Technology Roadmap for Semiconductors ITRS.

In view of this in the FP7 project SUPERTHEME a software system has been developed which enables the simultaneous assessment of the impact of systematic variations caused by process equipment and statistical variations caused by the granularity of matter on advanced More Moore and More than Moore devices and circuits. Within this workshop variability challenges will be outlined, and a selection of results obtained in SUPERTHEME will be presented. Furthermore, it is planned to also introduce related projects which are complementary to SUPERTHEME.

Agenda:

8:45 **Welcome and Orientation**
Jürgen Lorenz, Fraunhofer IISB

9:00 **Variability at all Levels - A Challenge for the Semiconductor Industry**
Andre Juge, ST

9:30 **Overview of the SUPERTHEME Project**
Jürgen Lorenz, Fraunhofer IISB

10:00 **Defects Responsible for BTI in CMOS Devices: MORDRED Perspective**
Alexander Shluger, UCL

10:30 **Variability Aware Process Simulation in SUPERTHEME**
Eberhard Bär, Fraunhofer IISB

11:00 Coffee Break

11:30 **Variability Aware Process Simulation in SUPERTHEME**
Asen Asenov, GU/GSS

12:00 **Hierarchical Modeling of Reliability and Time Dependent Variability in the MORV Project**
Ben Kaczer, IMEC

12:30 Lunch

14:00 **Covering Variability from Unit Process up to Circuit Level for Mixed – Signal Circuits**
Rainer Minixhofer, ams

14:30 **Variability Aware SPICE Modeling and Circuit Simulation in SUPERTHEME**
Campbell Millar, GSS

15:00 **Open Discussion and Concluding Remarks**

15:30 End of Workshop

www.supertheme.eu

Workshop 4 (Room 4, Inffeldgasse 25d, 14:00 to 17:30)

"Electromagnetic Compatibility of Integrated Circuits" (Half day)

Lead Presenter: Prof. Bernd Deutschmann, Ass.-Prof. Gunter Winkler, Graz University of Technology

Presentations at the conference

Today very complex electronic systems often consisting of large digital cores, analog and mixed-signal circuits, as well as power electronic devices can be realized in one single chip. But, as device dimensions are shrinking, ICs are often becoming more susceptible to electromagnetic interferences; on the other hand internal switching frequencies of modern ICs increasing, resulting in higher electromagnetic emission. Therefore, the design of ICs that are compliant to electromagnetic compatibility (EMC)

specifications has become more and more challenging during the last years. Noise signals such as radio-frequency interferences or transient disturbances such as electrostatic discharges (ESD) can interfere with the operation of the ICs and particularly with the analog circuits embedded in such devices. The undisturbed operation of electronic systems is of vital importance for safety and reliability and should therefore be of particular concern for designers of integrated circuits. In the first part of this workshop an introduction to EMC at the IC level as well as an overview of the most important EMC measurement techniques that are used for the characterization of the emission and immunity of ICs are given. In the further parts carefully selected IC design related topics such as the susceptibility to electromagnetic interferences of sensor signal conditioning circuits, the influences of packaging, connectors, PCB traces and ground planes on the performance of ICs with respect to EMC, as well as on-chip decoupling to improve the EMC of ICs will be presented.

Presentations at the conference

Agenda:

14:00 **Introduction to EMC at the IC Level, EMC Measurement Techniques of ICs**

Bernd Deutschmann, Gunter Winkler

14:40 **Susceptibility to EMI of Sensor Signal Conditioning Circuits**

Franco Fiori

16:00 Coffee Break

16:30 **Pro and Cons of Onchip Decoupling to improve the EMC of Integrated Circuit**

Timm Ostermann

17:30 End of Workshop

Workshop 5 /Room 4, Inffeldgasse 25d, 8:30 to 13:00)

"Variation-Aware Design for RF Engineers" (Half day)

Lead Presenter: Dr.-Ing. Stephan Weber, Cadence Design Systems

Presentations at the conference

Creating an RF design is always a challenge, but producing it with acceptable yield is even more difficult. We start with discussing Monte-Carlo and PVT corner analysis, and their measures and problems like confidence intervals, uncertainties from non-normal distributions, etc. Then moving over to advanced techniques for yield prediction and optimization. A demo will be given using Cadence Virtuoso ADE GXL for design of RF key blocks.

Agenda:

8:30-9:30	Hans Meyvaert (KU Leuven, Belgium): **Switched Capacitor DC-DC Converters: Concepts and Control Techniques**
9:30-10:30	Vadim Ivanov (TI, USA): **How to avoid most common mistakes in DCDC design: Voltage mode, PWM and fixed frequency**
10:30-11:00	--- Break ---
11:00-12:00	Luca Corradini (University of Padova, Italy): **Digital Control for Inductor Based DC-DC Converters**
12:00-13:00	Jesus A. Oliver (UPM Madrid, Spain): **Ripple-Based Control Techniques for Buck Type DC-DC Converters**

Workshop 6 (Room 3, Inffeldgasse 25d, 8:45 to 12:30)

"RFID Technologies Exploiting 2D and 3D Printing and Packaging Techniques" (Half day)

Lead Presenter: Prof. Wolfgang Bösch, Graz University of Technology

Presentations at the conference

Radio frequency identification (RFID) is a technology that offers the possibility of reading or changing data through radio waves without the need for contact. This allows the automatic identification and location of objects and makes the collection of data easier and covers a diverse application ranges. Styrian RFID companies – mostly situated around Graz – are highly renowned in the field of RFID technologies: more than 50% of RFID chips in use worldwide have been developed in Styria. In future developments, RFID transponder (tag) realizations will exploit the capabilities of 2D and 3D printing and packaging technologies such as the inkjet printing and embedded wafer-level ball grid array (eWLB) packaging technologies. This workshop will cope with this development and will give the workshop participants insight into recent developments in these areas.

Agenda:

08:45 **Welcome and Presentation of the RFID Hotspot in Graz/Styria**
Wolfgang Boesch, Graz University of Technology

09:20 **Presentation and Discussion "RFID Techno-logies Exploiting 2D and 3D Printing and Packaging Techniques"**
Jasmin Grosinger, Graz University of Technology

10:10 **Presentation and Discussion "Printed Electronics – Materials, Processes and Innovative Applications"**
Andreas Klug, NanoTec Center

11:00 Coffee break

11:30 **Presentation and Discussion "Advances in Packaging for RF Applications"**

Klaus Pressel, Infineon Technologies

12:20 **Final Discussion**

12:30 End of Workshop

Workshop 7 (Room 6, Inffeldgasse 12, 8:30 to 13:00)

"DC-DC Converter Techniques" (Half day)

Lead Presenter: DI Christoph Sandner

Presentations at the conference

This workshop will give insights into different key aspects of DC-DC converter concept and design. The designated speakers are worldwide recognized experts in this field. We target one speech in each of these fields: Inductor based converters, switched capacitor converter concepts and control techniques, buck converter control and stability, and last not least a talk about how to avoid most common mistakes in DC-DC converter circuit design.

Agenda:

8:30 **Switched Capacitor DC-DC Converters: Concepts and Control Techniques**
Hans Meyvaert, KU Leuven, Belgium

9:30 **Inductor Based DC-DC Converters**
tba

10:30 Coffee Break

11:00 **Ripple-Based Control Techniques for Buck Type DC-DC Converters**

Jesus A. Oliver, UPM Madrid, Spain

12:00 **How to Avoid Most Common Mistakes in DCDC Design: Voltage Mode, PWM and fixed Frequency**
Vadim Ivanov, TI, USA

13:00 End of Workshop

Workshop 8 (Room 3, Inffeldgasse 25d, 14:00 to 17:30)

"From Atom to Transistor"

Models and Techniques for Predictive Simulation of Emerging Devices (Half Day)

Organizer: Zlatan Stanojević, Global TCAD Solutions (Austria), z.stanojevic@globaltcad.com

Presentations at the conference

Program

Culminating in a live demonstration, this workshop discusses latest models and techniques for achieving new levels of detail in semiconductor device simulation. The used simulation tools provide excellent accordance with measured data as well as unprecedented insight in underlying physical phenomena.

50 years after the inception of Moore's Law, industry is facing ever increasing hurdles on the roadmap to produce devices which perform better and consume less power. The challenges in introduction of new technology nodes pose great risks to manufacturers, and there is always more than one possible way to proceed. Selecting apt models and tools is becoming increasingly important to efficiently gain profound data for making good decisions in device design and optimization. Especially for new technologies and nano-scaled devices, additional physical phenomena, such as quantum effects, need to be considered for meaningful analysis.
In this workshop, a methodological hierarchy of tools will be presented – ranging from atomistic models up to extraction of device parameters and optional circuit simulation, which consistently yields results well-founded in physics. Emerging device concepts will be covered, demonstrating how the chosen approach can help assess the risks involved in the introduction of new technologies. Depending on the audience's priorities, a mixed-mode device and circuit simulation can be carried out with the generated data at the end of the live demonstration.
http://www.globaltcad.com/essderc

Agenda:

14:00 **Extracting Materials Properties for Semiconductor Device Simulation from Ab-Initio and Atomistic Simulation**
Erich Wimmer, Materials Design s.a.r.l. (France)

14:30 **Blessing or Curse: Dissipative Quantum Transport in Nano-Scale Devices**
Hans Kosina, Vienna University of Technology, Institute for Microelectronics

15:00 **Just enough Quantum – Combining Semi-classical and Quantummechanical Models for Fast and Predictive Device Simulation**
Zlatan Stanojević, Global TCAD Solutions GmbH

15:30 **Modeling Reliability under Variability in Nano-Scale Devices**
Ben Kaczer, IMEC (Belgium)

16:00 Coffee Break

16:30 **Predictive Simulation in Action: Selected Case Studies — Live Demonstration**
Zlatan Stanojević, Erich Wimmer

17:30 End of Workshop

Information for workshop organizers

ESSDERC/ESSCIRC workshops offer network of researchers a unique opportunity to exploit the logistics of the conference and the presence on-site of a large number of potential participants to meet and present the result of a project, discuss the frontiers of novel research topics, foster new collaborations, share views and know-how. Here follows a list of the fundamental information for perspective workshop organizers:

- Prospective organizers should contact the workshop program chairs Mario Auer (mario.auer@tugraz.at), Gernot Hueber (gernot.hueber@gmail.com) or Bernd

Deutschmann (bernd.deutschmann@tugraz.at) by the **deadlines given below** with the following information:

- **24 March, 2015:** title and short description of the workshop; name, affiliation and e-mail contact of the organizer(s).
- **21 April, 2015:** full program of the workshop (abstract, schedule with title, time, speaker name and affiliation of each talk). The program will be posted on a dedicated page of the conference website. Alternatively, the organizers may report the URL of the website with the workshop full program. The available time-slots will be assigned on a first-come first-serve basis.

- An registration fee of € 35,00 is due by the **attendees** as partial coverage of the catering expenses, if they are registered participants of the main conference. Otherwise a workshop registration fee of € 120,00 is applied.
- The **organizer** of a workshop may also conclude a lump sum agreement with the conference organization in order to waive the individual participant's fees.
- A room with projection equipment will be reserved for each workshop, and a lunch and two coffee breaks will be served to the attendees.
- In order not to interfere with the technical program of the conference, the workshop day is **Friday, 18 September, 2015.**

Prospective organizers may also be interested in taking a look at the workshop program of the last conference:

- ESSDERC/ESSCIRC 2014 workshop program (http://www.esscirc2014.org/en/sistemacongressi/european-solid-state-circuits-conference-2014/website/home/workshops/)

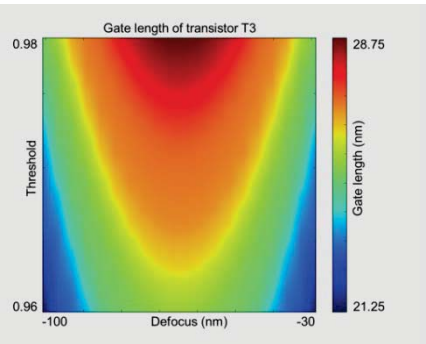
This project has received funding from the European Union's Seventh Framework Programme for research, technological development and demonstration under grant agreement no 318458.

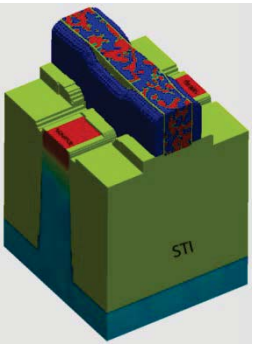
SUPERTHEME

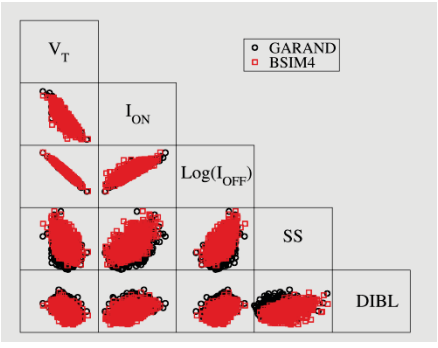
ESSDERC 2015 Workshop "Variability – from Equipment to Circuit Level"

Graz, September 18, 2015

8:45 – 9:00	Welcome and orientation, J. Lorenz, Fraunhofer IISB
9:00 – 9:30	Variability at all levels – a challenge for the semiconductor industry, A. Juge, ST
9:30 – 10:00	Overview of the SUPERTHEME project, J. Lorenz, Fraunhofer IISB
10:00 – 10:30	Defects responsible for BTI in CMOS devices: MORDRED perspective, A. Shluger, UCL
10:30 – 11:00	Variability-aware process simulation in SUPERTHEME, E. Bär, Fraunhofer IISB
11:00 – 11:30	Coffee break
11:30 – 12:00	Variability-aware device simulation in SUPERTHEME, A. Asenov, GU/GSS
12:00 – 12:30	Hierarchical modeling of reliability and time-dependent variability in the MORV project, B. Kaczer, IMEC
12:30 – 14:00	Lunch
14:00 – 14:30	Covering variability from unit process up to circuit level for mixed-signal circuits, R. Minixhofer, ams
14:30 – 15:00	Variability-aware SPICE modeling and circuit simulation in SUPERTHEME, C. Millar, GSS
15:00 – 15:30	Open discussion and concluding remarks







Simulation examples: Gate length vs. focus and dose variations in optical lithography (IISB - left); atomistic device simulation with variability sources *RDD, LER and MGG* (GU - middle); scatterplots of figures or merit obtained from statistical models and GARAND (GSS - right)

Speakers from the SUPERTHEME project

Dr.-Ing. **Jürgen Lorenz** obtained his degrees as “Diplom-Physiker” and “Diplom-Mathematiker” from the Technical University of Munich, and his PhD (“Dr.-Ing.”) in Electrical Engineering from the University of Erlangen-Nuremberg. Since 1985 he is head of the simulation department of Fraunhofer IISB in Erlangen, Germany. His main subjects are the development of physical models and programs for semiconductor process simulation and the required algorithms. He has been involved in 33 European projects and acted as coordinator for 8 of them, including the current FP7 project SUPERTHEME. He contributes since 2000 to the International Technology Roadmap on Semiconductors, and has been the chairman of its Modeling and Simulation chapter from 2002 to 2013.

Dr.-Ing. **Eberhard Bär** was born in Darmstadt, Germany, in 1967. He received the "Diplom-Physiker" degree with specialization in experimental solid-state physics from Darmstadt University of Technology in 1992, and the Dr.-Ing. in Electrical Engineering from the University of Erlangen-Nuremberg in 1998. In 1992 he joined Fraunhofer IISB, where he is now in charge of the structure simulation group. His current research interests focus on the development and application of topography simulation tools in semiconductor technology.

Asen Asenov (PhD, FRSE, FIEEE) is the James Watt Professor of Electrical Engineering and the leader of the Glasgow Device Modelling Group. He is an expert in solid state and semiconductor physics, modelling and simulation of semiconductor devices and CMOS device design and variability. He has published more than 700 related papers. He also has given more than 180 invited talks on advanced modelling and simulation of statistical variability including VLSI Tech. Symp. and IEDM. He is member of the IEEE EDS TCAD Committee, a co-author of the More Moore domain of ENIAC SRA and has been a reviewer of 12 FP5 and FP6 projects. He is also a CEO and co-founder of Gold Standard Simulations, Ltd.

Campbell Millar (BEng, PhD, MIEE) is the VP for Software Development of GSS directing the development of the GSS software tools and facilitation the provision of physical simulation, compact model extraction and statistical circuit simulation services to customers. Before moving to GSS he was a Senior Research Fellow in the Department of Electronics and Electrical Engineering of GU and eScience project coordinator of NanoCMOS, a flagship UK project on simulation and analysis of the impact of statistical variability on transistors, circuits and systems.

Dipl. Ing. Dr. tech. **Rainer Minixhofer** is Director of Solutions R&D at ams AG responsible for all sensor solution related R&D functions like packaging, test, software and IP. He has more than 20 years of experience in the field of semiconductors, TCAD, device development and more recently in the areas of ESD, EMC and high performance analog IP. He has published about 60 related papers. He is Senior Member of the IEEE and was reviewer for FP5 and FP6 projects.

External speakers

Andre Juge graduated with a PhD degree from Université Scientifique et Médicale de Grenoble. Starting 1988, he held positions as Modeling Engineer and Team leader in STMicroelectronics R&D, to support development of BICMOS and CMOS technologies. In 2002, he became Modeling manager within Crolles2 Alliance, France, to support the development of 90nm, 65nm, and 45nm Bulk CMOS technologies. Since 2007, his activities are devoted to Advanced modeling solutions through cooperative projects with Academia, Compact Model Council (CMC), and EDA tool suppliers.

Alexander Shluger graduated from the Latvia State University, Riga, USSR in 1976, received Ph.D and Doctor of Science degrees from the L. Karpov Physics and Chemistry Research Institute, Moscow in 1981 and 1988, respectively. He joined the Royal Institution of Great Britain, London in 1991 and the faculty of the University College London in 1996, where he is a Professor of Physics from 2004. He has been appointed a head of Condensed Matter and Materials Physics group in 2006. He is a Fellow of the Institute of Physics and of the American Physical Society, a Foreign Member of the Latvian Academy of Sciences and a Principal Investigator at the WPI-Advanced Institute of Materials Research, Tohoku University, Japan. Main research interests concern the mechanisms of defect related processes in the bulk and at surfaces of insulators. Current research is focused on theoretical studies of defects in oxides in relation to reliability of CMOS devices, the mechanisms of photo-induced processes at oxide surfaces, and on modelling of imaging and manipulation of molecular specie at insulating surfaces using Atomic Force Microscopy.

Ben Kaczer is a Principal Scientist at imec, Belgium. He received the M.S. degree in Physical Electronics from Charles University, Prague, Czech Republic, in 1992 and the M.S. and Ph.D. degrees in Physics from The Ohio State University, Columbus, in 1996 and 1998, respectively. For his Ph.D. research on the ballistic-electron emission microscopy of SiO_2 and SiC films he received the OSU Presidential Fellowship and support from Texas Instruments, Inc. In 1998 he joined the reliability group of imec, Leuven, Belgium, where his activities have included the research of the degradation phenomena and reliability assessment of SiO_2, SiON, high-k, and ferroelectric films, planar and multiple-gate FETs, circuits, and characterization of Ge, SiGe, III-V, and MIM devices. He has co-authored more than 350 journal and conference papers, presented a number of invited papers and tutorials at international conferences, and received the 2011 IEEE EDS Paul Rappaport Award, six IEEE IRPS Best or Outstanding Paper Awards and two IEEE IPFA Best Paper Awards. He has served or is serving at various functions at the IEDM, IRPS, SISC, INFOS, WoDiM, IPFA, and ICICDT conferences. He is currently serving on the IEEE T. Electron Dev. Editorial Board.

Jürgen Lorenz, Fraunhofer IISB

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WORKSHOP "VARIABILITY – FROM EQUIPMENT TO CIRCUIT LEVEL"

Welcome and Orientation

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EC FP7 PROJECT SUPERTHEME

Circuit Stability Under Process Variability and Electro-Thermal-Mechanical Coupling

- Funded by EC within FP7
- Duration 10/2012 – 12/2015
- Overall funding 3.3 M€
- Consortium of
  - 6 companies
  - 3 research institutes/universities

This project has received funding from the European Union's Seventh Framework Programme for research, technological development and demonstration under grant agreement no 318458.

SUPERTHEME

Fraunhofer IISB

PARTNERS OF SUPERTHEME

Fraunhofer

amu

GSS

University of Glasgow

IμE

ASML

HQ-Dielectrics

ibs ion beam services

SCREEN Laser Systems & Solutions of Europe

WORKSHOP AGENDA

- This orientation
- Industrial keynote on importance of variability
- Overview on SUPERTHEME project
- Four technical presentations from SUPERTHEME
- One presentation each from related projects MORDRED and MORV
- Final discussion

ESSCIRC ESSDERC 2015

WORKSHOP AGENDA

8:45 – 9:00	Welcome and orientation, J. Lorenz, Fraunhofer IISB
9:00 – 9:30	Variability at all levels – a challenge for the semiconductor industry, A. Juge, ST
9:30 – 10:00	Overview of the SUPERTHEME project, J. Lorenz, Fraunhofer IISB
10:00 – 10:30	Defects responsible for BTI in CMOS devices: MORDRED perspective, A. Shluger, UCL
10:30 – 11:00	Variability-aware process simulation in SUPERTHEME, E. Bär, Fraunhofer IISB
11:00 – 11:30	Coffee break
11:30 – 12:00	Variability-aware device simulation in SUPERTHEME, A. Asenov, GU/GSS
12:00 – 12:30	Hierarchical modeling of reliability and time-dependent variability in the MORV project, B. Kaczer, IMEC
12:30 – 14:00	Lunch
14:00 – 14:30	Covering variability from unit process up to circuit level for mixed-signal circuits, R. Minixhofer, ams
14:30 – 15:00	Variability-aware SPICE modeling and circuit simulation in SUPERTHEME, C. Millar, GSS
15:00 – 15:30	Open discussion and concluding remarks

SUPERTHEME

Fraunhofer IISB

André Juge, STMicroelectronics

ESSCIRC ESSDERC 2015

WORKSHOP "VARIABILITY – FROM EQUIPMENT TO CIRCUIT LEVEL"

Variability at all levels – A Challenge for Semiconductor Industry

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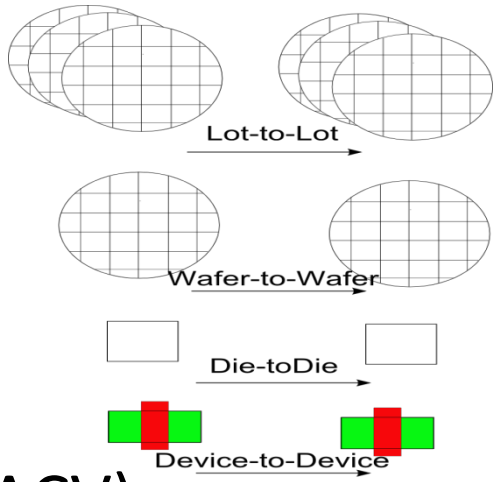
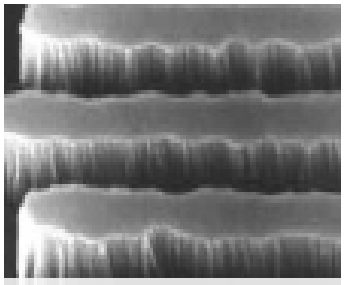
ABSTRACT

- Presentation highlights Research and Industry effort to mitigate impact of multi-level Variability sources in order to enable design of high yield manufacturable circuits
- Variability scope is wide; samples of techniques among Process variability reduction, DFM, Electrical Characterization, Compact Statistical Modeling, Design methodology are shown for illustration.
- New challenges are identified

OUTLINE

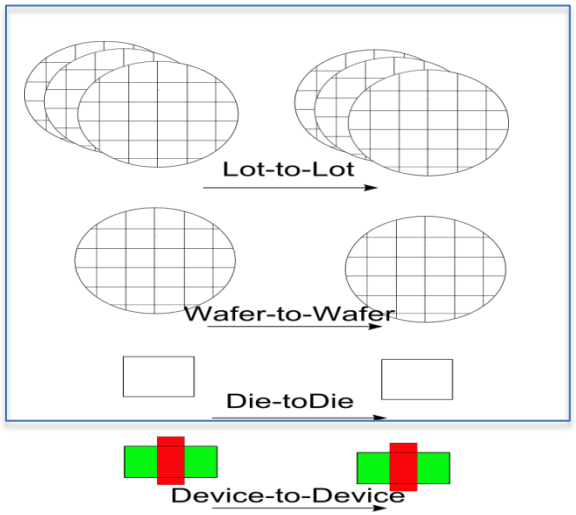


1. Introduction: Variability sources
2. Design for Manufacturing
3. Global Process Variations (Interdie)
4. Local Across Chip Variations (Intradie, ACV)
5. Local Systematic Variations (Local Layout Effects, LLE)
6. Local Statistical Variations (Mismatch)
7. Circuit simulation requirements
8. Conclusion



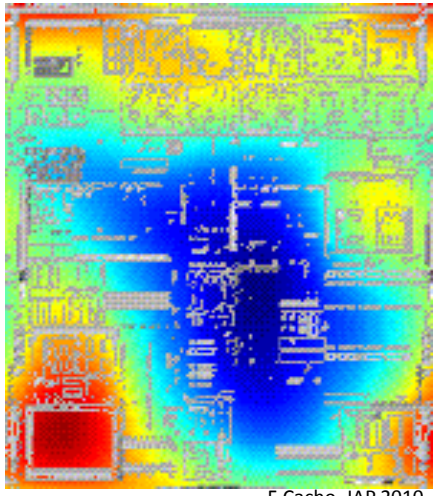
VARIABILITY SOURCES

Global Process(Interdie)



Across Chip (Intradie)

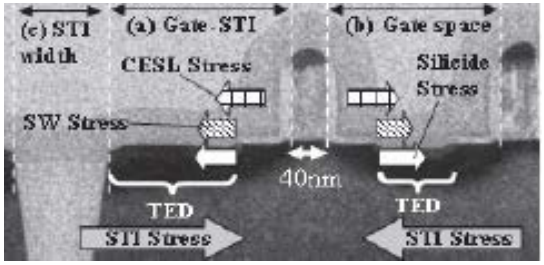
Systematic (mm-cm)



F.Cacho, JAP 2010

Local Layout Effect

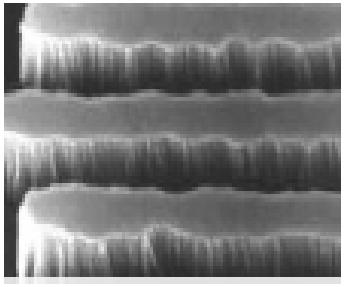
Systematic (0.1-1um)



[H.Tsuno, VLSI 2007]

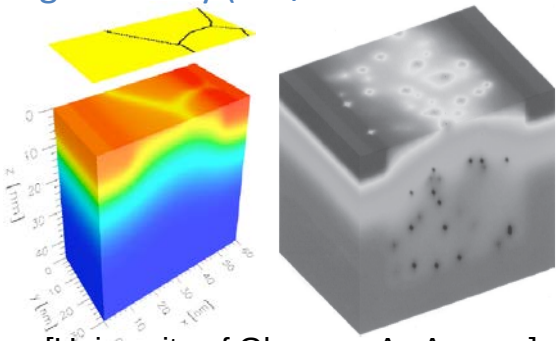
Local Random

Line edge roughness (nm)



Channel dopants (A)

PolySi granularity (nm)



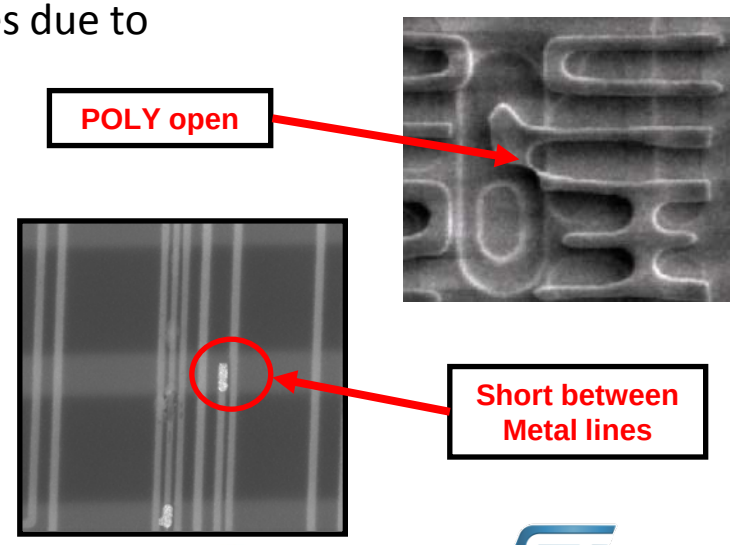
[University of Glasgow, A .Asenov]

DESIGN FOR MANUFACTURING (DFM)

- DFM is about Yield.
  - "DFM is a set of methodologies used to guide the design process so that product fabrication will have low cost, high conformance quality, low manufacturing ramp-up time and short time to market"

- DFM rules and models allow to minimize yield losses due to
  - Systematic defects
    - Product/process ramp-up
  - As well as random defectivity
    - Volume production

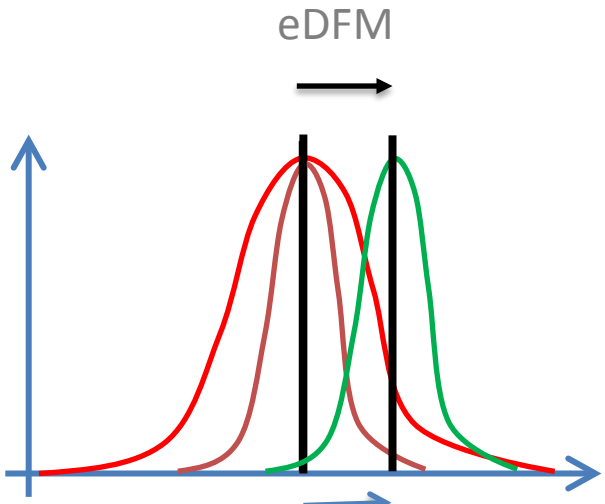
- DFM is indeed about chip functional yield …
  …. but not only…



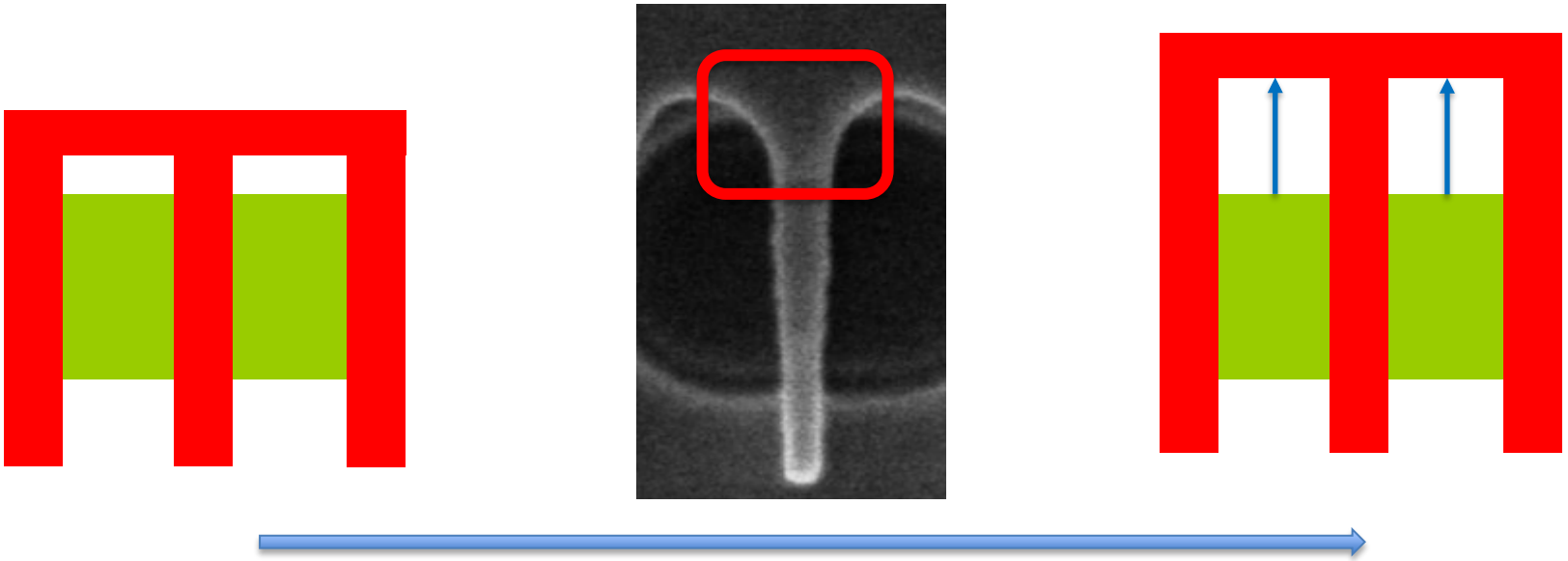
DFM VS PERFORMANCE VARIABILITY

- At nanometer technologies, process variability has become one of leading causes of chip yield loss and delayed schedules
  - designers must be aware of how complex manufacturing steps lead to device and interconnects performance variability
  - variability is to be accounted for in various design operation modes, power states/domains, leading to more complex and longer design cycles

- "electrical DFM" (eDFM) rules to
  - Reduce impact of process variability
    - Reduction of circuit performance spread
    - More dice with maximum performances
  - Verify layout design vs accurate simulation validity domain
    - Minimize discrepancy bw simulated /measured circuit performance



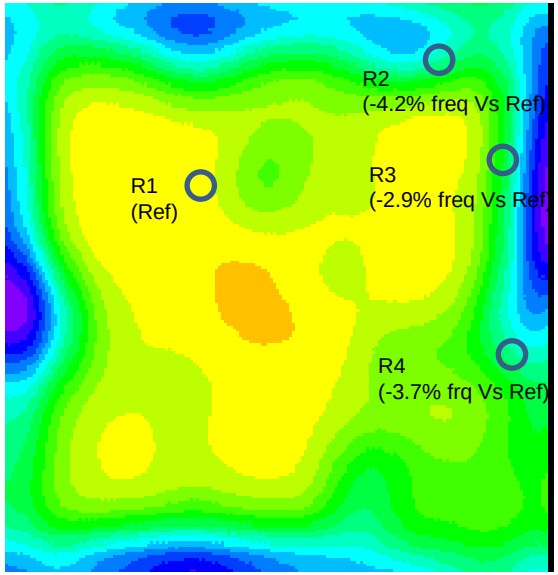
ELECTRICAL DFM VS PERFORMANCE VARIABILITY

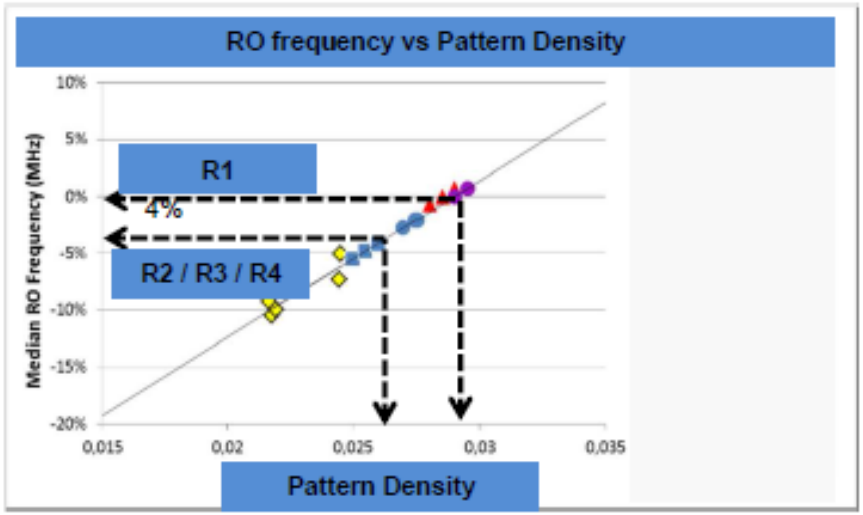


Improved channel W control
Spice model compliance (Nominal + Variations)

- Small scale eDFM example. eDFM minimizes impact of process variability on circuit performance variations and maximize CAD/Silicon correlation

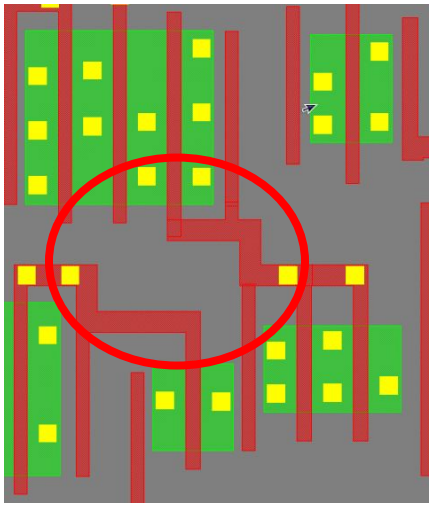
ELECTRICAL DFM VS PERFORMANCE VARIABILITY

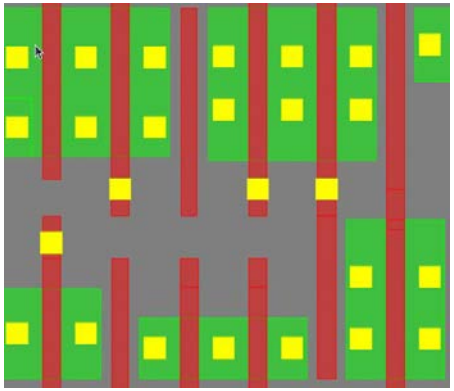




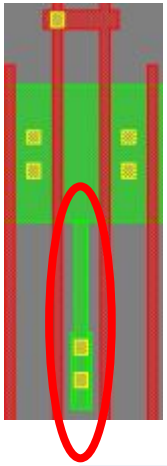
- Large scale eDFM example
  - Large variations in Pattern density lead to systematic acrosschip variations (ACV)
- Can be mitigated by layout regularity
  - Cell level (regular gate pitch, limited set of geometries,…)
  - Chip level (density/gradient design rules, smart dummy devices,…)

ELECTRICAL DFM VS CAD ACCURACY





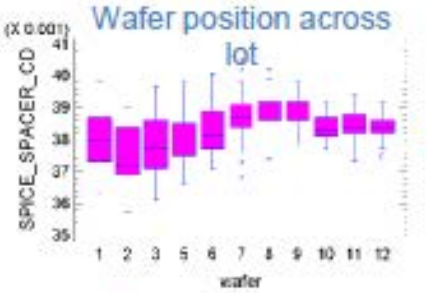
Improved CD control
Spice model accuracy

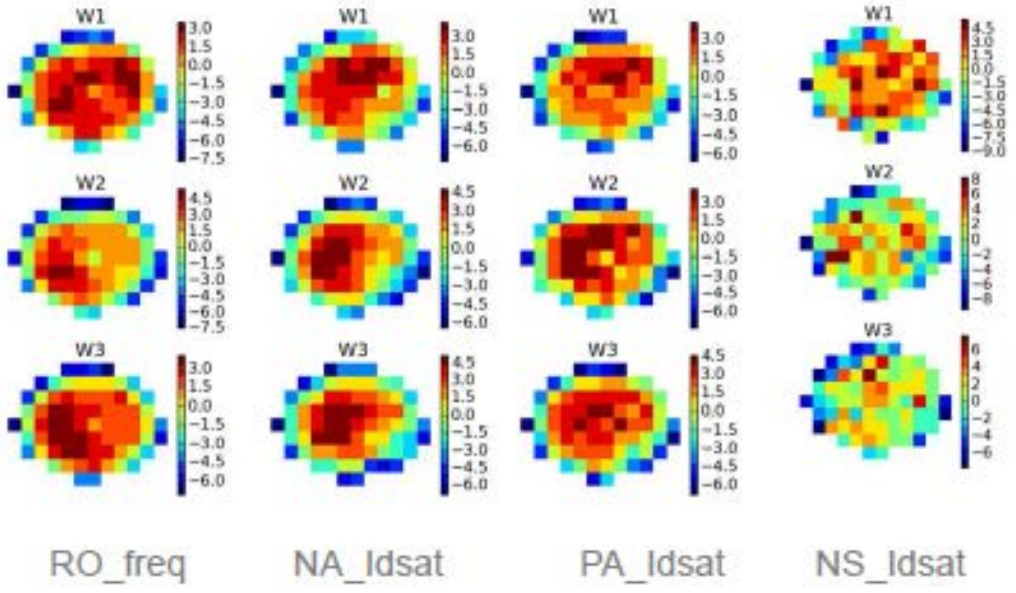


Reduced IR-Drop
PEX tool accuracy

- Need to verify layout design vs accurate simulation validity domain
  - For specific layout situation simulation may not be fully accurate
  - Allowed by DRC, nevertheless can be restricted by eDFM rules

GLOBAL PROCESS VARIABILITY



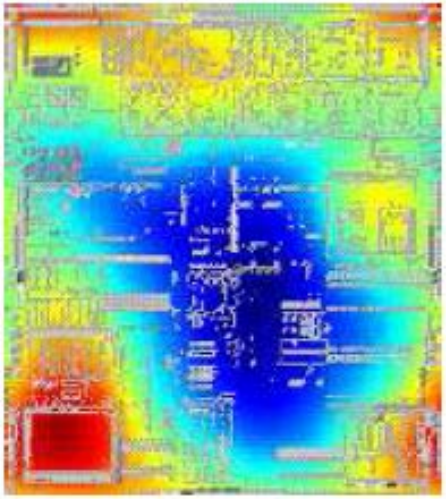


- Intrawafer die/die variations tend to dominate Global variations
- Electrical impact similar for RO delays and Mosfet currents; can be put in evidence with properly design structures [GC Castaneda ICMTS 2012]

ACROSS CHIP VARIATIONS

Anneal Temperature profile

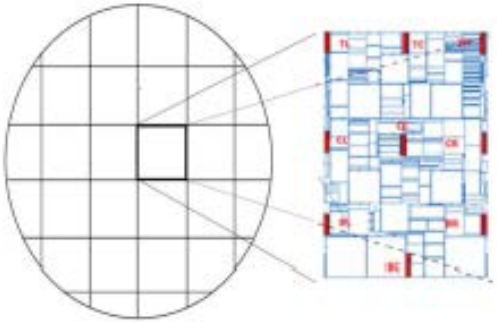
Anneal Temperature profile



[F.Cacho, JAP 2010]

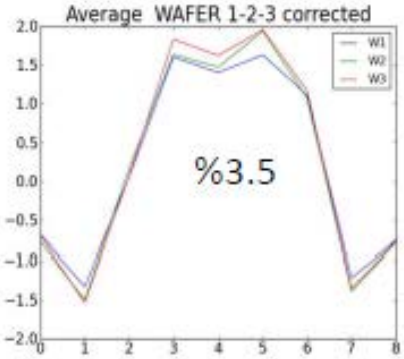
Within die sampling

(9 positions)



Within die variations

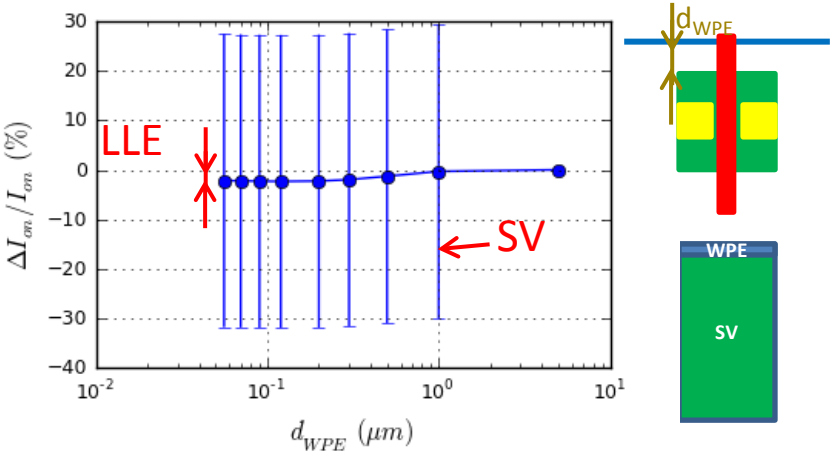
(9 positions, 3 wafers)



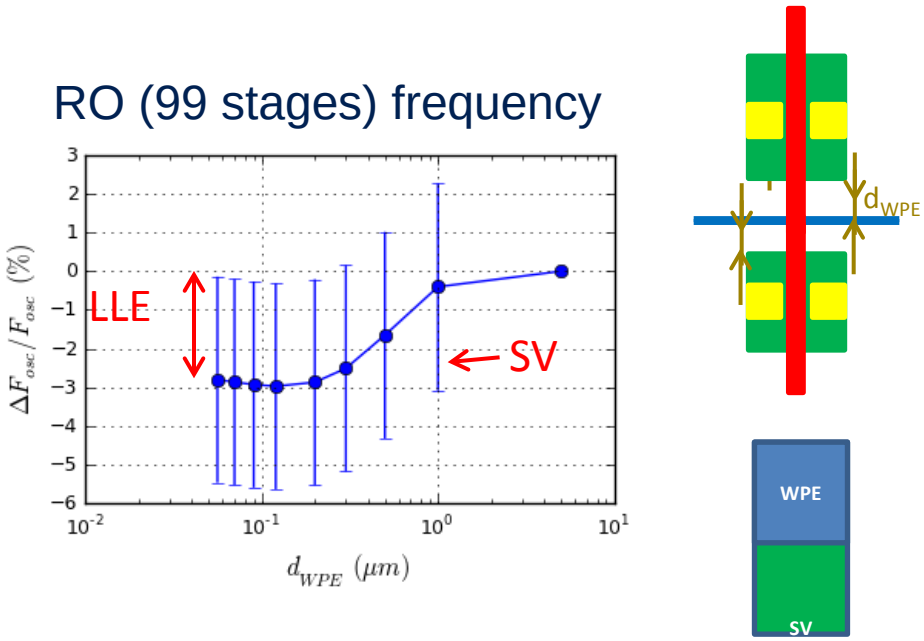
- ACV may originate from pattern density gradient within chip
- Experimental evidence with ROs , thanks to SV averaging effect
- Mitigated with smart dummy patterns to reduce density gradients

LOCAL VARIATIONS: SYSTEMATIC VS STATISTICAL

Transistor I_{on}



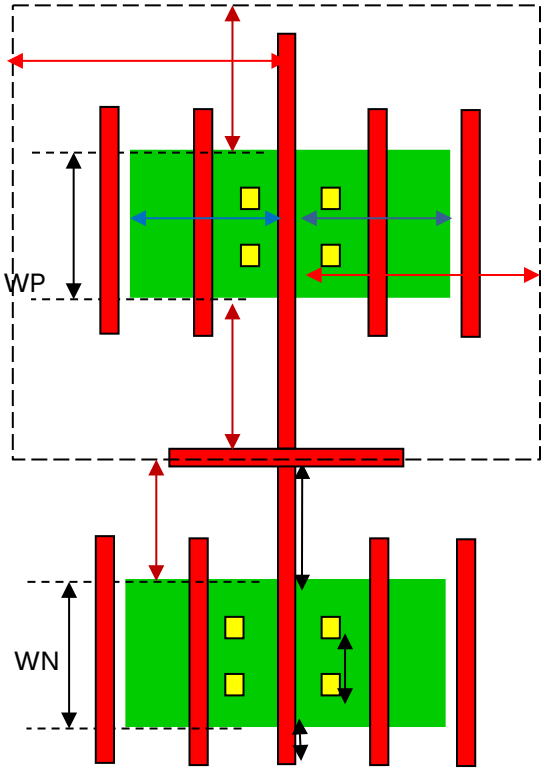
RO (99 stages) frequency



- Transistor level : random variations (SV) dominant for devices at critical dimensions
- Circuit level: random variations averaged, and systematic variations (LLE) revealed
- LLE methodology: characterization, compact modeling, post-layout extraction tool

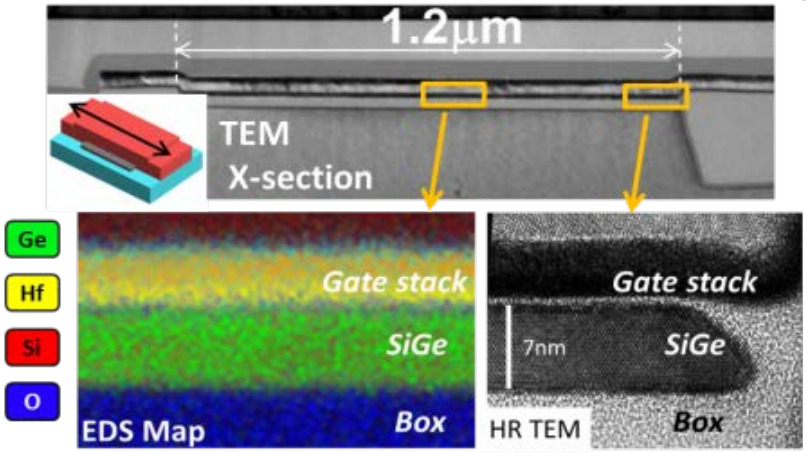
LOCAL SYSTEMATIC VARIATIONS (LLE)

Layout effect	Root cause	Critical distance	Electrical Parameters	Instance Layout par.
Well Proximity (WPE)	Deep Well implants	>1um	Vt, Mu, Kb	3
LOD/STI	STI Stress S/D SiGe (P) **SiGe channel (N)**	1um	Vt, Mu	> ~6
Gate Spacing Nb of Fingers	CESL/DSL Stressor	~1 um	Vt, Mu	>~6
S/D Contacts Nb & Position	CESL/DSL Stressor	1um	Vt, Mu	>~4
Distance to Stress Liner	DSL	1um	Vt, Mu	>~4
Active corner	Litho & Etch rounding	Local	Weff	~4
Gate corner or endcap	Litho & Etch rounding	Local	Leff	~4

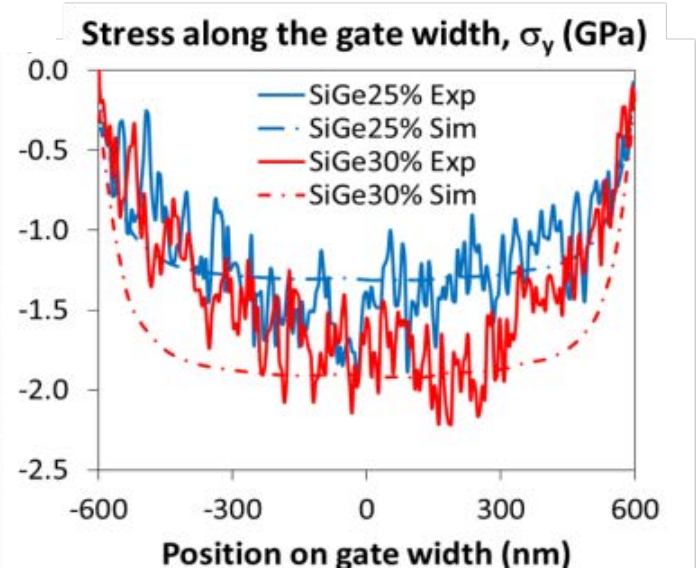


- LLE are technology dependent
- For each W/L instance, a bunch of layout dependent effects interplay
- Risk of inaccurate design reduced with Layout regularity and LLE model accuracy

LLE STUDY CASE (UTBB FDSOI SI-GE CHANNEL)



[B.De Salvo *et al.*, IEDM 2014]

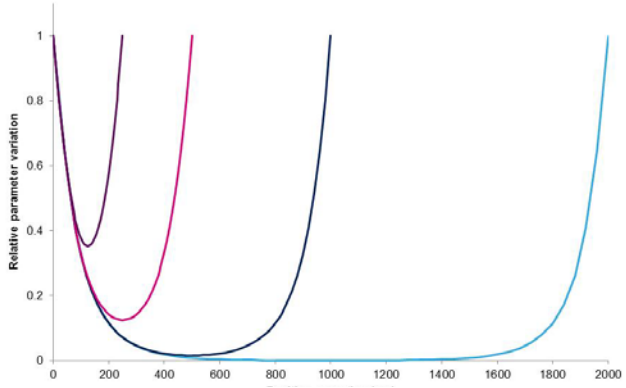


- Ge induces compressive strain in SOI film
- Strain tends to relax at the edges of the film

LLE STUDY CASE (UTBB FDSOI SI-GE CHANNEL)

$$P(x, L_{act}) = P_{full\ strain} + \Delta P \times g(x, L_{act})$$

$$\Delta P = P_{edge} - P_{full\ strain}$$



$g(x, L_{act})$ for $\lambda = 120nm$ and $\alpha = 3$

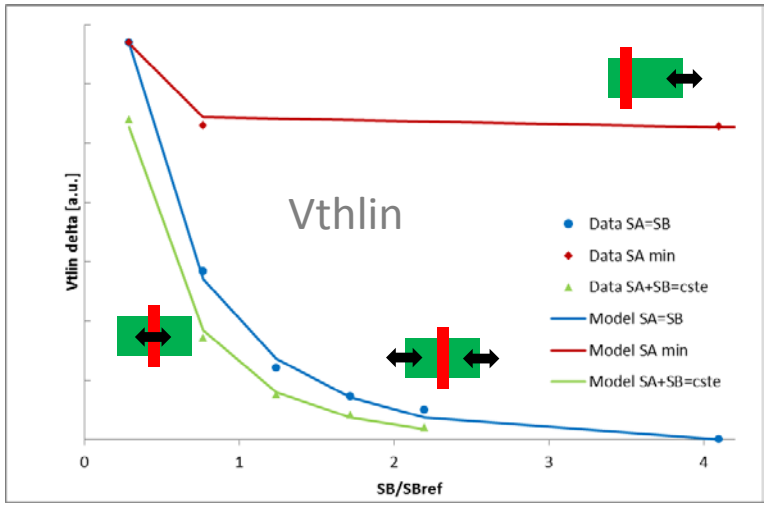
$$g(x, L_{act}) = 1 - \left[\frac{2}{(1 - e^{-x/\lambda})^{-\alpha} + (1 - e^{(x-L_{act})/\lambda})^{-\alpha}}\right]^{1/\alpha}$$

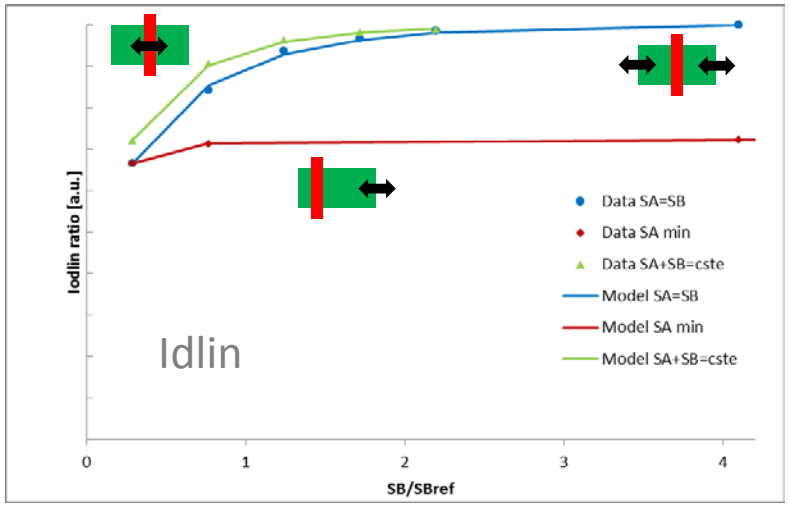
λ and α are model parameters

[T.Poiroux & al., MOSAK 2015 Q1]

- Compact model formulation for Electrical Parameters P inspired from Stress profile
- Impacts on Vfb, DIBL, Mobility, and Velocity saturation accounted for in UTSOI2 model

LLE STUDY CASE (UTBB FDSOI SI-GE CHANNEL)



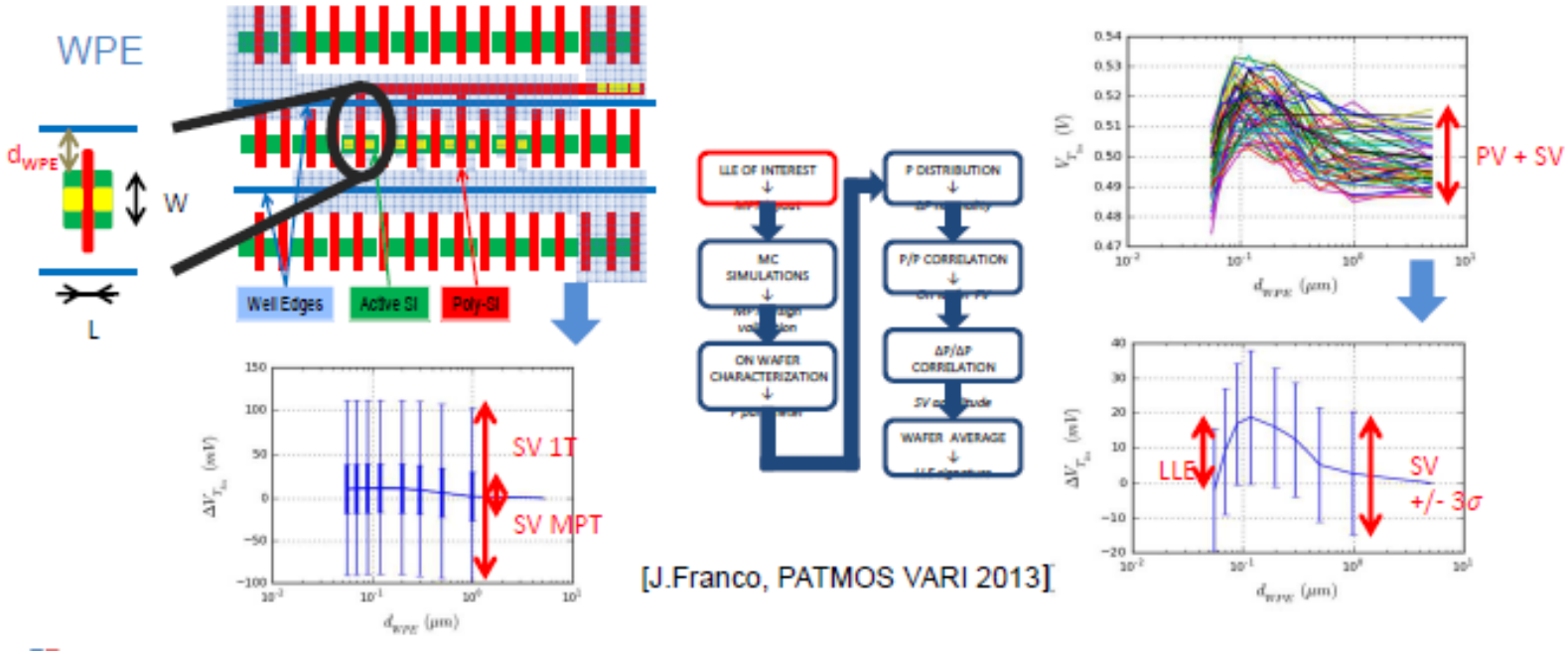


$$P(SA,SB) = P(SA_{ref},SB_{ref}) + \Delta P\left(g(SA,SB) - g(SA_{ref},SB_{ref})\right)$$

[T.Poiroux & al., MOSAK 2015 Q1]

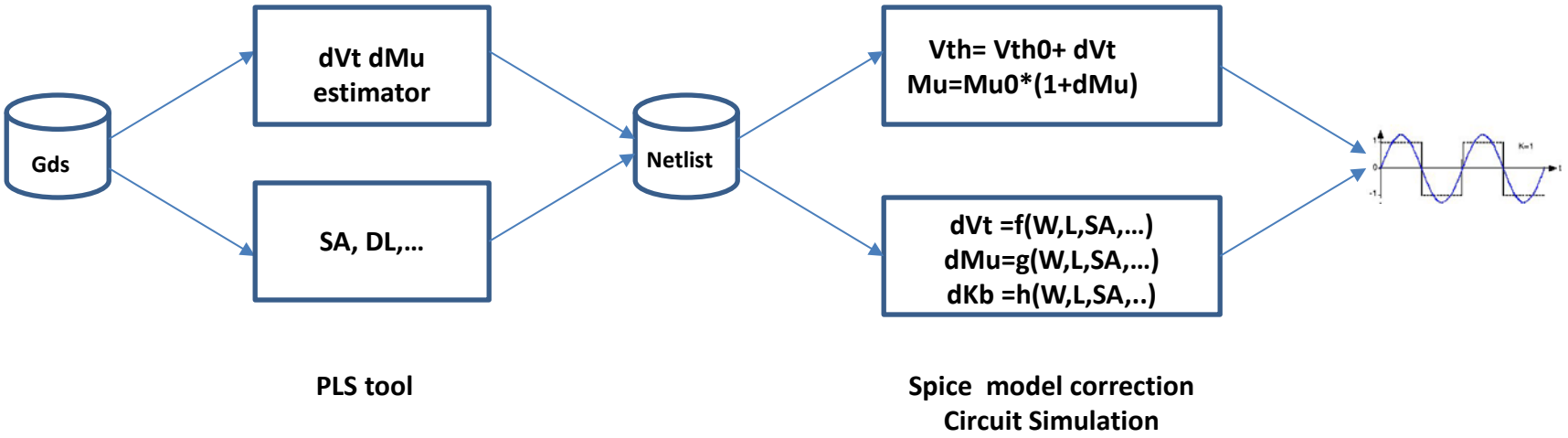
- SA/SB effect model validation

LLE CHARACTERIZATION METHODOLOGY



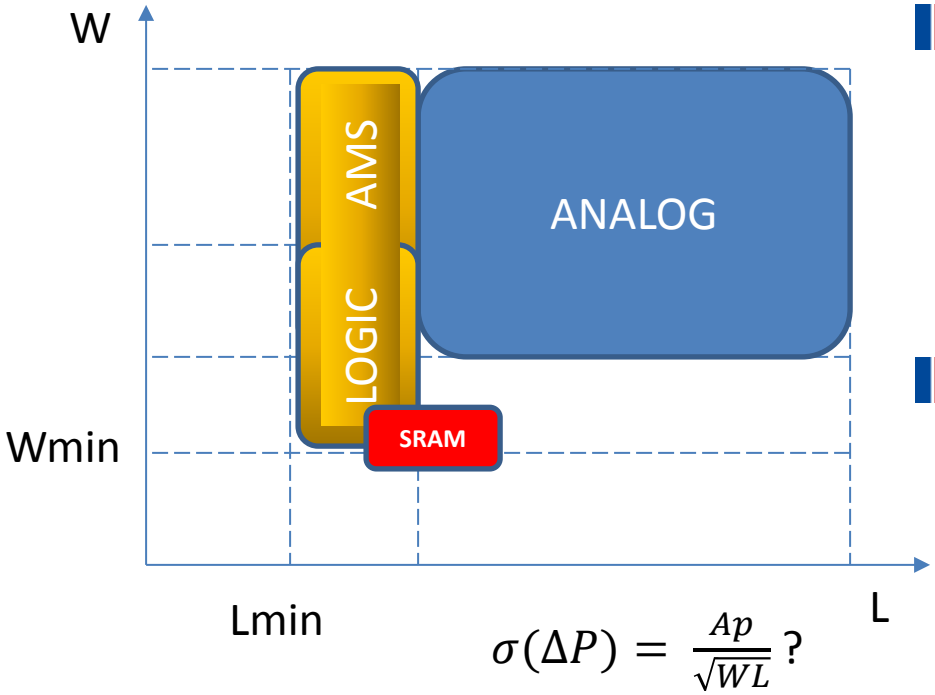
- Characterization methodology revisited for transistor LLE
- Test structure, data processing in presence of PV and SV, LLE signature

LLE DESIGN FLOW



- LLE simulation flow: implementation shared bw Post-Layout extraction and Compact Spice modeling

LOCAL STATISTICAL VARIATIONS (SV)

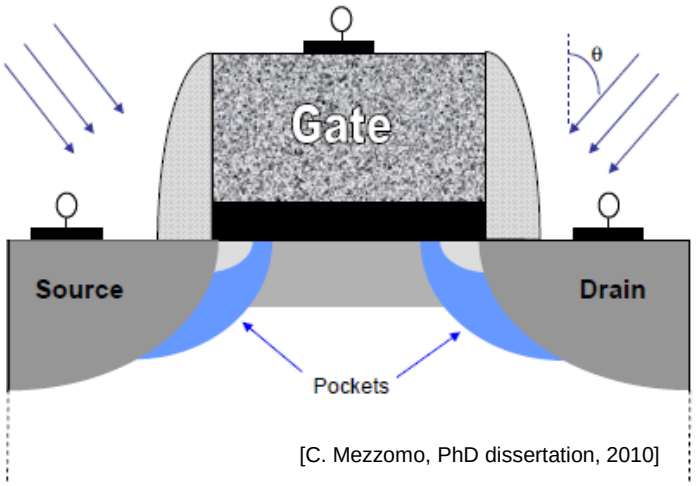


$$\sigma(\Delta P) = \frac{Ap}{\sqrt{WL}} \; ?$$

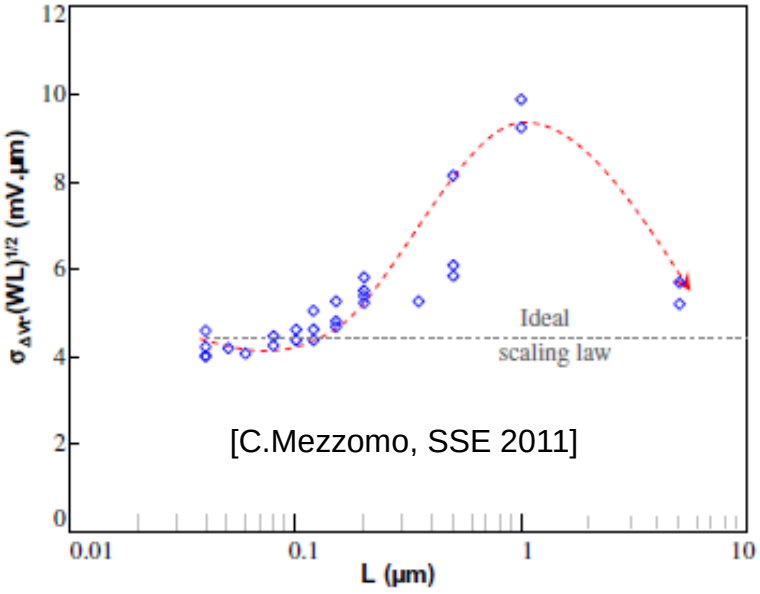
- SV scaling driven by SRAM
  - VDDmin
  - Minimization of SV sources and Device sensitivity to SV
- SV impacts AMS-Analog
  - Current Mirrors accuracy
  - Need to investigate SV scaling on W and L

- Pelgrom model is nice metric, but does scaling apply throughout Design Space?
- Which sources are present and which electrical parameters are impacted?

LOCAL STATISTICAL VARIATIONS: BULK PLANAR CMOS



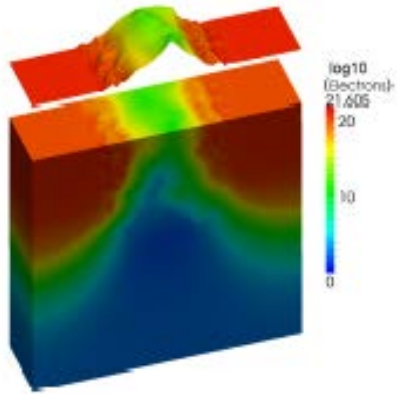
[C. Mezzomo, PhD dissertation, 2010]

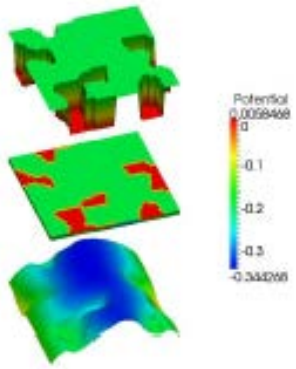


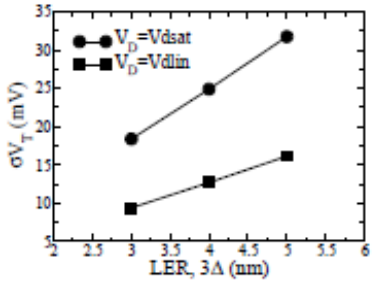
[C.Mezzomo, SSE 2011]

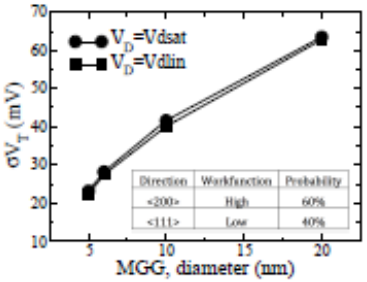
- 45nm devices exhibit AVT degradation for large L
- Model improved for AMS circuit design assuming Channel doping gradient

LOCAL STATISTICAL VARIATIONS: BULK PLANAR CMOS



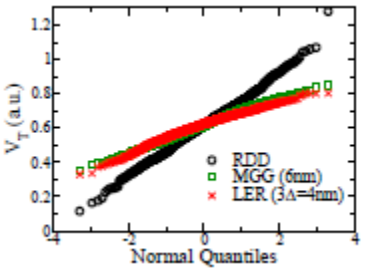


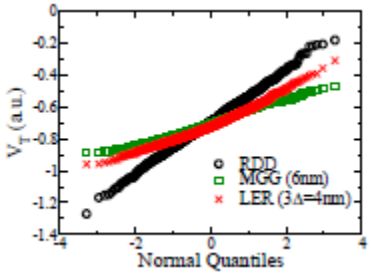




σV_T [mV]	n-MOSFET		p-MOSFET	
	V_{Dsat}	V_{Dlin}	V_{Dsat}	V_{Dlin}
RDD	49.8	44.4	54.4	42.3
LER (3Δ=4nm)	24.9	12.7	33.3	12.8
MGG (6nm)	28.2	27.4	25.3	24.7
Combined	63.2	52.7	68.7	52.1
Measurement	63.4	55.5	69.5	54.0

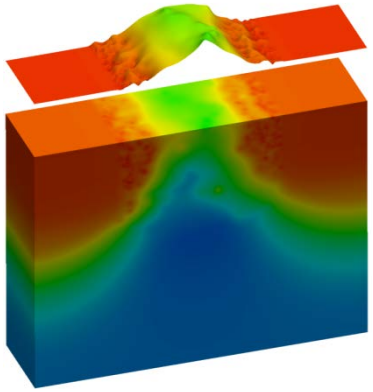
[X.Wang &al, Univ. Glasgow, EDL 2011]

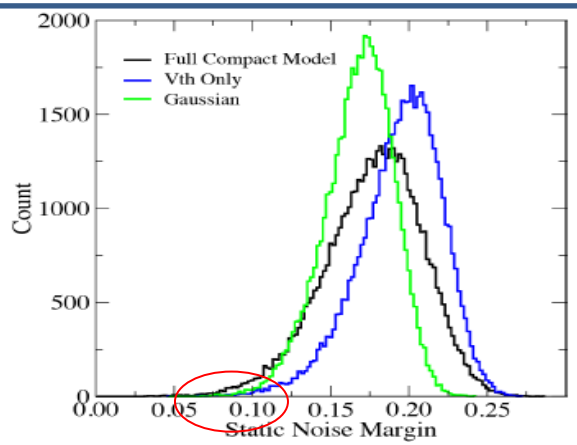


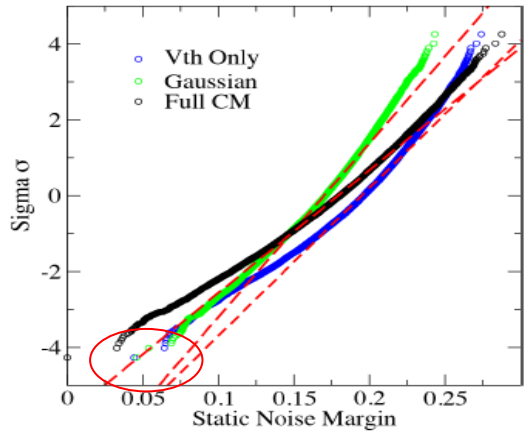


- SV sources well identified and contributions quantified (RDD dominant)
- SV models validated for 32nm devices (ENIAC Modern project support)

LOCAL STATISTICAL VARIATIONS: SRAM CASE



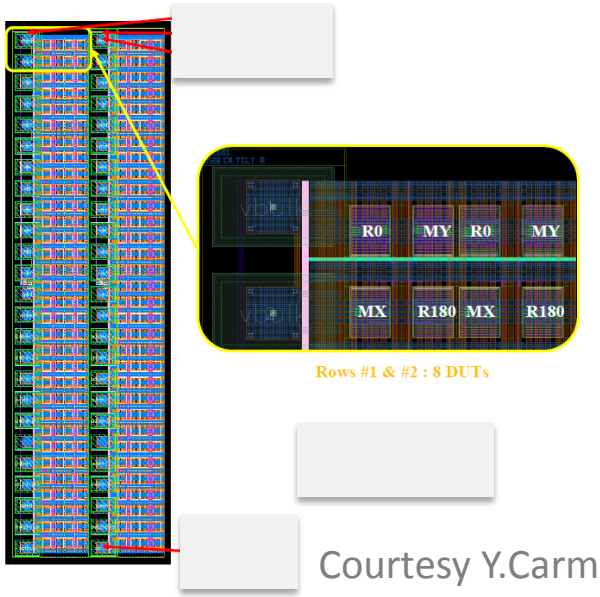




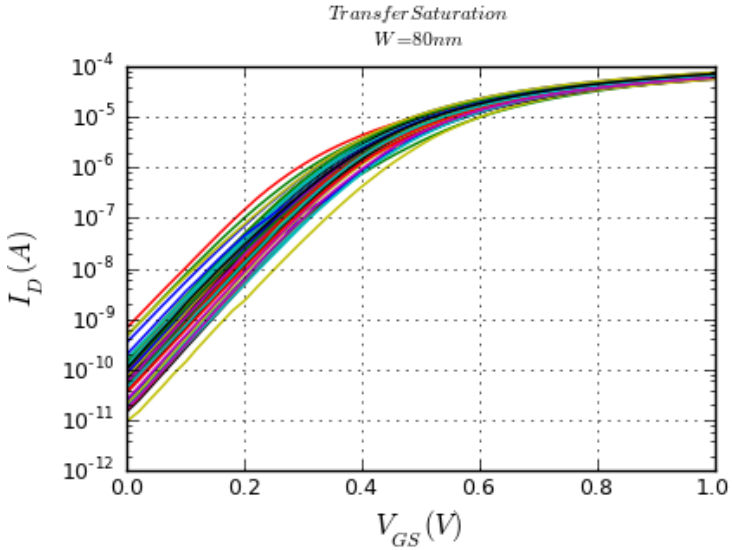
Monte-Carlo TCAD Device to SRAM circuit simulation chain [P.Asenov, PATMOS VARI 2011]

- Importance of accurate SV models has been demonstrated
- In particular, assumption of Vth-only and Gaussian-only PDF distribution may fail
- Full statistical compact models for accurate estimates of SRAM SNM

LOCAL STATISTICAL VARIATIONS: CHARACTERIZATION



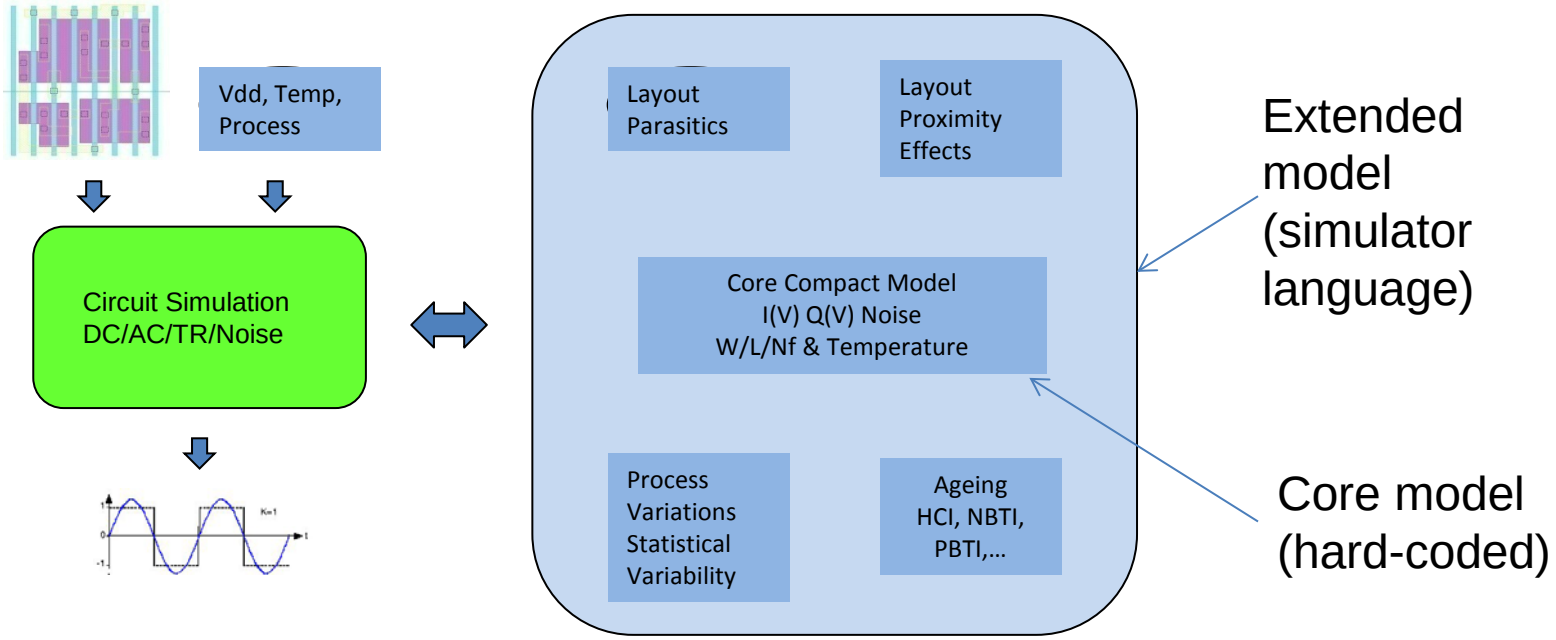
Courtesy Y.Carminati



Courtesy J.Franco

- Characterization methodology revisited
- Transistor pairs suited for standard mismatch figures characterization
- Addressable transistor arrays suited for statistical I(V) characterization (Vth, DIBL, SS, Idsat, Ioff,…) and statistical compact Spice model extraction

CIRCUIT SIMULATION REQUIREMENTS



- Accurate core models vs Bias, Geometry, Temperature
- Accurate model extensions for predictivity of PV, SV, LLE, and Ageing impact
- Efficient Circuit simulation methods and integrated design flow

CONCLUSION

- Variability has multiple contributions of different nature from technology and device.
- Those effects must be addressed concurently by dedicated developments in Technology, Characterization, Modeling, CAD tools, and Circuit design.
- Effective collaboration between those players is must-have to enable emergence of high volume high yield IC products in time with respect to market needs.
- Comprehensive understanding of variability at all-levels, variability reduction techniques, model accuracy, predictivity of statistical simulation tools, and design flow efficiency, are key.

REFERENCES

[1] B. De Salvo *et al*., "A mobility enhancement strategy for sub-14nm power-efficient FDSOI technologies", IEDM 2014

[2] T. Poiroux *et al*., "UTSOI2: A Complete Physical Compact Model for UTBB and Independent Double Gate MOSFETs", IEDM 2013

[3] G.Castaneda *et al*., "Test Structures for Interdie Variations Monitoring in Presence of Statistical Random Variability ", ICMTS 2012

[4] J.Franco *et al.,* "Characterization Methodology for MOSFET Local Systematic Variability in Presence of Statistical Variability ", JOLPE Journal, 2014, Vol10 no1

[5] P.Asenov *et al.,* "Introducing Statistical Variability into SRAM SNM Simulations – a Comprehensive Study ", VARI workshop, 2011

[6] C.Mezzomo *et al.,* "Modeling local electrical fluctuations in 45 nm heavily pocket-implanted bulk MOSFET", SSE Journal, 2010

[7] T. Poiroux *et al.,* "New version of Leti-UTSOI2 featuring further improved predictability, and a new stress model for FDSOI technology", MOSAK Workshop, March 2015

[8] F.Cacho *et al.,* " Simulation of pattern effect induced by millisecond annealing used in advanced metal-oxide-semiconductor technologies ". Journal of Applied Physics, 2010

[9] X.Wang *et al.,* " Simulation Study of Dominant Statistical Variability Sources in 32-nm High-κ/Metal Gate CMOS " , IEEE EDL, May 2012

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Jürgen Lorenz, Fraunhofer IISB

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OVERVIEW OF THE SUPERTHEME PROJECT

Conference Sponsors:

JOANNEUM RESEARCH

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OUTLINE

1. Introduction
2. Background pillars: Process and device
3. Consortium and project data
4. Project structure
5. Methodology used
6. Example: 23.5 nm transistor
7. Conclusion

INTRODUCTION: VARIATIONS

- Many variations have their source at equipment level

  ⇒ Equipment and process simulation core parts of the project

- Examples for variations at equipment level:
  - Lithography: Defocus; dose variations; (mis-)alignment, …
  - Etching/deposition: Inhomogeneities of gas flow, temperature; drifts, chamber coating; source characteristics, …
  - Ion implantation: Variations of angle(s) and dose; statistics, …
  - Annealing: Temperature variations in space/time, …
- Additional pattern-induced variations

INTRODUCTION: VARIATIONS

- Challenge: Insufficient quantitative data on variations in equipment
  - Data can only be gathered by / in cooperation with equipment companies
  - Use data from literature plus experiment on selected tools
- Combination with treatment of statistical variations necessary

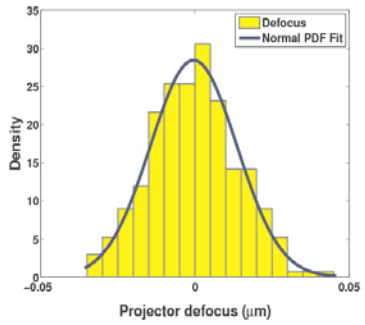
  $\Rightarrow$ Challenge: Predictive simulation chain equipment/process/ device/circuit for variations needed

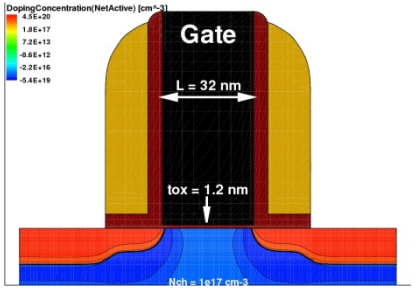
INTRODUCTION: SUPERTHEME OBJECTIVES

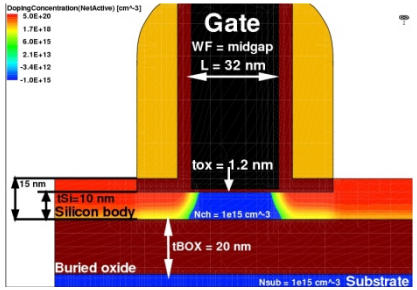
- Extend / integrate SW of partners
  + required third-party SW
- Data reduction / hierarchical simulation needed – from discretization of equipment to compact models
- Collect data for variability at process level
- Challenge: Correlations of variations must be included
- Exploit background of partners esp. for variabiliy simulation

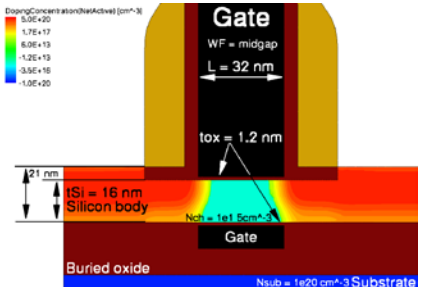
BACKGROUND PILLARS: PROCESS – IISB

Impact of lithography focus variations on transistor performance









Focus variations

⇩

CD variations

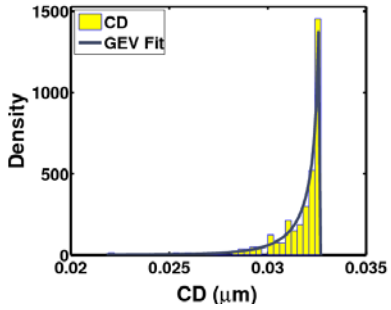
Bulk

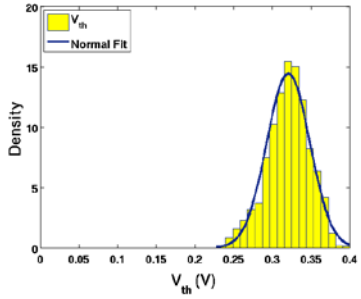
Device architecture

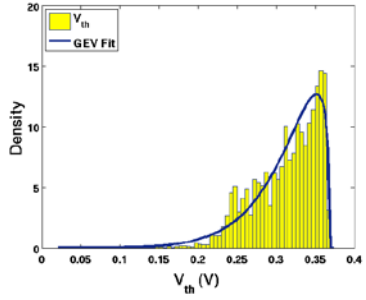
SG FD SOI

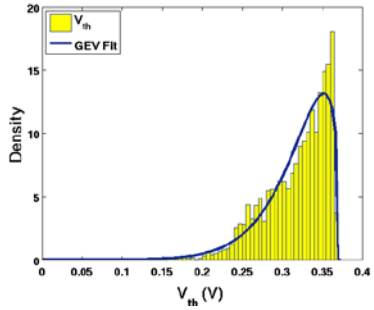
DG FD SOI

acts as filter for CD variations and leads to variations e.g. of V_{th}





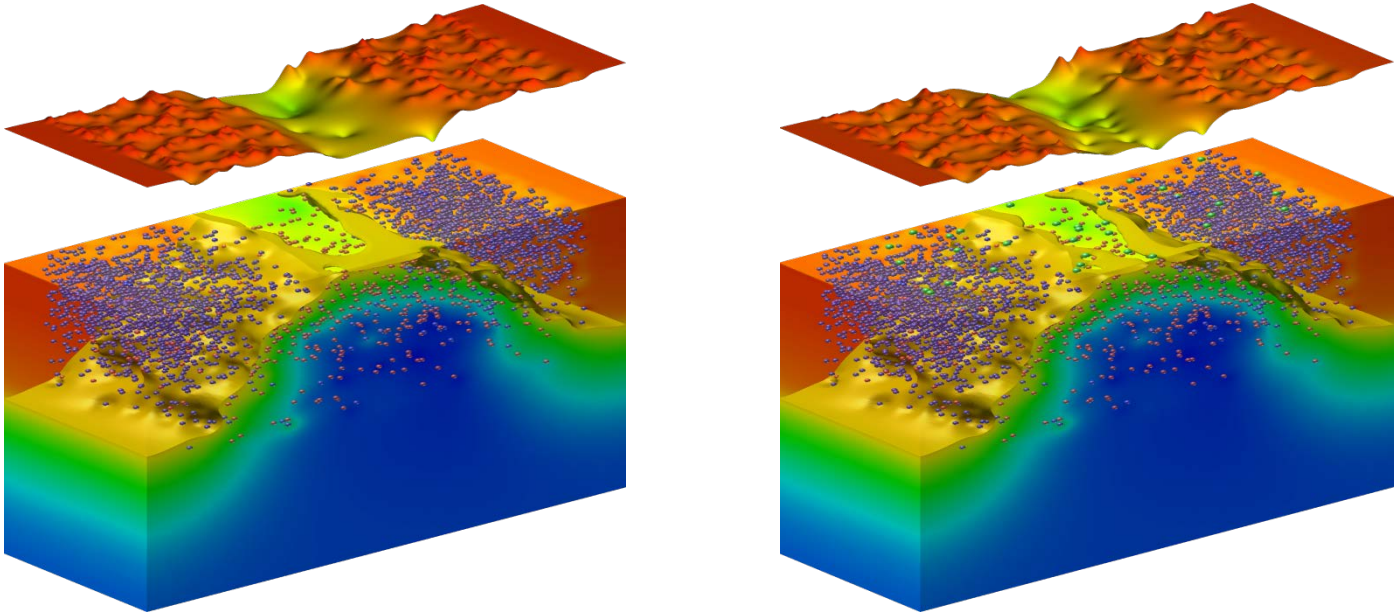




J. Lorenz et al., *Proc. 2009 Intl. Symposium on VLSI Technology, Systems and Applications*, Hsinchu, Taiwan, 2009, pp. 17-18.

BACKGROUND PILLARS: DEVICE – GU/GSS

Device simulation SW for the study of the impact of variations caused by the granularity of matter, esp. RDF, LER, MGG



Left: Simulation of a 45 nm technology transistor in the presence of discrete dopant, line edge roughness and polysilicon gate granularity. Right: Simulation of the same transistor subject to degradation. By chance two holes are trapped in the vicinity of the percolation path. From GU / GSS

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CONSORTIUM AND PROJECT DATA

- Project partners
  - Semiconductor industry: ams
  - Equipment companies: ASML, HQD, IBS, LASSE
  - SW house: GSS
  - Research institutes: Fraunhofer IISB (coord.), IIS/EAS
  - Universities: Univ. Glasgow, TU Wien
- Project period: 10/2012 – 12/2015
- EC funding: 3.3 M€ from FP7 ICT Call 8
  - Action line 3.1 “Very advanced nanoelectronic design, engineering, technology and manufacturability“
- See www.supertheme.eu

SUPERTHEME PROJECT STRUCTURE

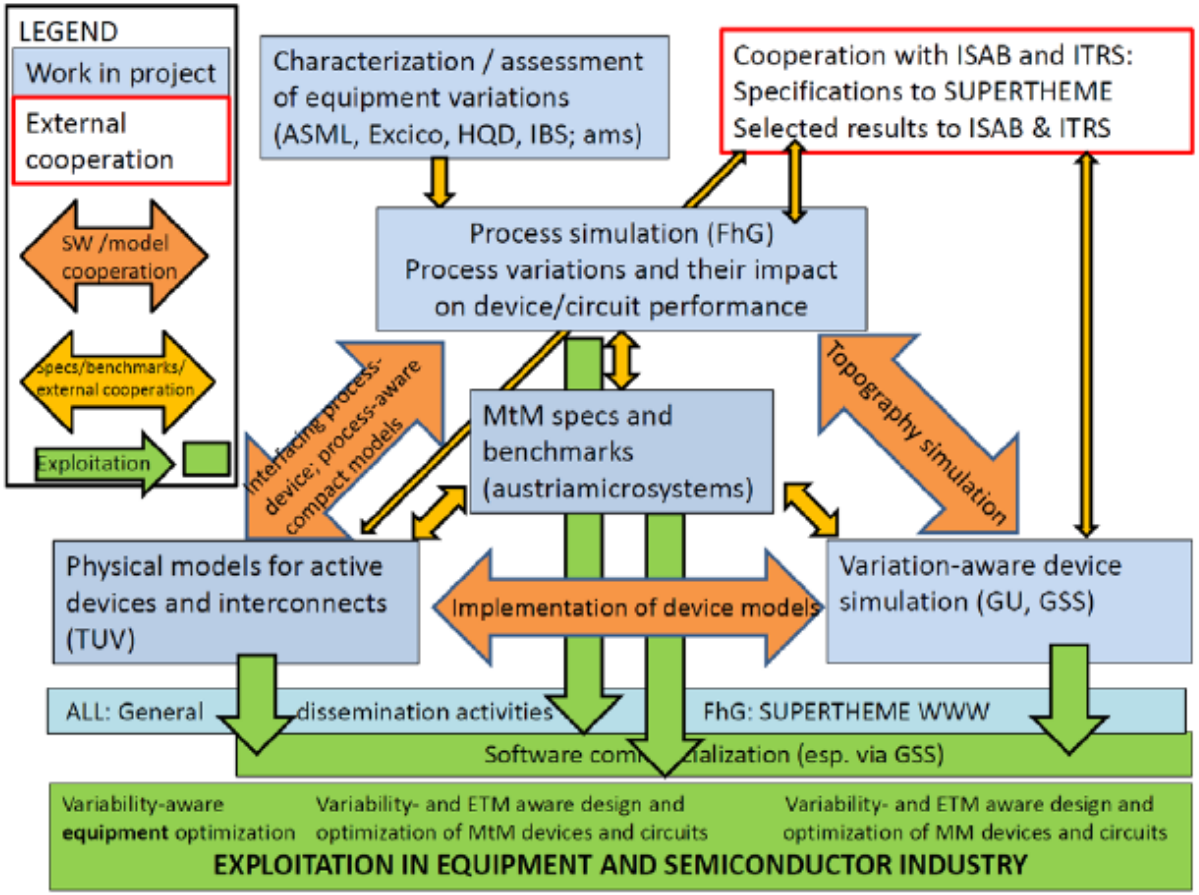
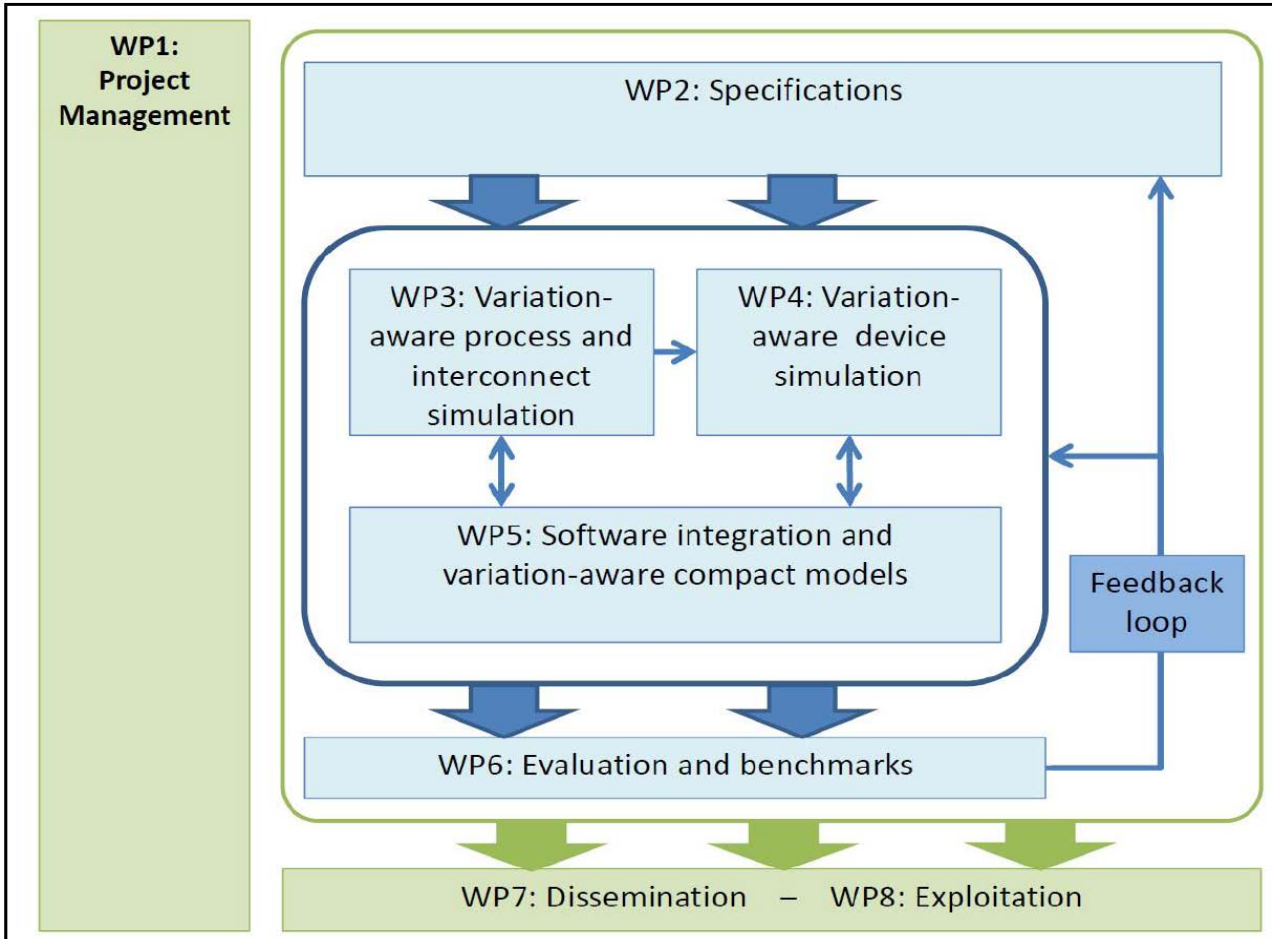


Fig. 2: Focal activities of SUPERTHEME partners and mutual interactions

(From SUPERTHEME proposal and DoW)

SUPERTHEME PROJECT STRUCTURE

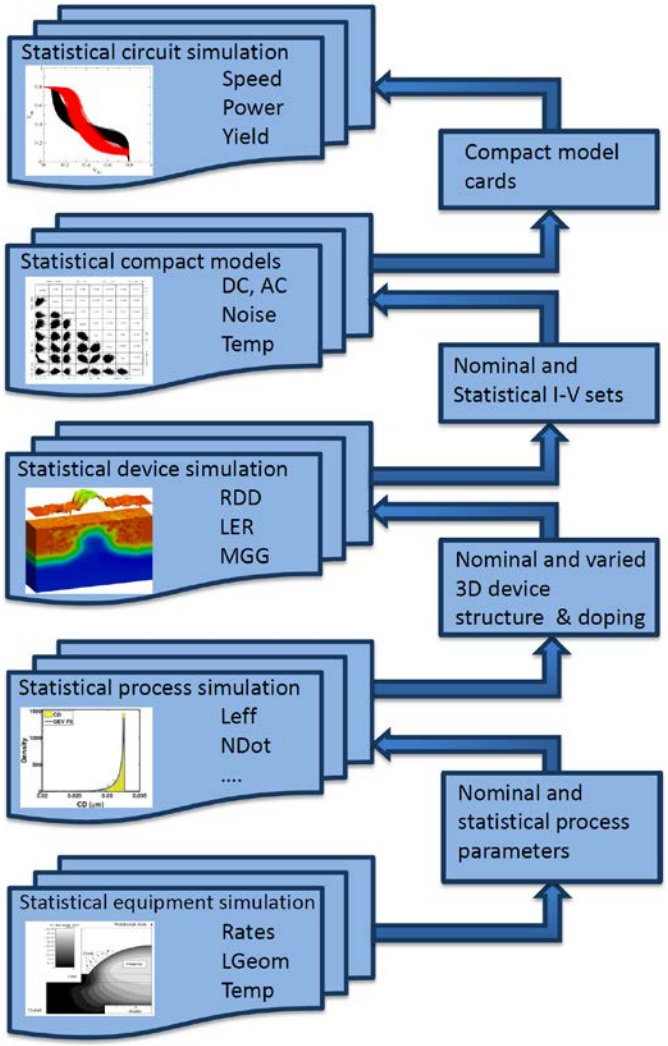


(From SUPERTHEME proposal and DoW)

METHODOLOGY USED

Simulation levels and tools used

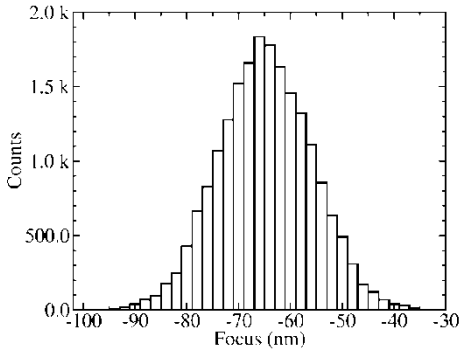
- Equipment simulation: Q-VT (Quantemol), CFD-ACE (ESI Group)
- Process simulation:
  - Lithography: Dr.LiTHO (Fraunhofer)
  - Etching/deposition: ANETCH / DEP3D (Fraunhofer)
  - Annealing: Sentaurus Process (SNPS)
- Device simulation: GARAND (GSS)
- (Statistical compact model extraction: MYSTIC (GSS))
- (Circuit simulation: RandomSpice (GSS))

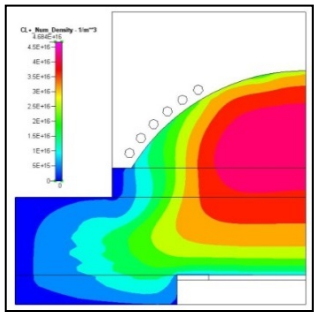


From J. Lorenz et al, SISPAD 2014

METHODOLOGY USED

- Assumed variations at equipment level – probability density p(P) of some varying parameter P (e.g. litho defocus/dose; position on wafer)





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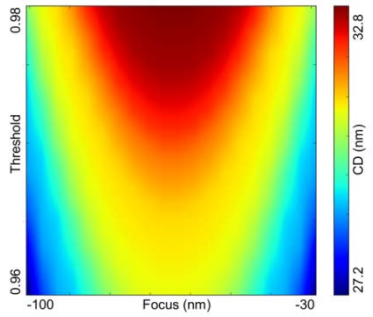
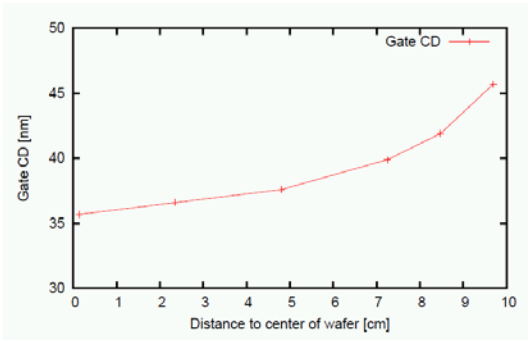
From J. Lorenz et al, SISPAD 2014

METHODOLOGY USED

- Integrated equipment and process simulation

  ⇨Variation of device geometries (and continuum doping) caused by process or equipment variations – e.g. *L(P)* and *W(P)*: ***Device Defining Data D3***

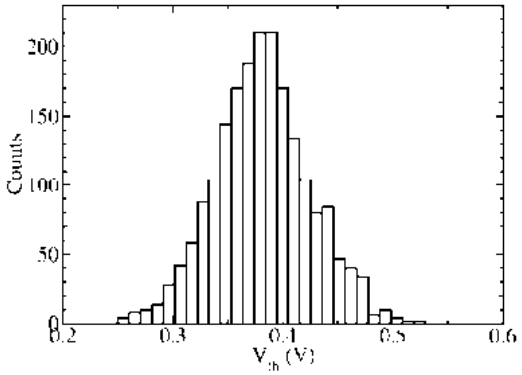




From J. Lorenz et al, SISPAD 2014

METHODOLOGY USED

- Stochastical device simulation based on geometries and doping of continuum devices (matrix of *L* and *W*), including RDF, MGG, LER
  - ⇨ Statistical probability densities g_s of electrical data for devices with identical geometry/continuum doping profiles



From J. Lorenz et al, SISPAD 2014

METHODOLOGY USED

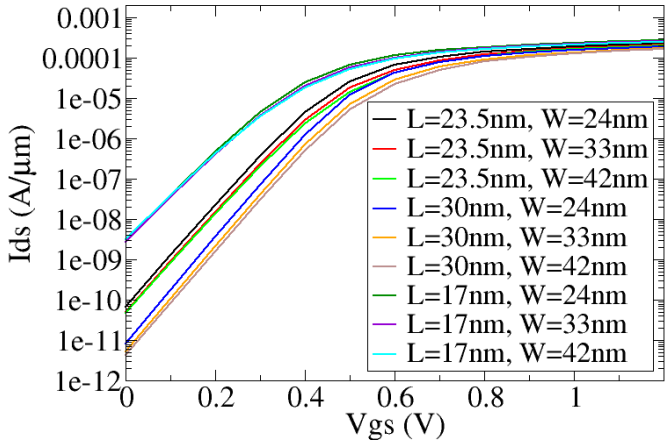
- Combination of equipment/process and device level by taking probability of geometry/continuum doping into account
- Extraction of hierarchical compact model

⇨ Statistical distribution h_s of electrical data for given p(P)

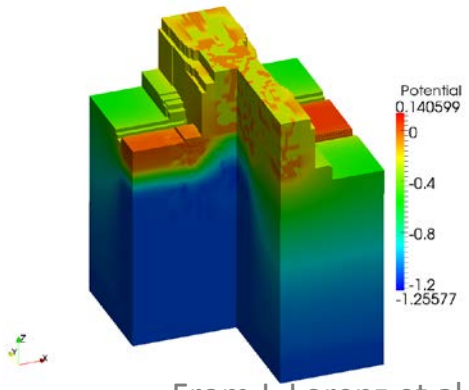
$$h_s = \int g_s(L(P),W(P))\, p(P)\, dP$$

EXAMPLE: 23.5 NM TRANSISTOR

- Continuum devices considered: Planar bulk NMOS transistors,
  - Mean values L =23.5nm, W =33nm
  - 5 x 5 matrix, L between 17nm and 30nm, W between 24nm and 42nm
- Example of results for continuum devices



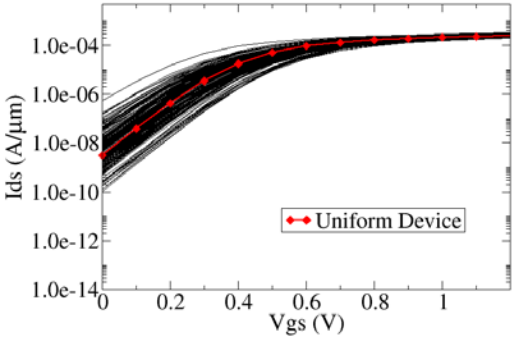
- Potential for nominal device with RDF, MGG and LER (simulated with GARAND)



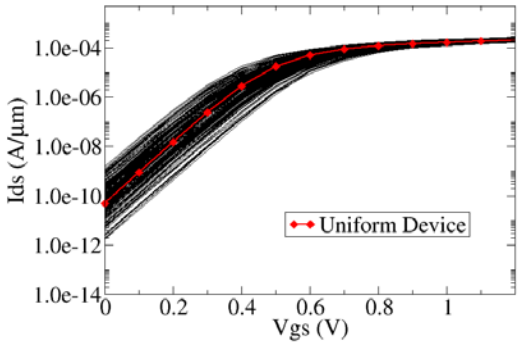
From J. Lorenz et al, SISPAD 2014

EXAMPLE: 23.5 NM TRANSISTOR

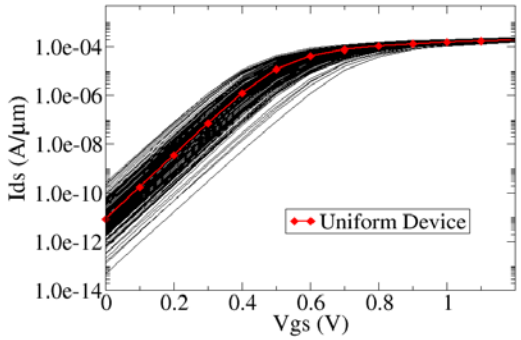
- Statistical device simulation including RDF, MGG and LER for matrix of 5 x 5 continuum devices
- Example: Output characteristics at V_D= 0,05V for devices with different L and W



min. L / max W
L= 17 nm, W= 42 nm



nominal device
L = 23.5nm, W = 33 nm

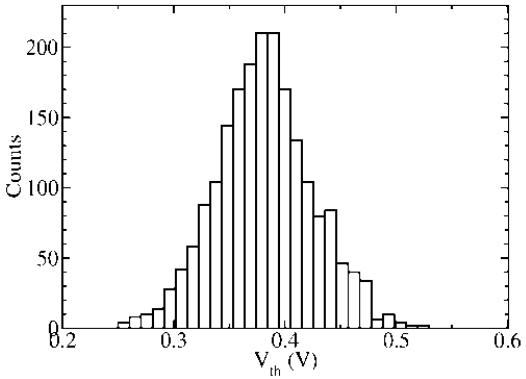


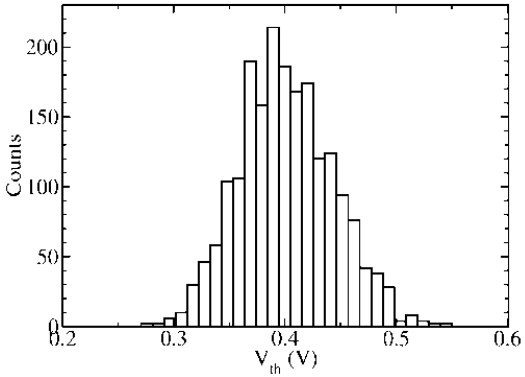
max. L / min. W
L = 30 nm, W = 24 nm

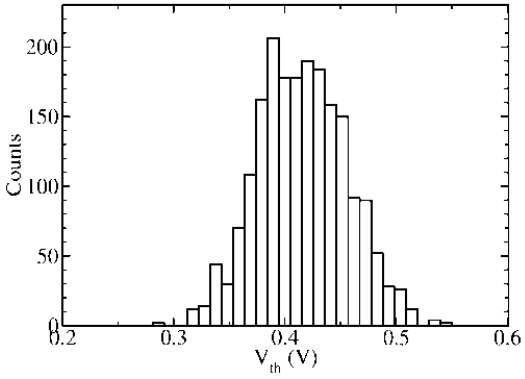
From J. Lorenz et al, SISPAD 2014

EXAMPLE: 23.5 NM TRANSISTOR

- Statistical device simulation including RDF, MGG and LER for matrix of 5 x 5 continuum devices
- Example: Probability densities for V_{th} at V_D = 0,05 V for devices with different L and W: Different minimum, mean and maximum values of V_{th} distribution







min. L / max W
L= 17 nm, W= 42 nm

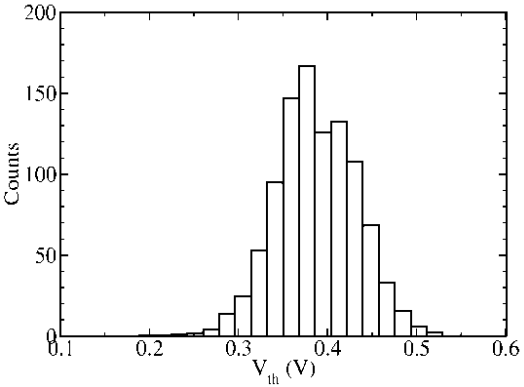
nominal device
L = 23.5nm, W = 33 nm

max. L / min. W
L = 30 nm, W = 24 nm

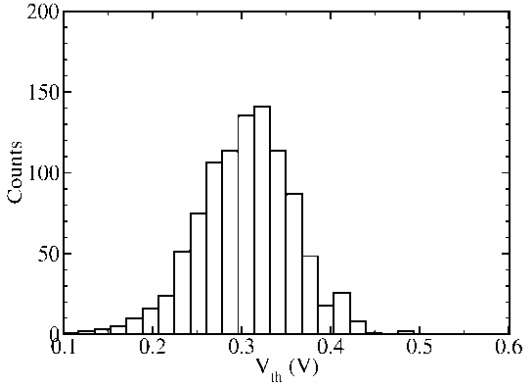
From J. Lorenz et al, SISPAD 2014

EXAMPLE: 23.5 NM TRANSISTOR

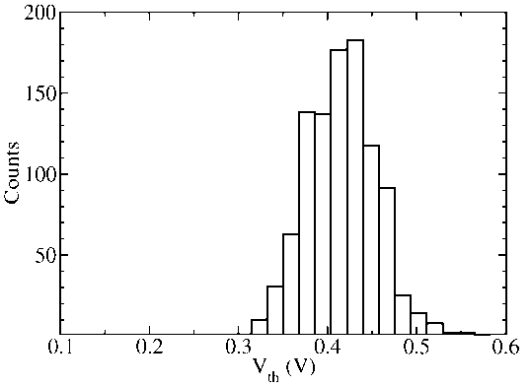
- Hierarchical compact model extracted
- Simulation of coupled influence from lithography (focus, dose), etching (equipment-induced bias variations), RDF, LER, MGG
- Example: V_{th} for average etch bias (5nm) and for different positions at the wafer
- PDF caused by litho variations, RDF, LER and MGG is strongly modified by etch bias variations across wafer



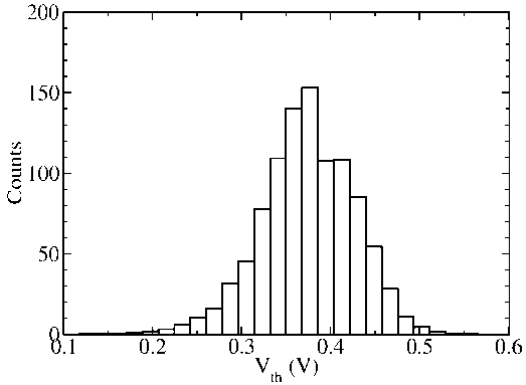
Etch bias 5 nm



Etch bias 10 nm



Etch bias 0 nm



Average across wafer

CONCLUSIONS

- SUPERTHEME has demonstrated:
  - Feasibility of hierachical variability simulation equipment/process/device/circuit
  - Important impacts on device and circuits
  - Correlations can and must be included
  - Gaussian sources of variability frequently lead to highly non-Gaussian variations at device or circuit level
- Very promising prospects for application and extension of work

ACKNOWLEDGEMENTS

- Contribution of all colleagues at partners highly appreciated
- Valuable inputs from EC review team and from SUPERTHEME ISAB
- Funding from EC highly appreciated

This project has received funding from the European Union's Seventh Framework Programme for research, technological development and demonstration under grant agreement no 318458.

Alexander Shluger, University College London, UK

ESSCIRC ESSDERC 2015

DEFECTS RESPONSIBLE FOR BTI IN CMOS DEVICES: MORDRED PERSPECTIVE

Atomistic picture

Conference Sponsors:

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NXP

TU Graz Graz University of Technology

EC FP7 PROJECT MORDRED

Modelling of the reliability and degradation of next generation nanoelectronic devices

- Funded by EC within FP7
- Duration 04/2011 – 03/2015
- Overall funding 4.5 M€
- Consortium of
  - 3 companies
  - 5 research institutes/universities

This project has received funding from the European Union's Seventh Framework Programme for research, technological development and demonstration under grant agreement no 318458.

MORDRED

PARTNERS


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Aalto University


KATHOLIEKE UNIVERSITEIT
LEUVEN


UCL


University of Glasgow
VIA VERITAS VITA


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WIEN
TECHNISCHE
UNIVERSITÄT
WIEN


imec


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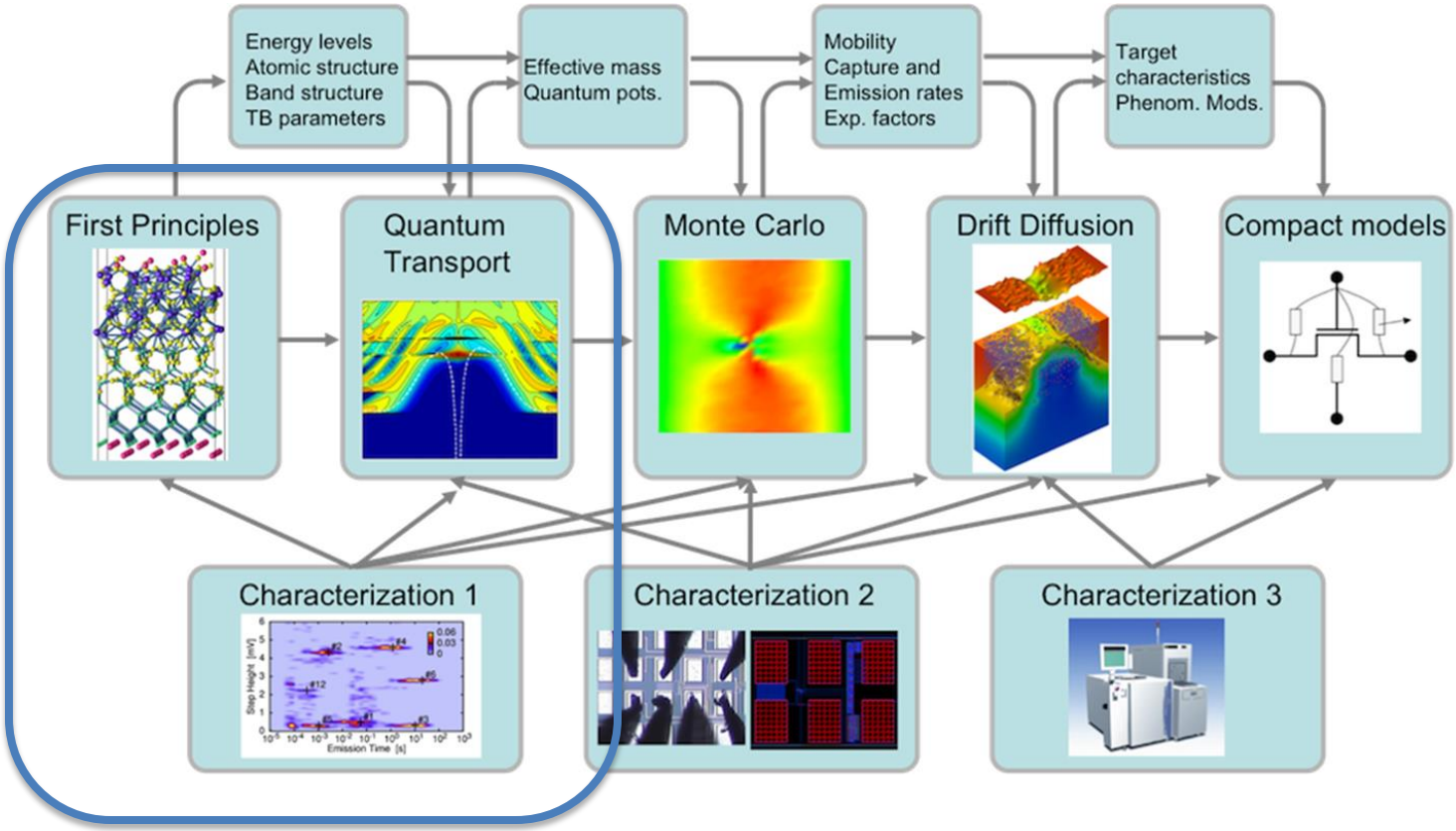
OUTLINE

1. Introduction
2. Carrier capture/emission by oxide defects
3. Computational models
4. Defect parameter extraction from experimental data
5. Establishing defect models
6. Defect reactions
7. Summary and Outlook

MORDRED Grand Design

ESSCIRC ESSDERC 2015

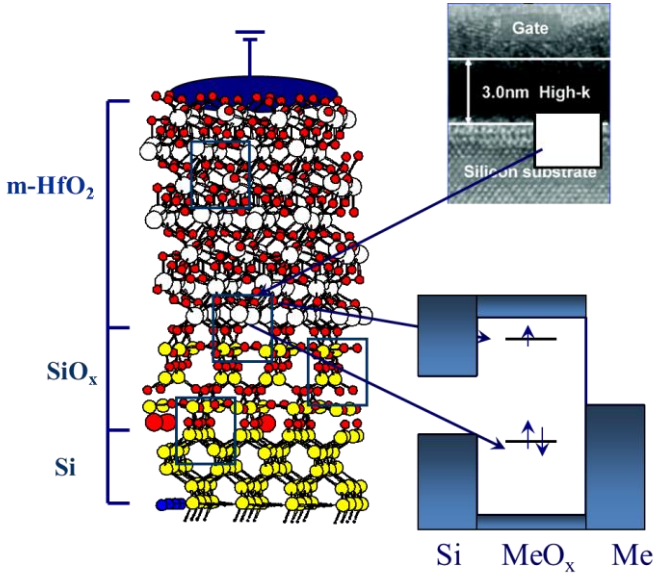


To develop multi-scale modelling technology, supported by comprehensive experimental characterization techniques, to study the degradation and reliability of next generation CMOS devices

MORDRED

Electronic devices are complex systems of *interfaces*

- Generic atomistic models for interfaces
- Relation between defects structure and interface morphology
- Electronic structure of the electron and hole traps



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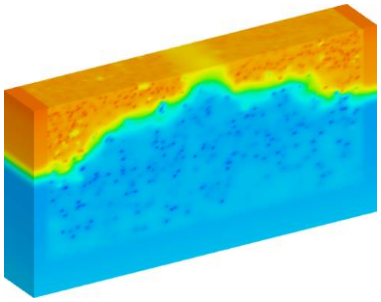
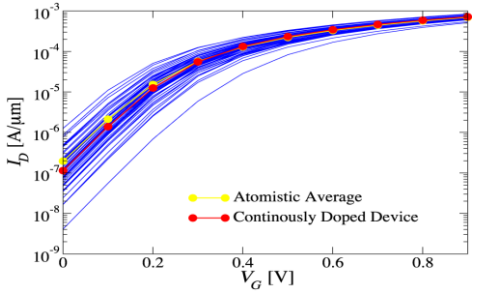
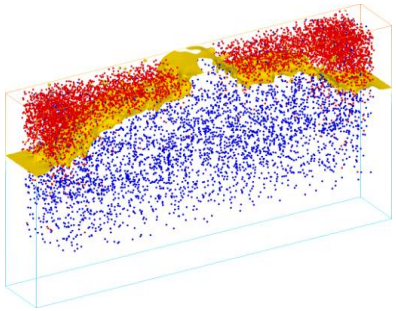
Goal: Linking atomistic and device modelling

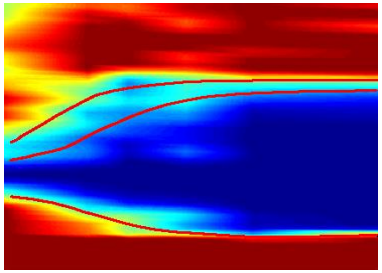




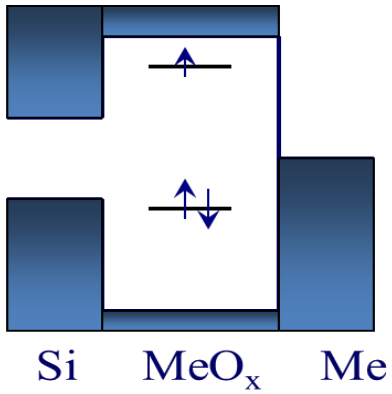


- Three dimensional
- Statistical
- Quantum corrections

Input from atomistic modeling



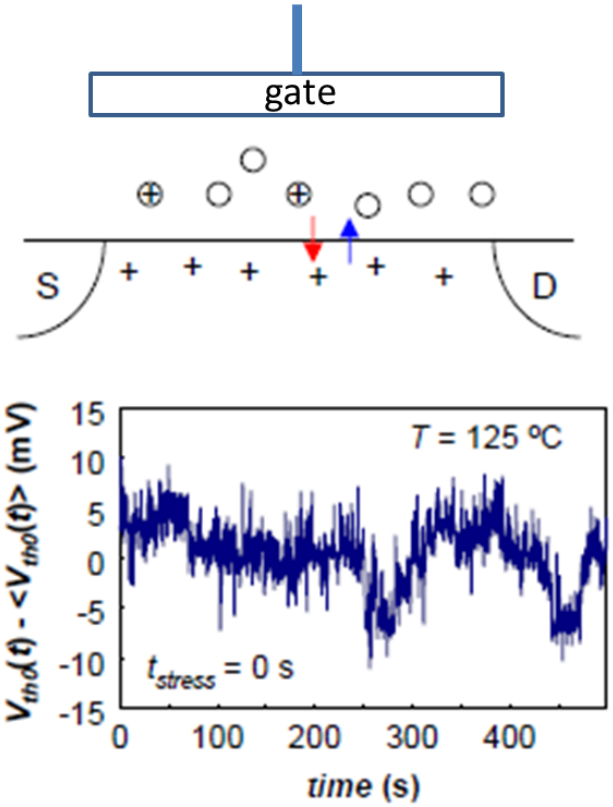
- Dielectric constant variations.
- Band gap variations.
- Interface states.
- Defect states in the dielectric.
- *e* scattering potentials
- Granularity models



Collaboration with GU and TU Wien

MORDRED

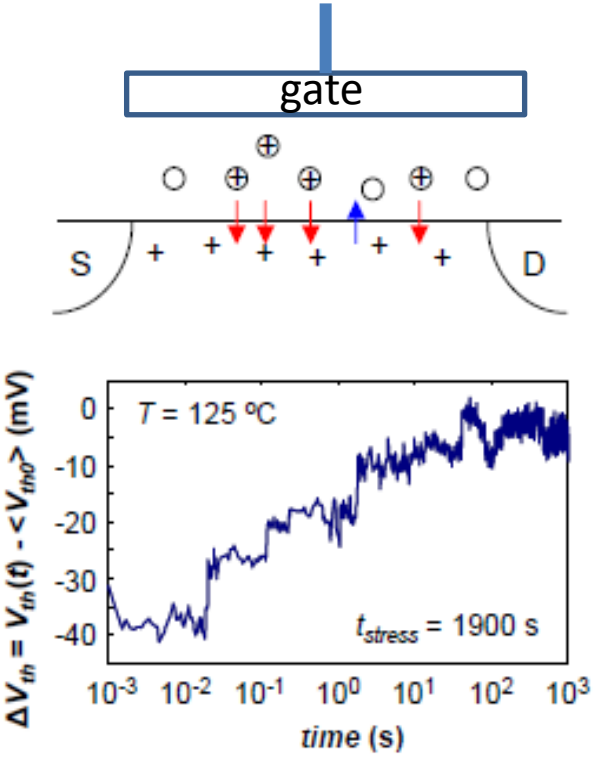
RANDOM TELEGRAPH NOISE



B. Kaczer et al. IRPS10

- At **constant bias** conditions, oxide defects are charged by channel carriers and subsequently discharged back into the channel
- A **wide range of time constants** is controlled by a nonradiative **multiphonon emission process**
- The system is in ***dynamic* equilibrium**, manifested by low-frequency noise or Random Telegraph Noise (RTN) in small devices

(NEGATIVE) BIAS TEMPERATURE INSTABILITY

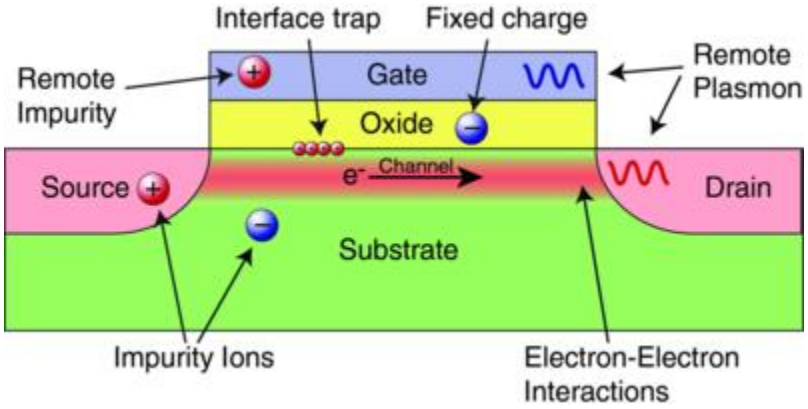


B. Kaczer et al. IRPS10

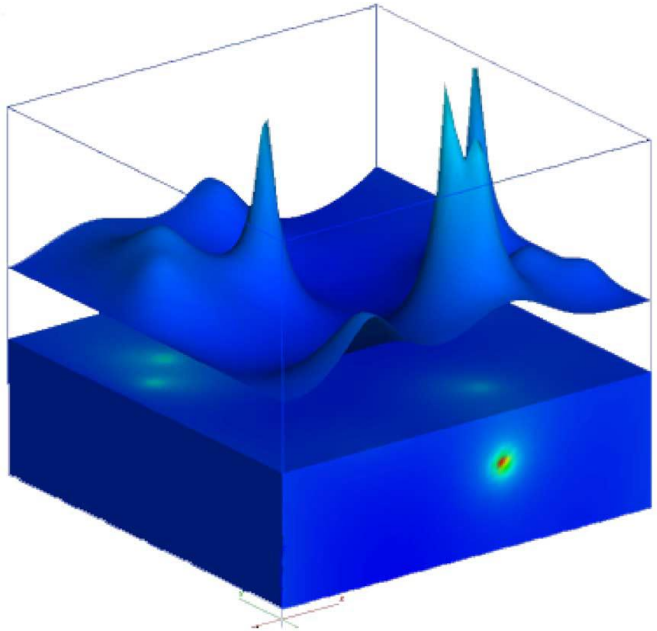
- Following the perturbation by NBTI stress, excess **charged oxide defects gradually discharge** and the system is returning to the dynamic equilibrium of (a), resulting in long NBTI transients

- NBTI in downscaled devices can be treated as a **stochastic ensemble of individual defects**, Poisson-distributed in number per device, with each defect described by its impact on the channel conduction characterized by its **capture and emission times**

PERCOLATION PATH



Carrier scattering centres in CMOS devices



Potential distribution in a 3-D volume with random discrete dopants. The carriers are scattered by Coulombic potential of the dopants.

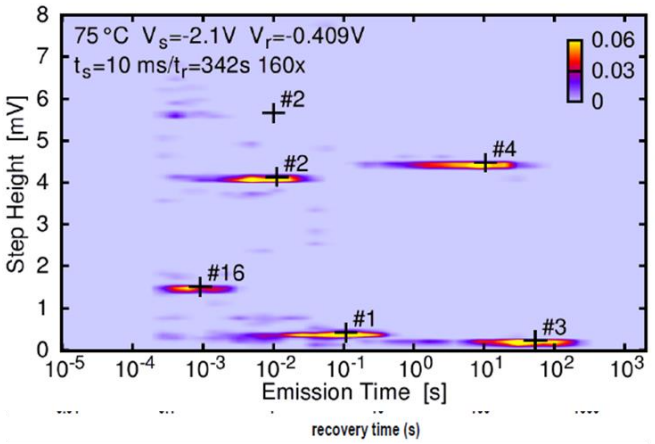
E. A. Towie et al. Semicond. Sci. Techn. 26, 055008 (2011)

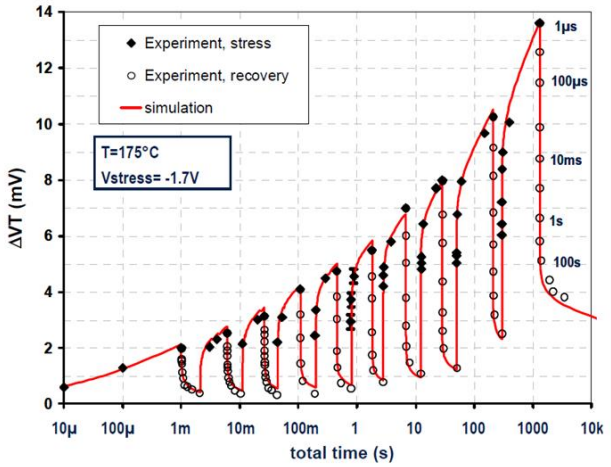
C. Alexander et al., Sol. St El. 49, 733 (2005)

TIME-DEPENDENT DEFECT SPECTROSCOPY

Negative Bias Temperature Instability

- Time dependent defect spectroscopy: Small area devices in which recovery after stress proceeds in discrete steps
- Each discrete step due to emission of **single** trapped charge carrier
- **Individual defects** characterized by step height





REVERSE-ENGINEERING DEFECT MODELS

- Model extraction
- Candidate selection
- Candidate evaluation
- Rate calculation

Defect elimination

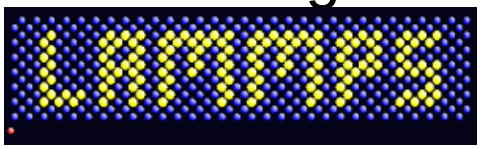
Computational details

ESSCIRC ESSDERC 2015

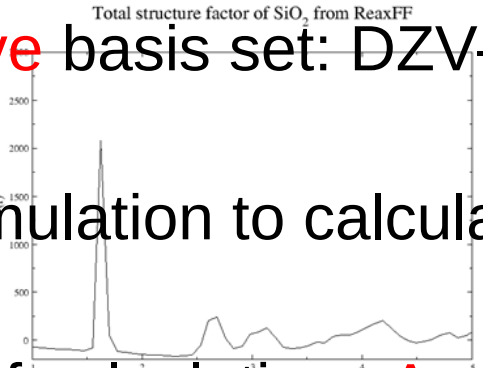
Calculations performed on > 300 models of amorphous silica with cells containing 216 atoms

Amorphous silica generated using empirical force-field (ReaxFF) and molecular dynamics to simulate heating and

$$E(q_1,\ldots,q_N)=\sum_i^N\left(E_{i0}+\chi_i^o q_i+\frac{1}{2}J_{ii}^o q_i^2\right)+\sum_{i<j}^N q_i q_j J_{ij}$$

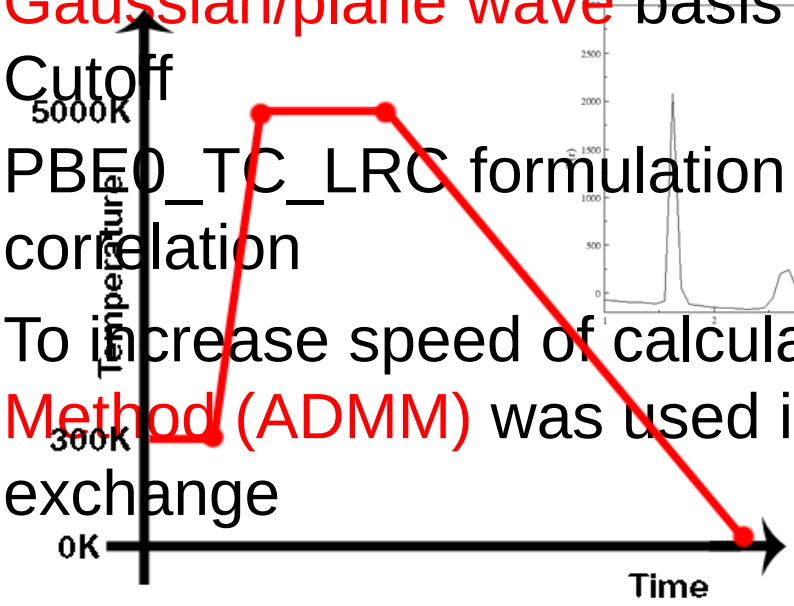


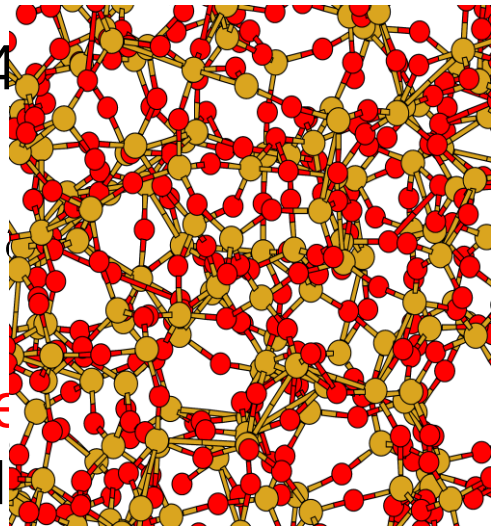
Gaussian/plane wave basis set: DZV-Basis, 4
Cutoff



PBE0_TC_LRC formulation to calculate exch
correlation

To increase speed of calculations Auxiliary De
Method (ADMM) was used in calculation of H
exchange





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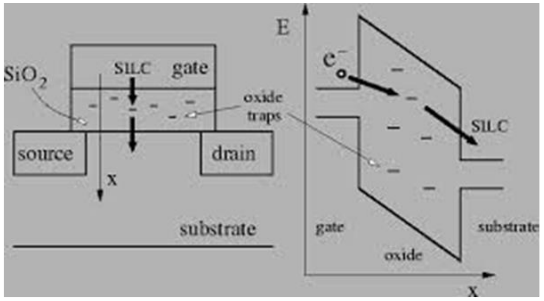
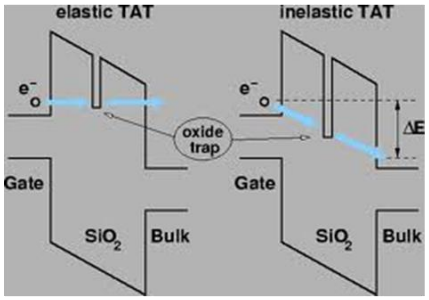
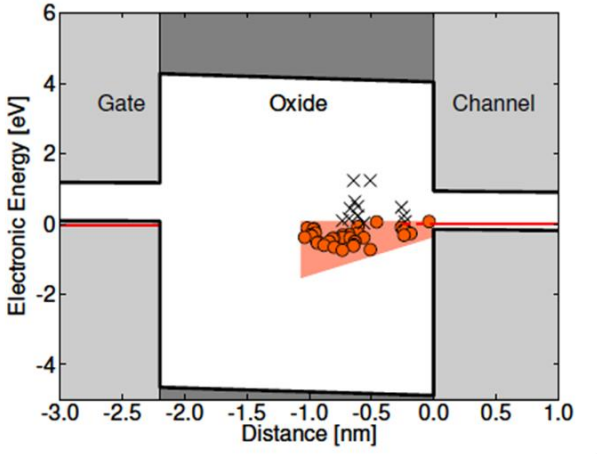
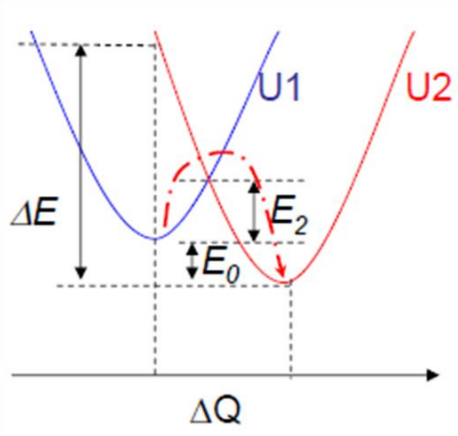
TRAP ASSISTED TUNNELLING







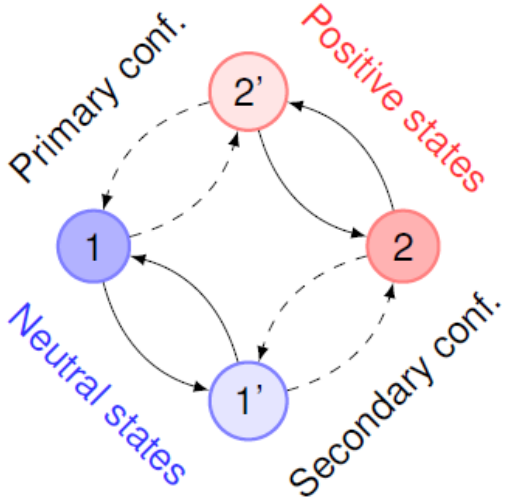
Experimental window



Configuration diagram

MODEL EXTRACTION

Identifying atomistic oxide trap responsible for NBTI:



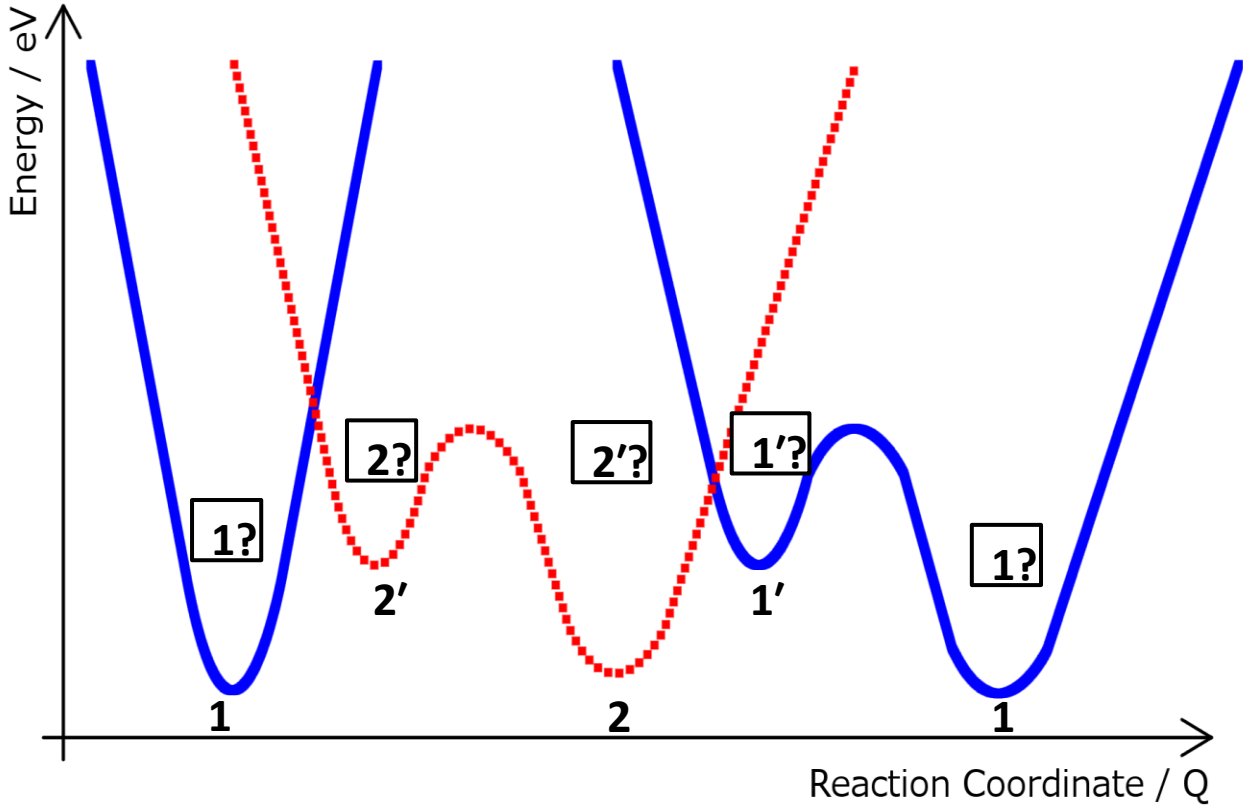
- Multi-state Multi-phonon model
- $\tau_c = \tau_{12'} + \tau_{2'2}(1+ \tau_{12'} / \tau_{2'1})$
- $\tau_e^{-1} = \tau_{e1}^{-1} + \tau_{e2}^{-1}$
- $\tau_{e1} = \tau_{22'} + \tau_{2'1}(1+ \tau_{22'} / \tau_{2'2})$
- $\tau_{e2} = \tau_{21'} + \tau_{1'1}(1+ \tau_{21'} / \tau_{1'2})$

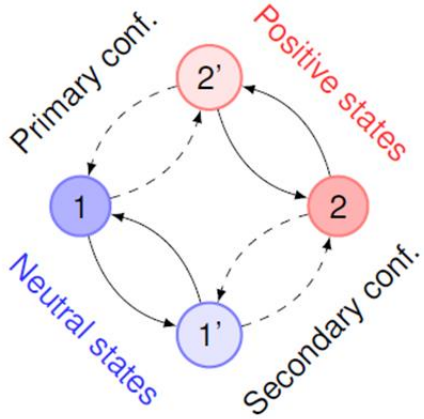
- Barrier-hopping transitions: $\tau_{\alpha\beta} = \nu^{-1} \exp[E_{\alpha\beta}/K_B T]$

- Vibronic transitions: $\tau_{if} = 2\pi/\hbar \, |\langle\Phi_f|V'|\Phi_i\rangle|^2 \, |\langle\eta_{f\beta}|\eta_{i\alpha}\rangle|^2 \, \delta(E_{f\beta}-E_{i\alpha})$
  - Summing over all vibrational states: Lineshape function
  - $fv^{(0/+)} = \text{avg} \, \Sigma \, |\langle\langle +F|0I\rangle\rangle|^2 \, \delta(E_{0I} - E_{+F} - E_{v0} - E)$

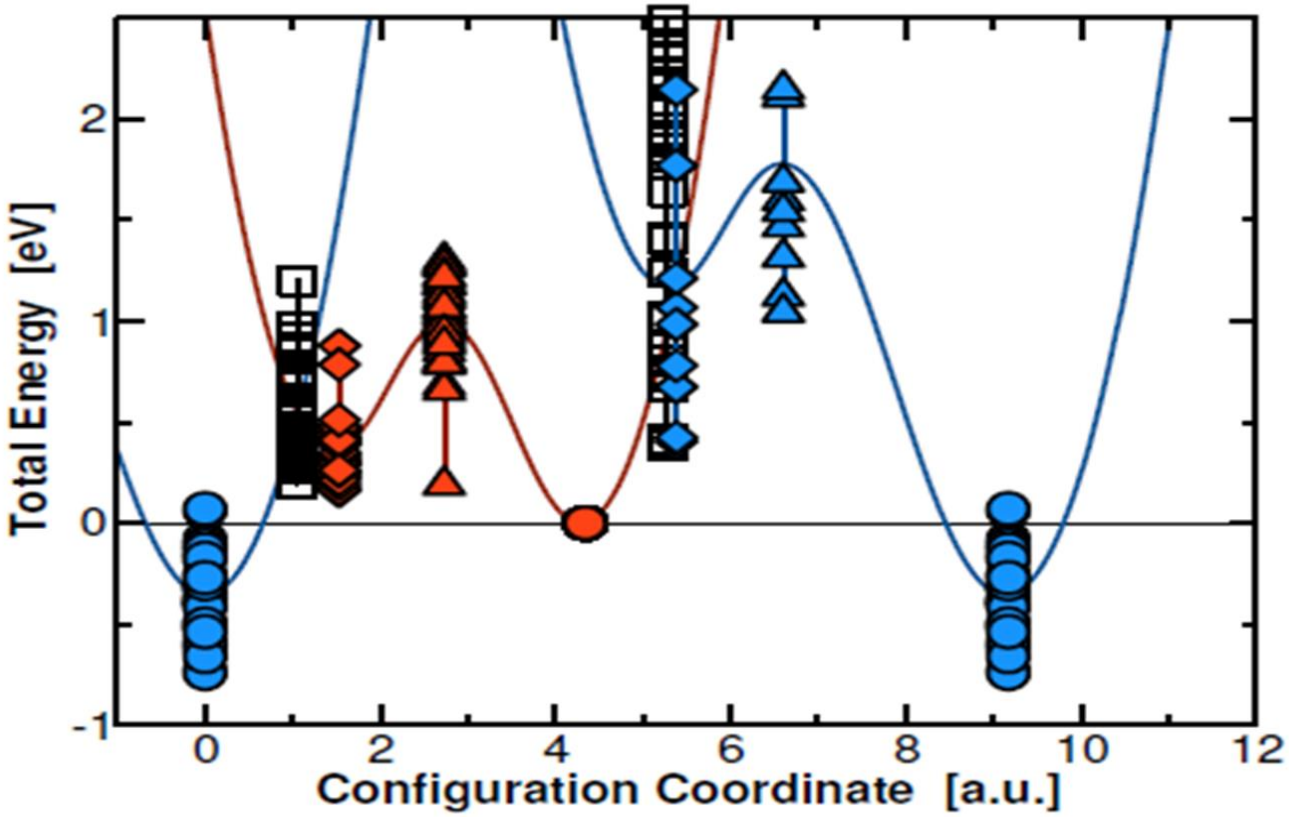
T. Grasser et al., IEEE TRANSACTIONS ON ELECTRON DEVICES 2011

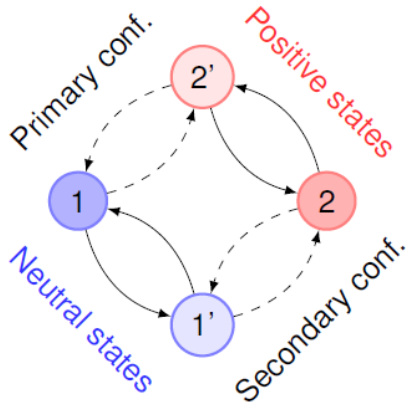
ENERGY LANDSCAPE: HYPOTHETICAL



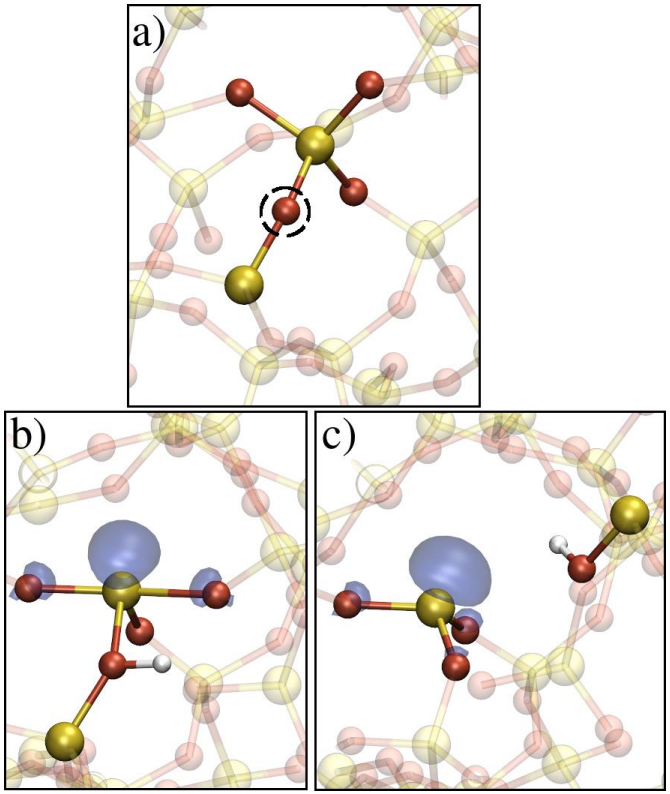


ENERGY LANDSCAPE: EXTRACTED





DEFECT MODELS



Atomic configuration and spin density of the two hydrogen induced defect configurations and their precursor:

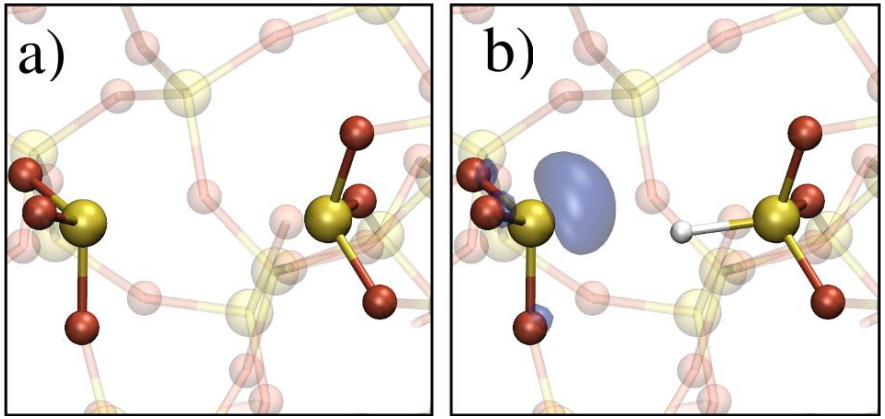
a) An unperturbed SiO_4 tetrahedron;

b) The **$[SiO_4/H]^0$ center**

c) The **hydroxyl E´ center**

A-M. El Sayed et al. Phys. Rev. B. 92, 014107 (2015)

DEFECT MODELS

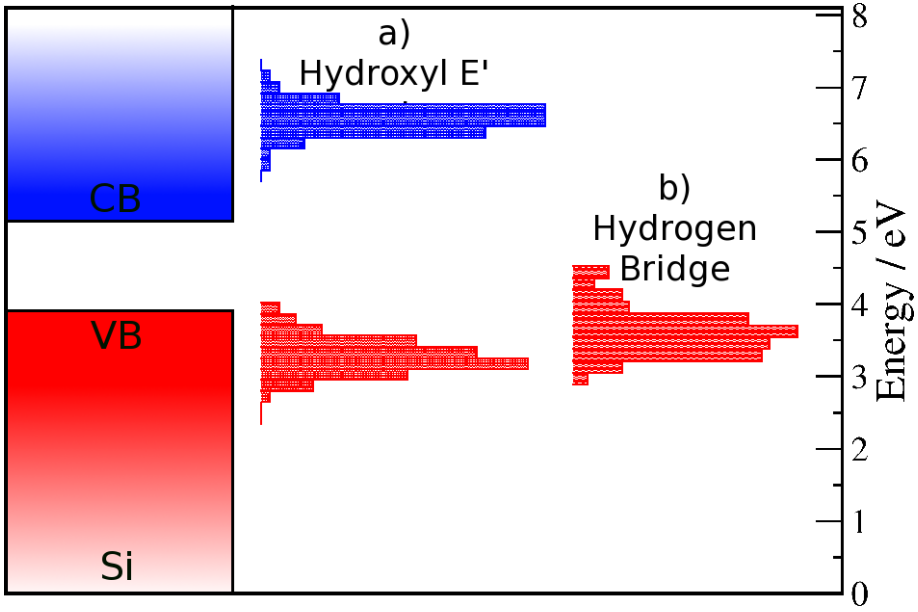


a) Atomic structure of the **oxygen vacancy** which is the precursor to the hydrogen bridge

b) Atomic structure and spin density of the **hydrogen bridge**

A-M. El Sayed et al. Phys. Rev. B. 92, 014107 (2015)

DISTRIBUTION OF DEFECT LEVELS

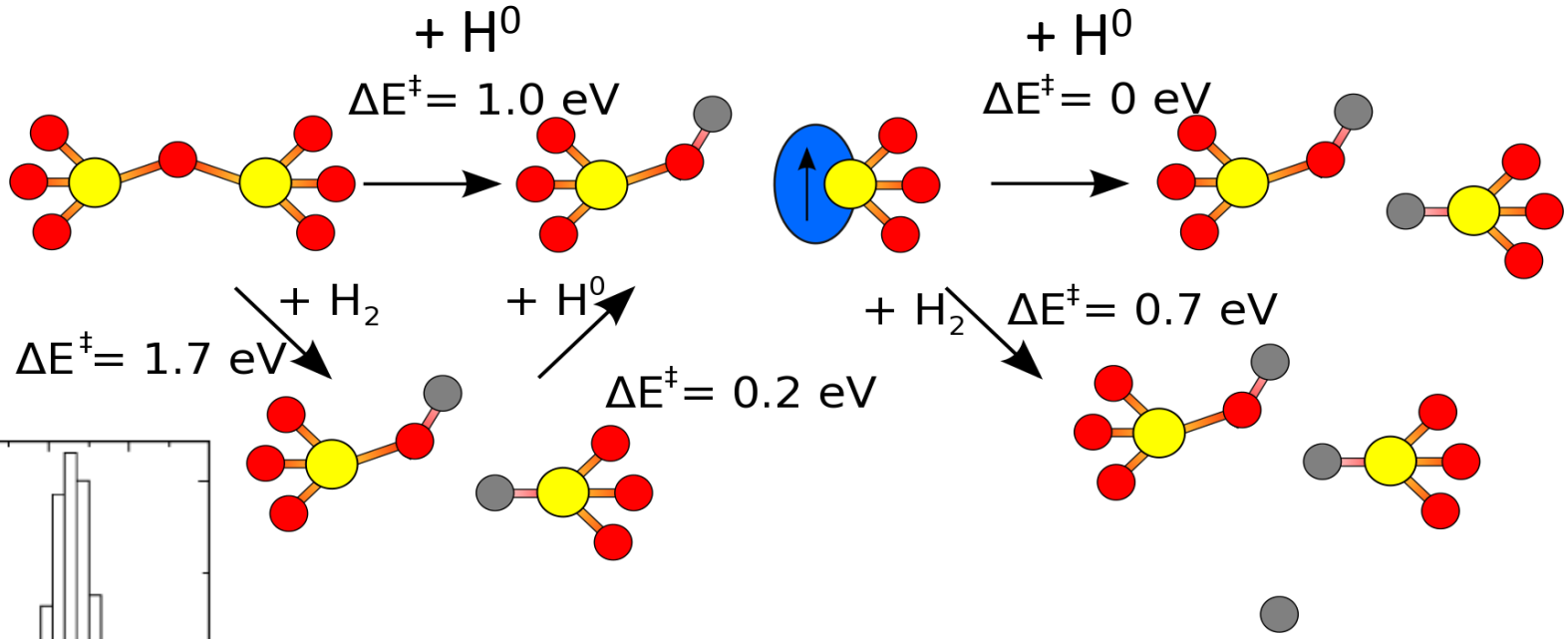


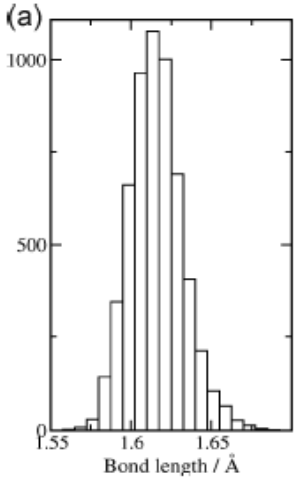
Histogram of the one-electron levels of defect configurations of:
a) the hydroxyl E´ center,
b) the hydrogen bridge defect

The area in the histograms colored dark red show occupied states while the area of the histograms colored blue show the unoccupied states.

A-M. El Sayed et al. Phys. Rev. B. 92, 014107 (2015)

HYDROGEN REACTIONS

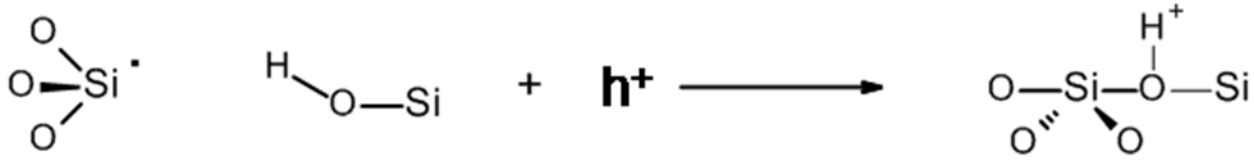




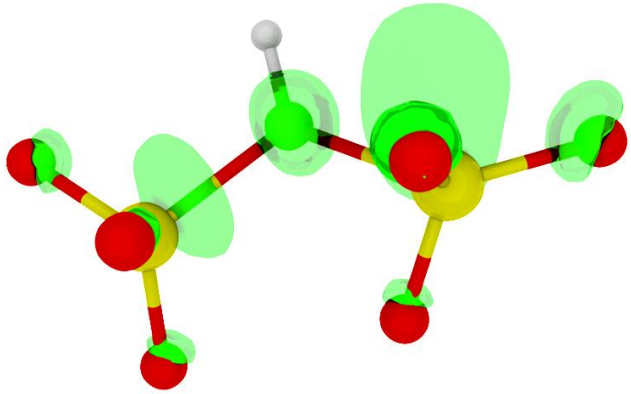
H^0 can break strained Si – O bonds

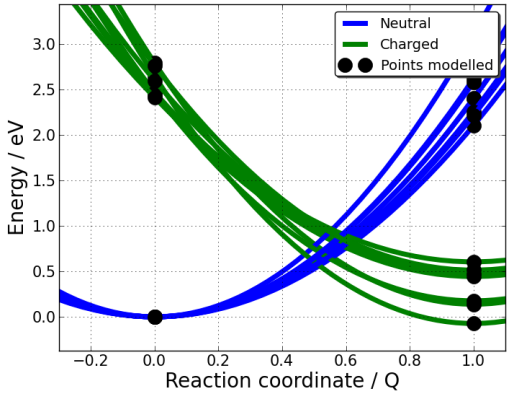
Hydroxyl E' centre is formed at sites where Si – O bond is > 1.65 Å

HOLE TRAPPING AFTER DEFECT ACTIVATION



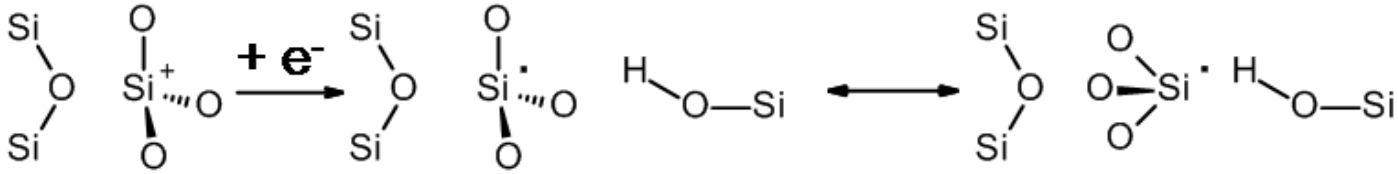
- **Hole** can be trapped on the defect state ~ 3.5 eV above SiO_2 VB
- **Two** configurations are possible. Si-O bond can reform and proton is bound to bridging O

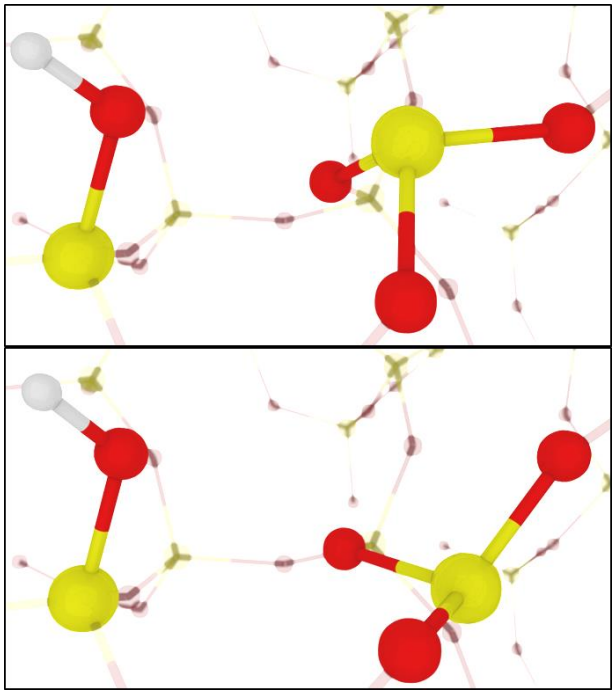




A-M. El-Sayed et al. Microel. Eng. 147, 141 (2015)

ELECTRON RE-TRAPPING





- A metastable state in the neutral charge state for the puckered configurations where an electron is trapped on a back-projected O_3Si
- The barrier from the back-projected configuration to the ground state is <1.1 eV> (0.3 – 1.6 eV) while the back-projected configuration is higher in energy by <0.7 eV> (0.2 – 1.6 eV)

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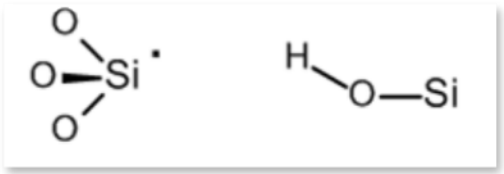
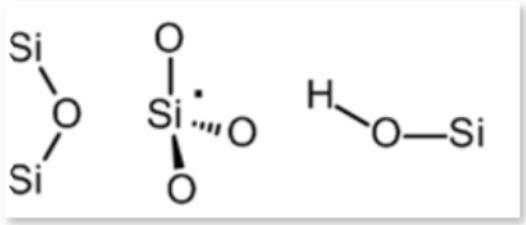
HYDROXYL E´ CENTRE: SUMMARY

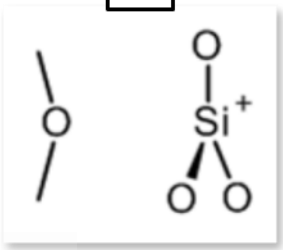
1



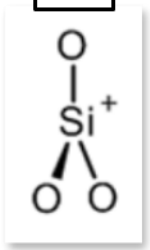
1′

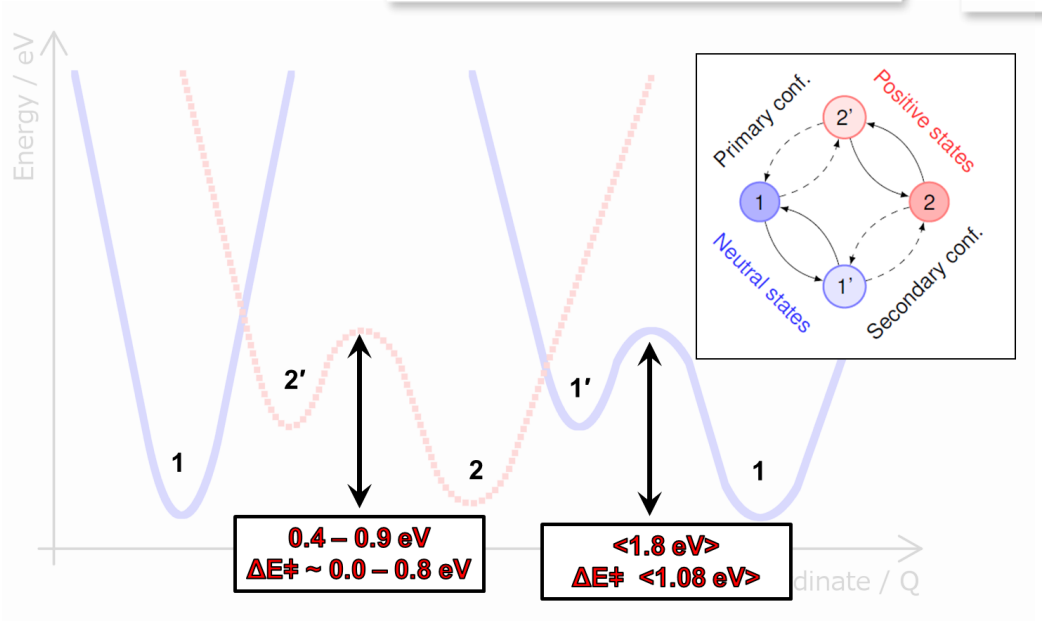


2



2′





MORDRED

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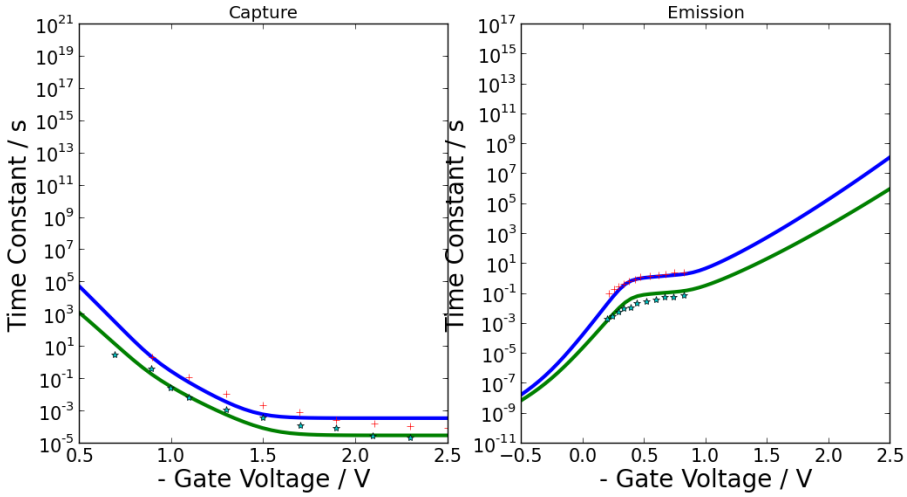
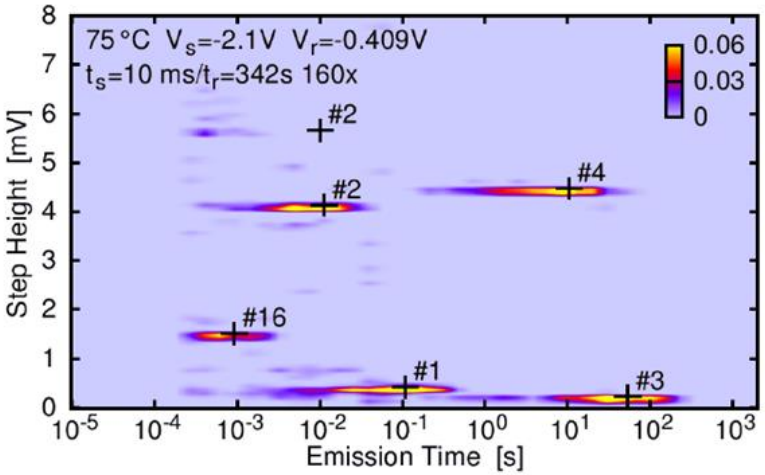
HYDROXYL E´ CENTRE: RATES





Calculated defect parameters give good agreement with the capture and emission rate dependence on voltage and temperature

SUMMARY AND OUTLOOK

- Developed a multi-scale methodology for determining defects in the gate oxide and interface layer responsible for fixed charge and BTI
- Multi-state Multi-phonon model is used to calculate capture and emission events in Si/SiO_2 devices linked to ab initio calculations
- H generates defect states in a-SiO_2 which are resonant with Si CB
- H used in device manufacturing processes to passivate electrically active defects can also activate defects
- Similar processes explain reliability issues in high-k stacks

Eberhard Baer, Fraunhofer IISB

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VARIABILITY-AWARE PROCESS SIMULATION IN SUPERTHEME

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OUTLINE

1. Introduction
2. Software components
3. Example: through-silicon via (TSV) processing
4. Example: simulation of spacer patterning for FinFET structure
5. Conclusions

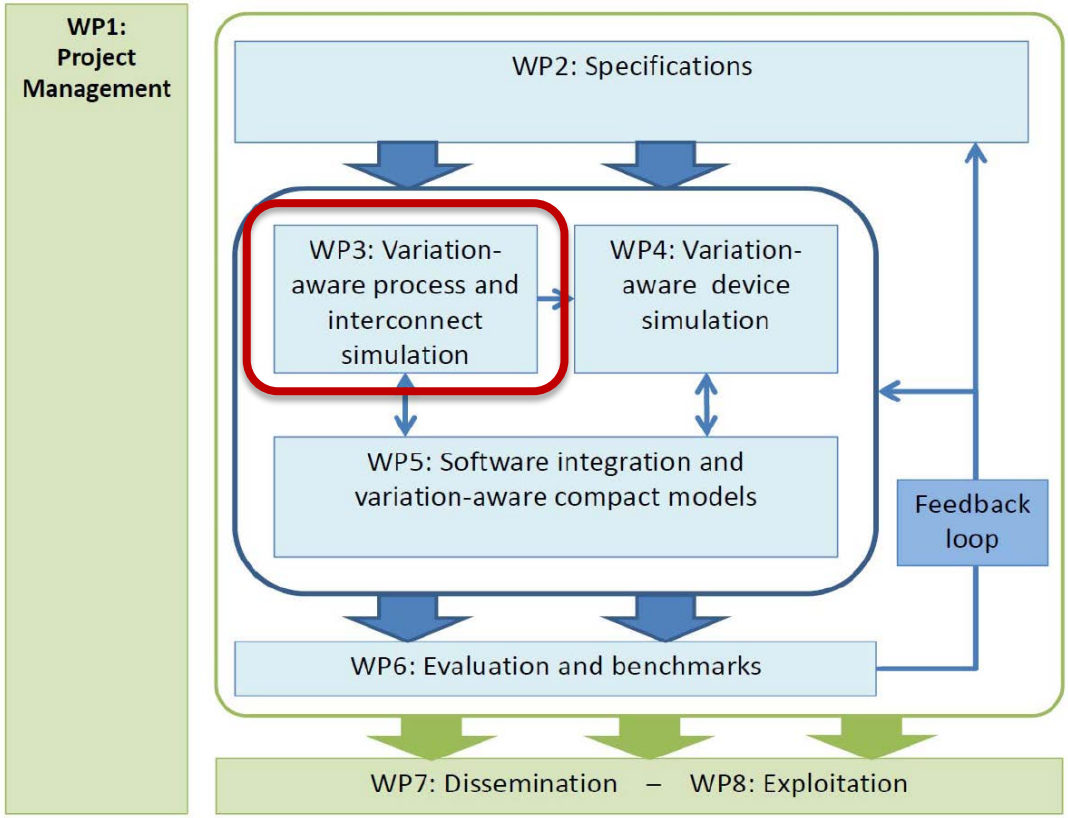
1

INTRODUCTION

INTRODUCTION – GOALS AND STRATEGY

- Quantification of process variability at its source at equipment level
- Variation-aware simulation of the processes for the fabrication of active semiconductor devices and interconnects
- Modeling of performance and reliability of interconnects and their dependence on the fabrication process
- Proprietary software of the partners IISB and TUW as well as third-party software are used, extended, and integrated

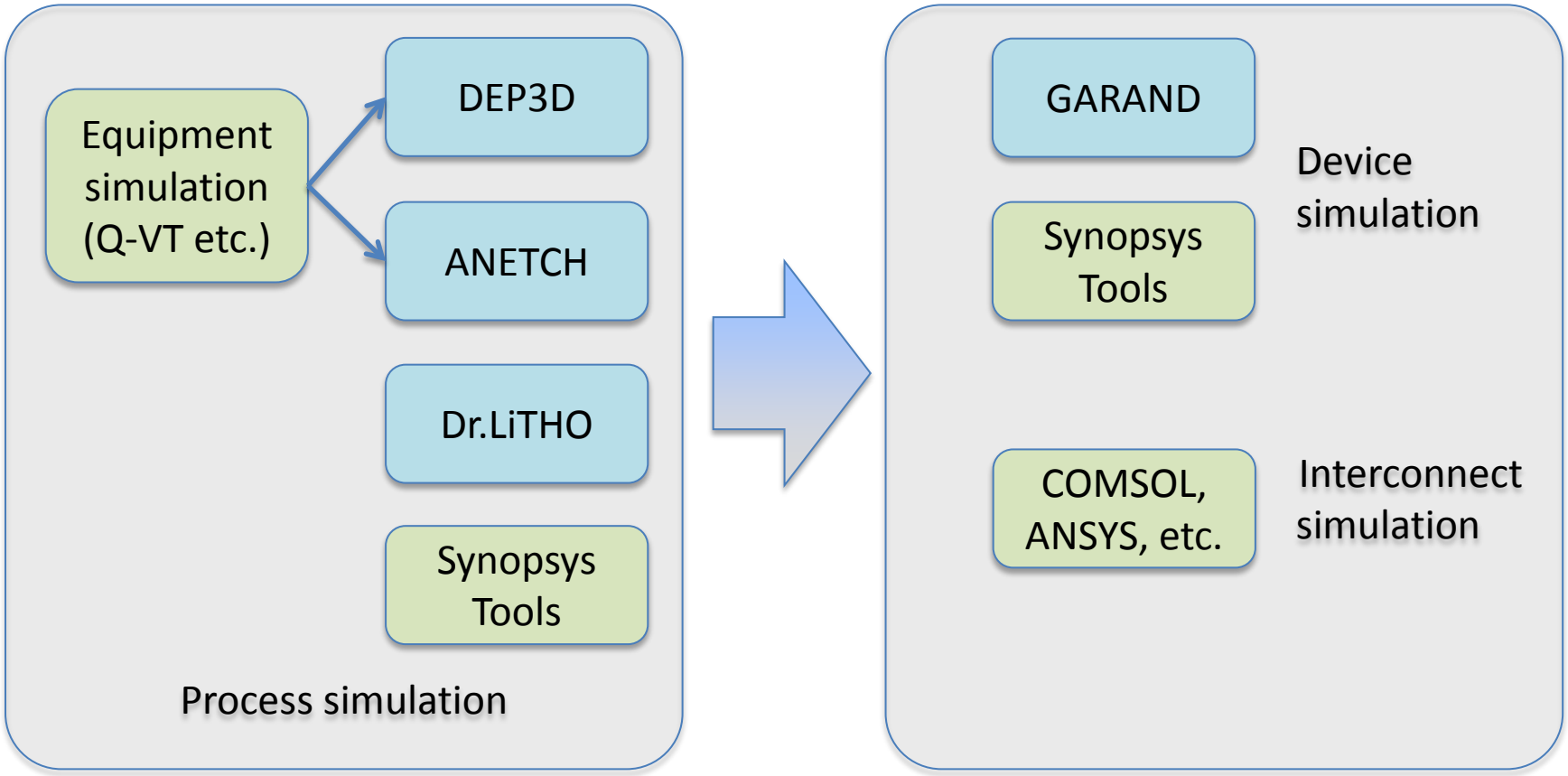
INTRODUCTION – PROJECT CONTEXT



2

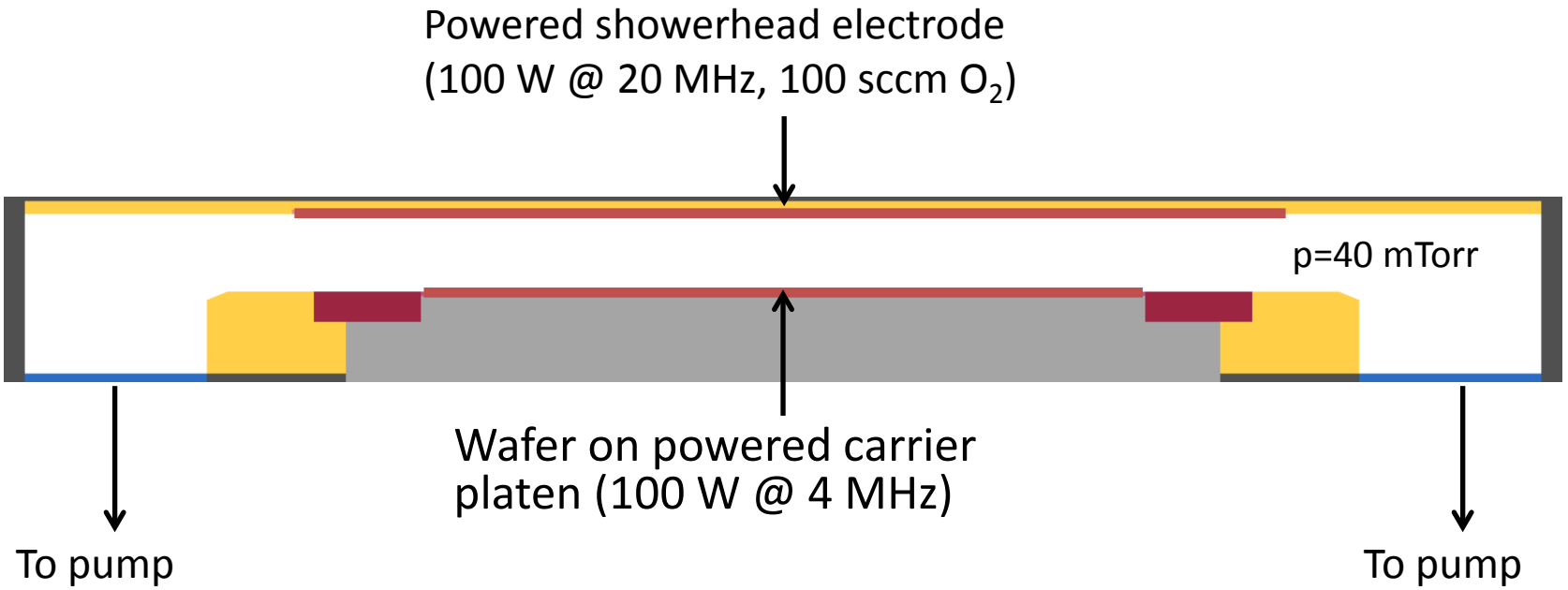
SOFTWARE COMPONENTS

SOFTWARE COMPONENTS



3

EXAMPLE: THROUGH-SILICON VIA (TSV) PROCESSING



PLASMA-ENHANCED CHEMICAL VAPOR DEPOSITION (PECVD) OF SIO2 FROM TEOS AS PART OF TSV PROCESS

Simulation of PECVD capacitively coupled plasma (CCP) reactor using the software Q-VT (Quantemol), TEOS assumed to be saturated

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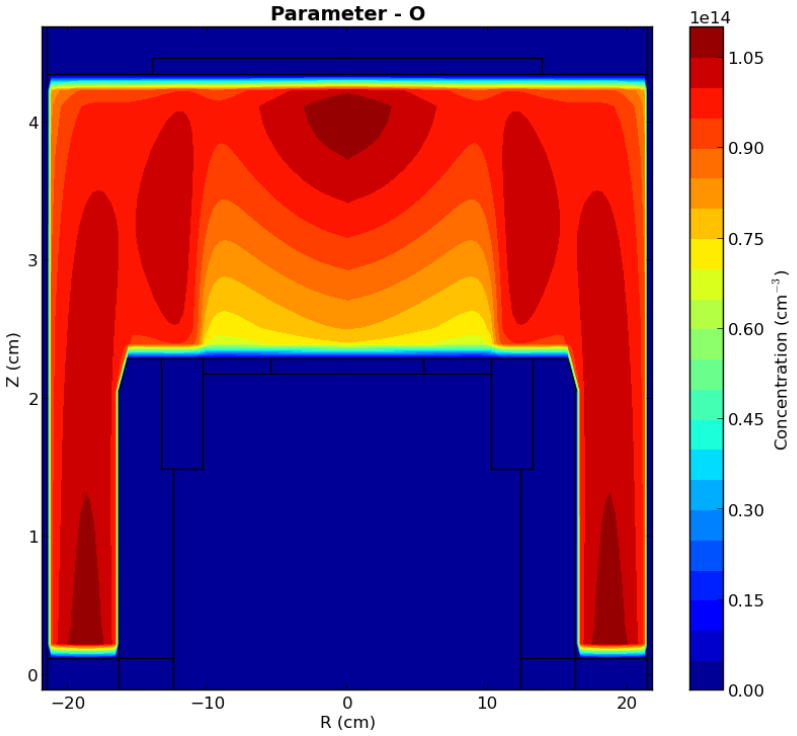
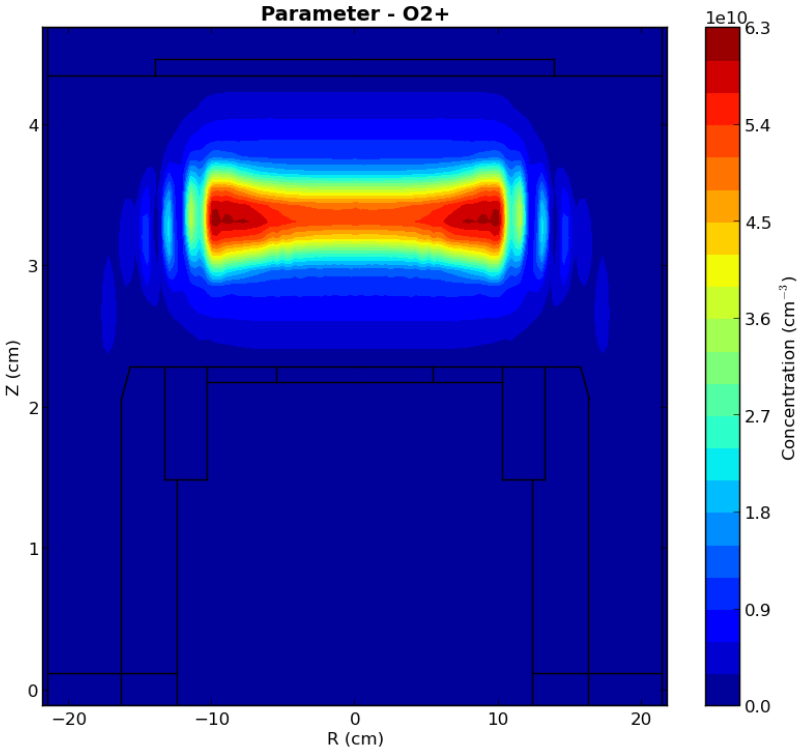
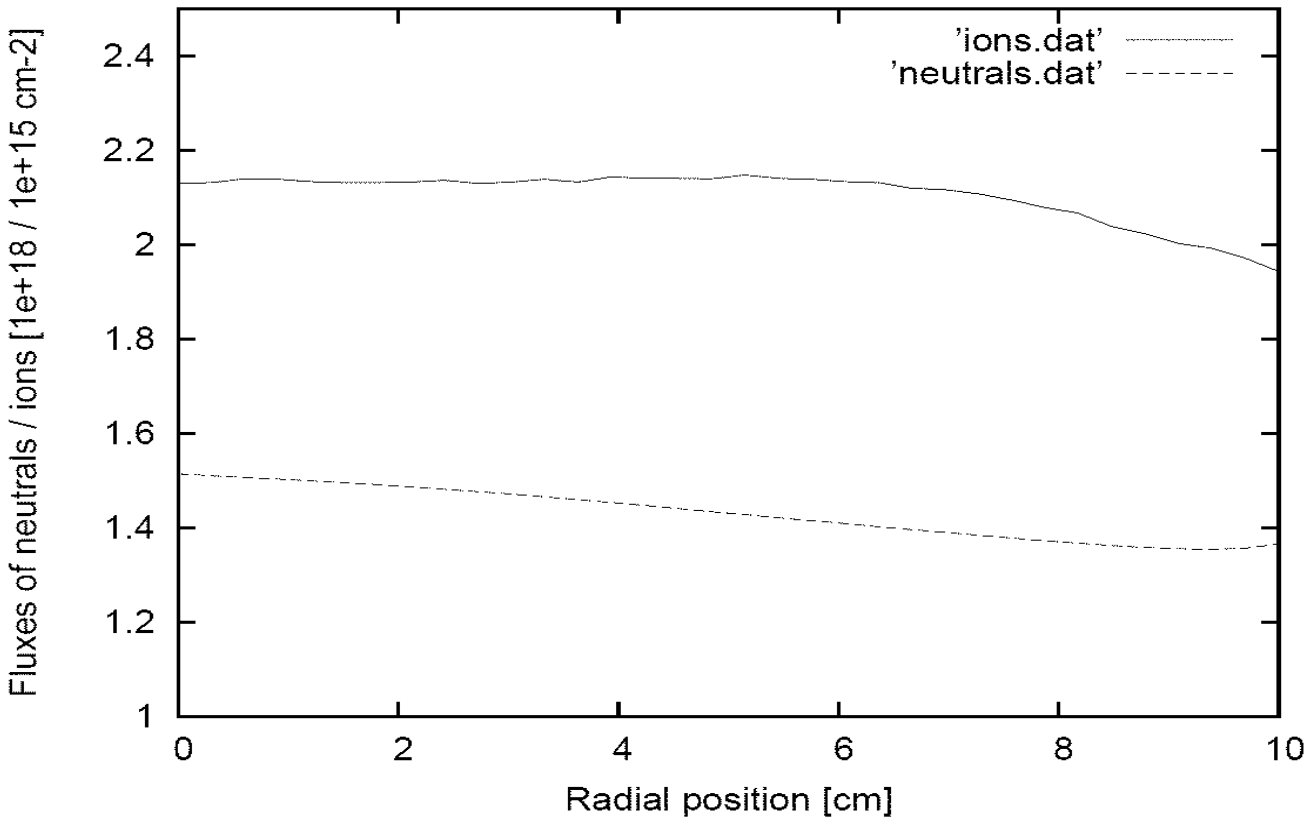
Neutrals (O)



Ions (O_2+)



Example for concentration of neutrals (O) and ions (dominant ion species is O_2+) in a CCP reactor (figure aspect ratio is scaled)



Example for flux at wafer vs. radial position for neutrals (O) and ions (dominant ion species is O_2+) in a CCP reactor

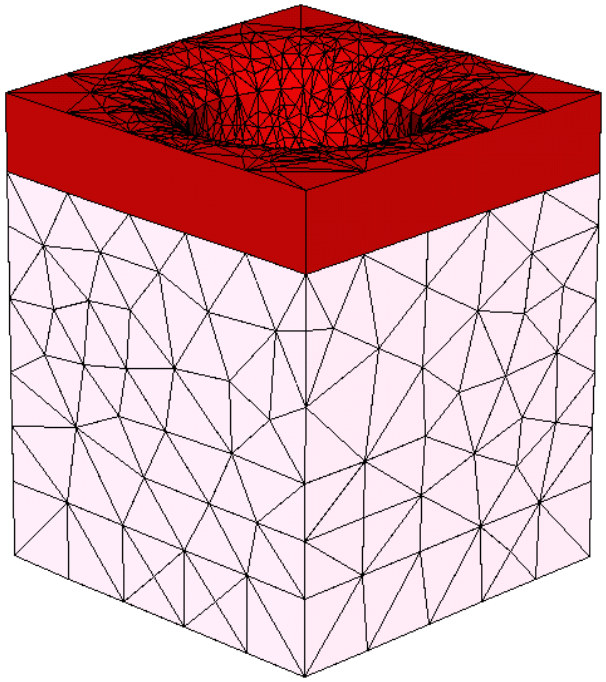
MODELING OF PECVD OF SILICON OXIDE ON FEATURE SCALE

- Rate contributions are due to
  - Neutrals (radicals): isotropic angular distribution
  - Ions: Gaussian distribution
- Local rate $R_{PECVD} \sim (s_c F_{neutral} + F_{ion})$, with
  - F_x: local particle flux of neutrals and ions, respectively
  - s_c: neutral sticking coefficient
- Model parameters
  - **r** = $R_n / (R_n + R_i)$ in 1D regions (R_i is rate resulting from ions, R_n is rate resulting from neutrals)
  - Sticking coefficient of neutrals **s_c**
  - σ of Gaussian distribution for ions

MODEL PARAMETER VARIATIONS ACROSS WAFER

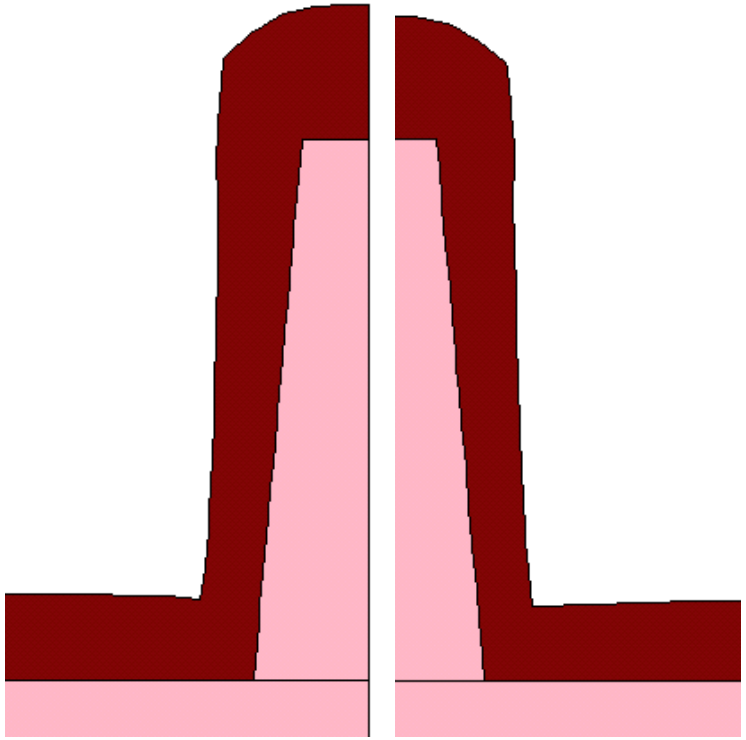
Position [cm]	O_2^+ ion flux [1e15 cm^{-2}]	Neutral flux [1e18 cm^{-2}]	$r = R_n / (R_n + R_i)$ in 1D regions	d_{top} [µm]
0.0	2.13	1.52	0.80	1.0
1.8	2.13	1.49	0.80	0.99
3.9	2.14	1.45	0.79	0.97
5.8	2.14	1.42	0.79	0.95
7.9	2.08	1.37	0.79	0.92
10.0	1.94	1.37	0.80	0.90

SiO_2 layer deposited in hole

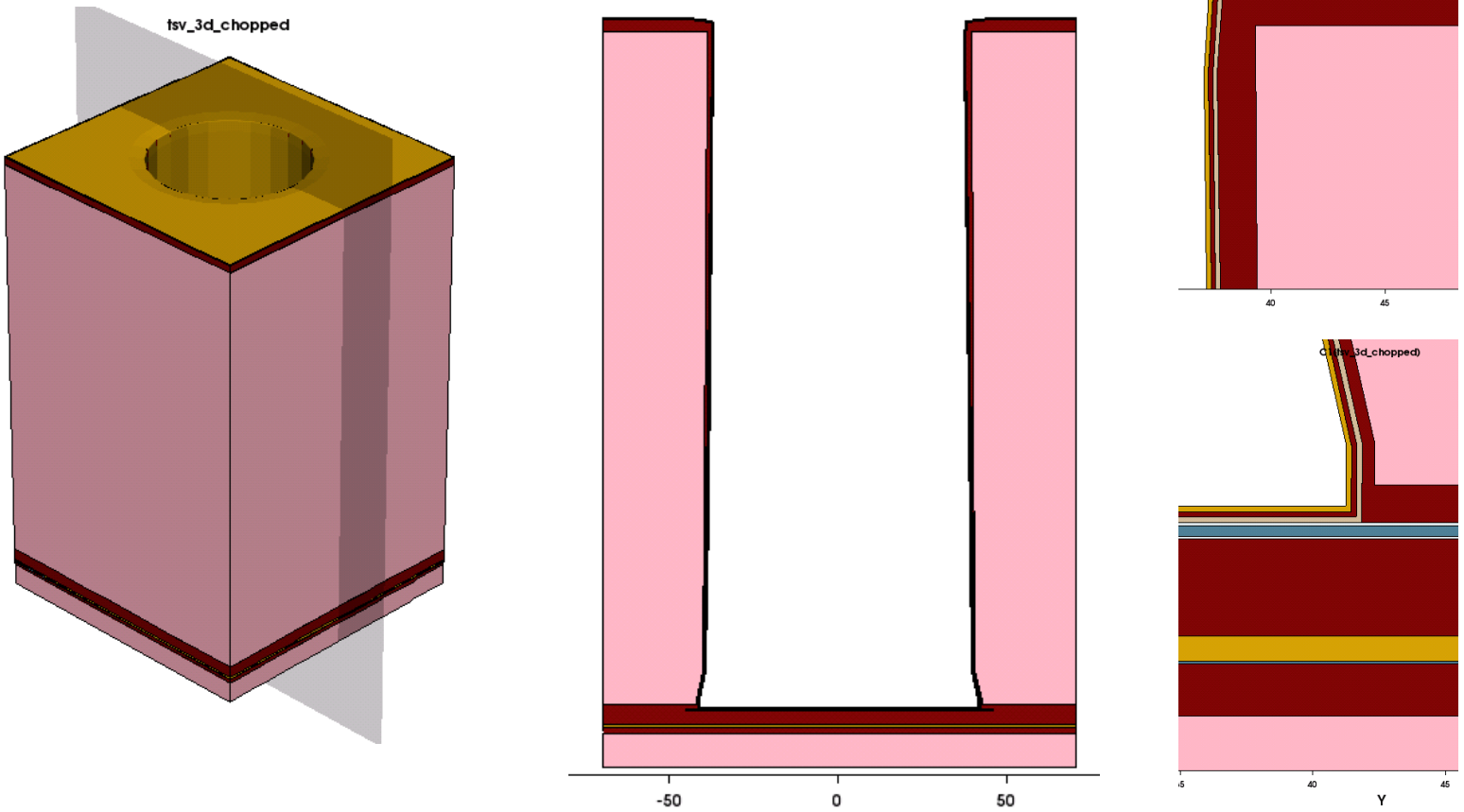


Wafer center

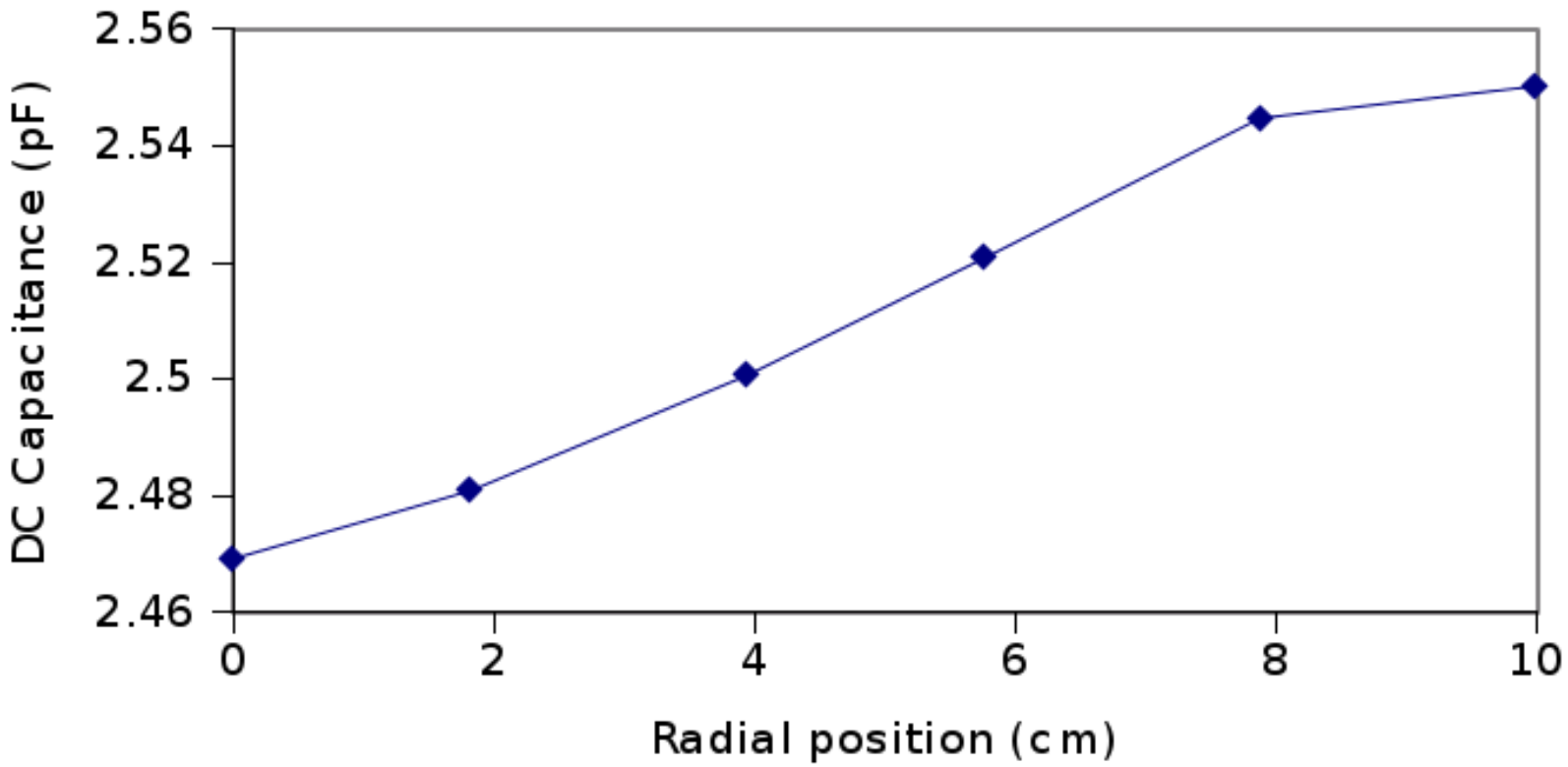
10.0 cm off-center



EXAMPLE FOR PROFILE VARIATION ACROSS WAFER



In the TSV, two PECVD layers form part of the oxide layer stack before tungsten deposition



Simulated variation (COMSOL) of DC capacitance between different positions of the TSV structure on the wafer

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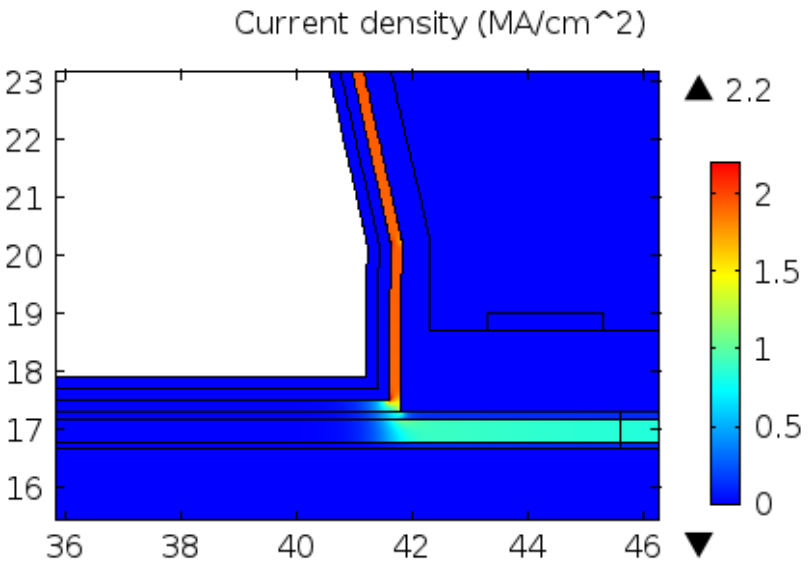
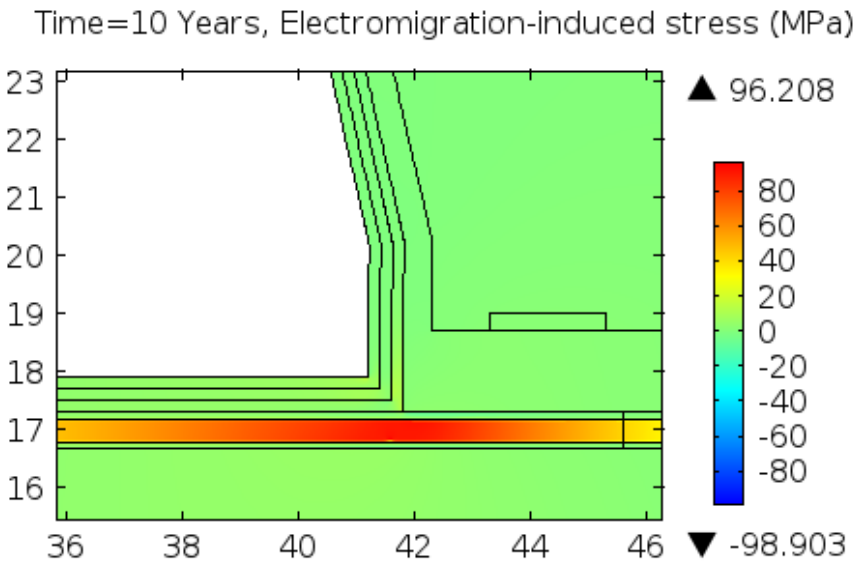
Current density distribution



Resulting electromigration-induced stress distribution after 10 years



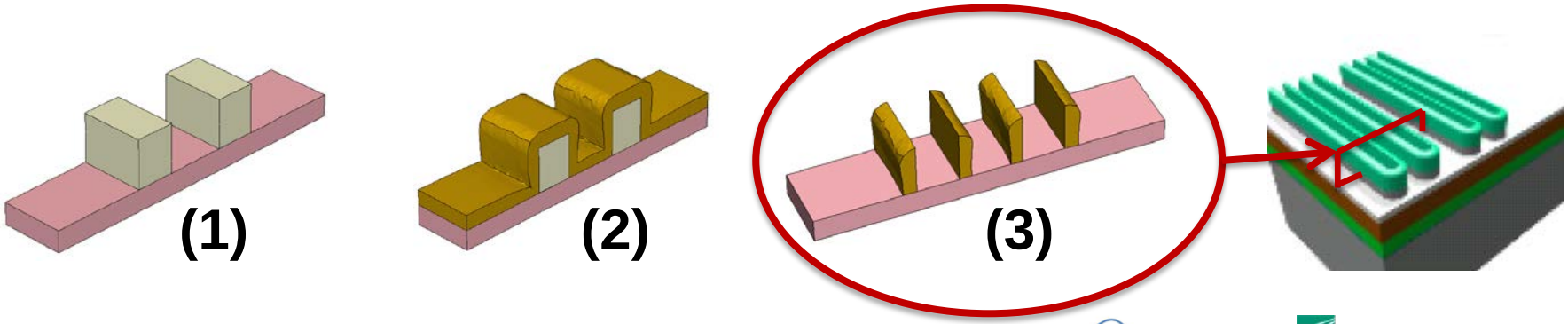
SIMULATED CURRENT DENSITY AND STRESS

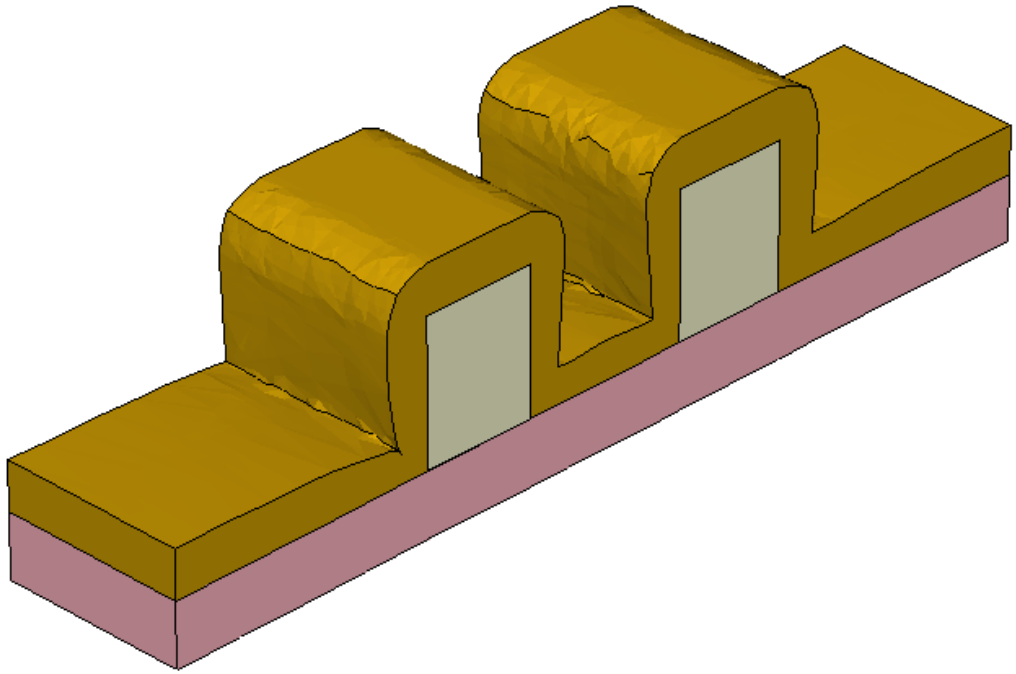
4

EXAMPLE: SIMULATION OF SPACER PATTERNING FOR FINFET STRUCTURE

SIMULATION OF SPACER PATTERNING FOR FINFET STRUCTURE AS PART OF SRAM CELL

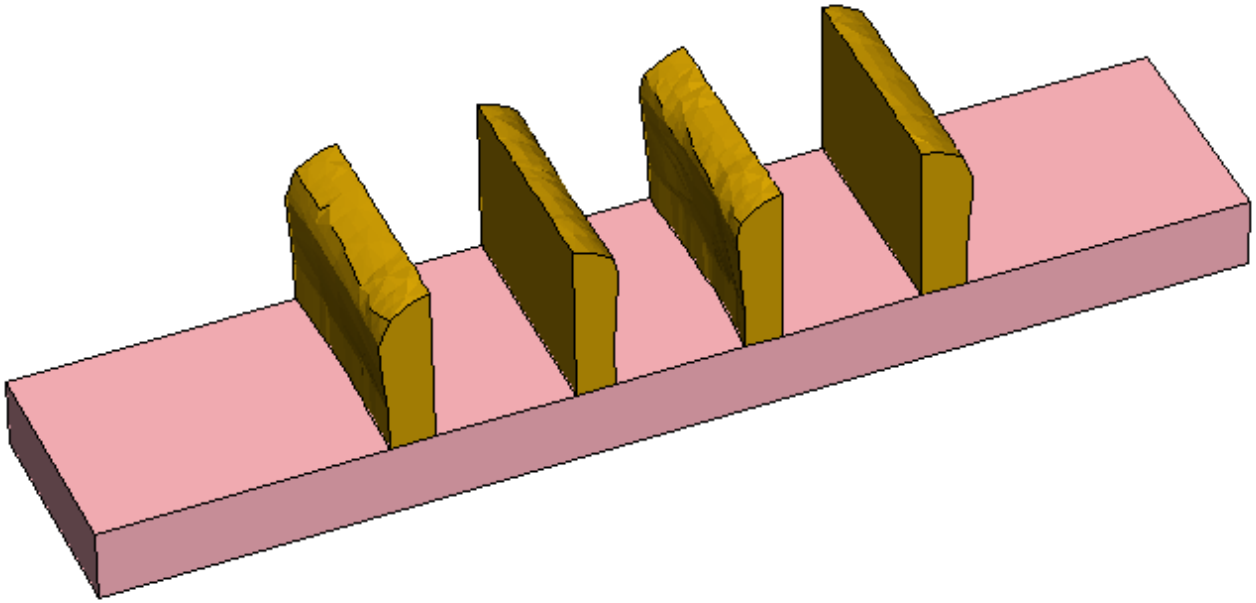
- Carbon lines are created using CD values from a lithography model (1)
- CVD oxide is deposited (2) and etched back to form the spacers after carbon line removal (3)





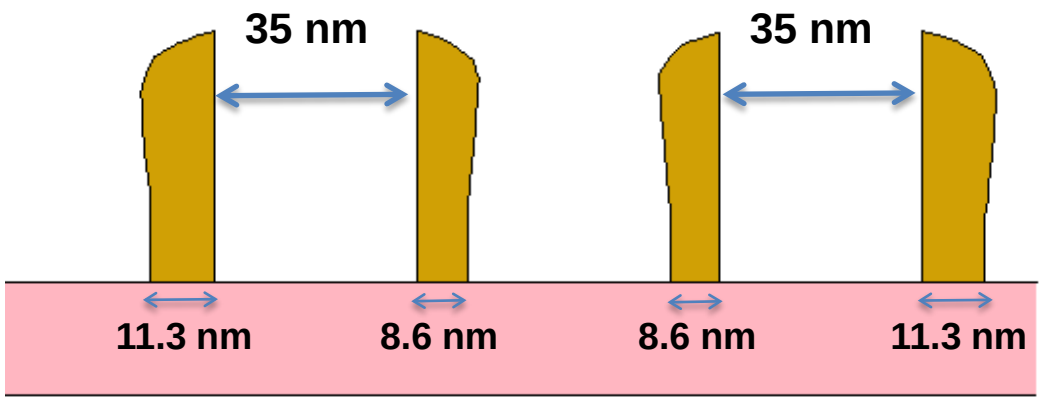
MODELING OF NON-CONFORMAL OXIDE DEPOSITION

Chemical vapor deposition simulated with IISB physical deposition simulator DEP3D using single sticking coefficient model (sticking coefficient s_c = 0.5)



MODELING OF ANISOTROPIC ETCHING

Etching emulated as perfectly anisotropic, using geometrical model of Synopsys SPROCESS. Etching is followed by removal of carbon lines.



CD [nm]	Bottom width inner spacers [nm]	Bottom width outer spacers [nm]
31.5	8.9	11.3
35	8.6	11.3
38.5	8.3	11.3

Simulation for **nominal CD (35 nm)** of carbon lines

Variation of CD of carbon lines leads to a variation of the **bottom width** of the inner spacers

5

CONCLUSIONS

CONCLUSIONS

- Coupling between equipment- and feature-scale simulation allows us to take into account equipment effects for feature-scale modeling
  - As an example, for PECVD of SiO_2 using TEOS chemistry, the coupling has been implemented by transferring fluxes of ions and neutrals from equipment- to feature-scale
  - The simulations have been integrated into the process flow simulation for the fabrication of a TSV structure
  - The simulated structures were transferred to electrical and mechanical modeling for performance and reliability analysis
- Coupled simulation of topography steps allows us to predict variation effects on feature-scale level
  - As an example, spacer patterning for a FinFET structure was shown

Asen Asenov, Salvatore M. Amoroso
Gold Standard Simulations Limited/University of Glasgow

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VARIABILITY-AWARE DEVICE SIMULATION IN SUPERTHEME

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OUTLINE

1. Introduction
2. Modeling Methodology for variability
3. Interplay of Process and Statistical Variability
4. Conclusions

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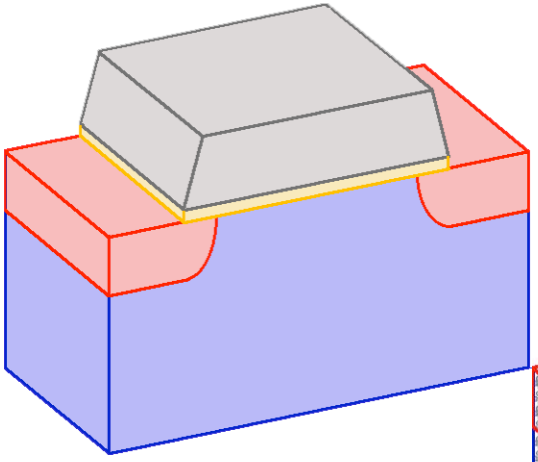
OUTLINE

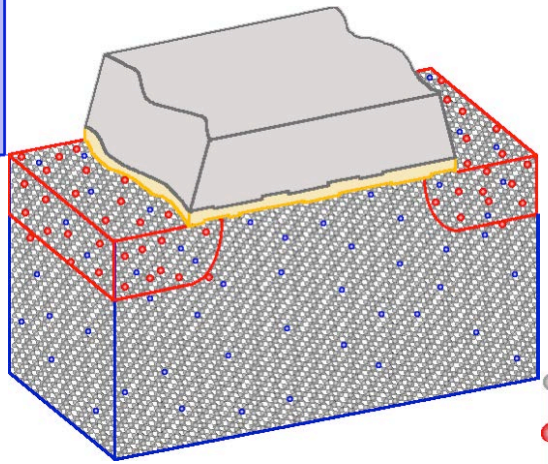
1. **Introduction**
2. Modeling Methodology for variability
3. Interplay of Process and Statistical Variability
4. Conclusions

SUPERTHEME GSS University of Glasgow

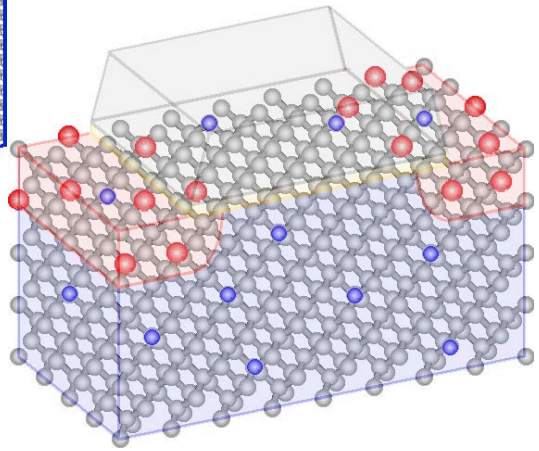
The semiconductor industry is facing atomic scale limitations



The simulation
Paradigm now



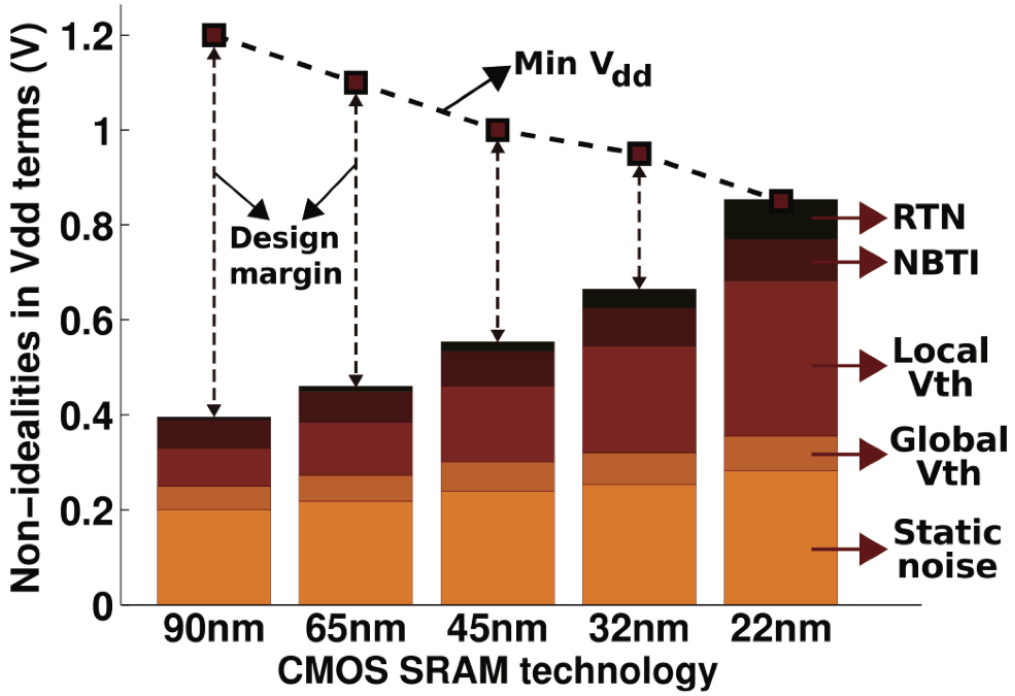
A 22 nm MOSFET
In production 2013



A 4.2 nm MOSFET
In production ????

A. Asenov 1998

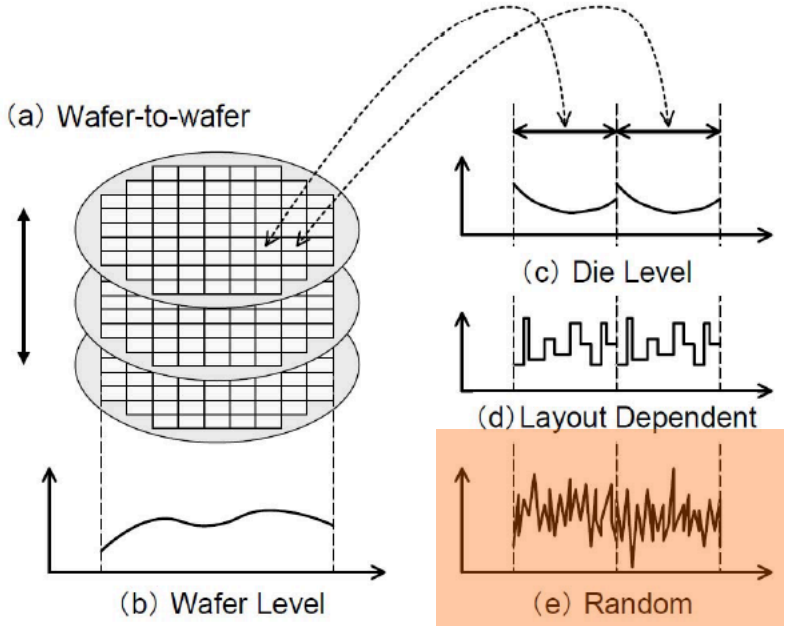
Statistical variability is one of the major challenges associated with scaling



After K. Takeuchi (NEC)

Variability results in higher parametric yield loss

Variability Decomposition



(Takeuchi, Nishida, Hiramoto, SISPAD 2009)

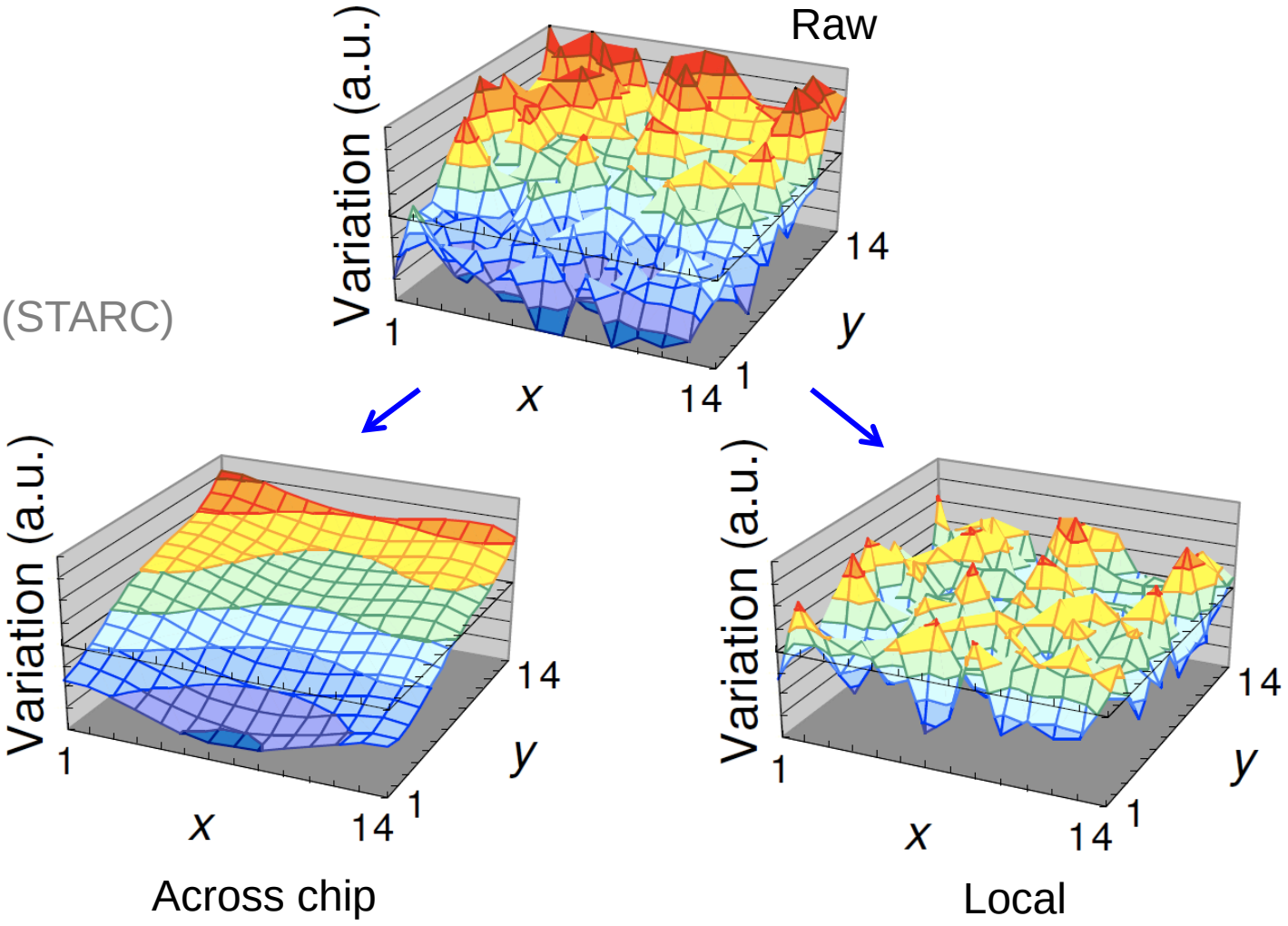
	Process	Environment	Temporal
Global	<L_g> and <W>, <layer thicknesses>, <R>'s, <doping>, <t_{ox}>, <V_{body}>	Operating temperature range, V_{DD} range	<NBTI> and Hot electron shifts
Local	**Line Edge Roughness (LER), Discrete doping, Discrete oxide thickness,** R and V_{body} distributions	Self-heating, IR drops	**Distribution of NBTI,** Voltage noise, SOI V_{body} history effects, Oxide breakdown currents
Across-chip	Line Width, due to pattern density effects	Thermal hot spots due to nonuniform power dissipation	Computational load dependent hot spots

(D. Frank, IBM)

- In general, the variability can be decomposed into global process variation and local random variability.
- PV: systematic, spatially correlated, long-range.
- SV: random, no (weak) correlation, short-range.

Variability Decomposition

M. Muracata (STARC)



Saturation in performance and increasing variability drives the CMOS innovations

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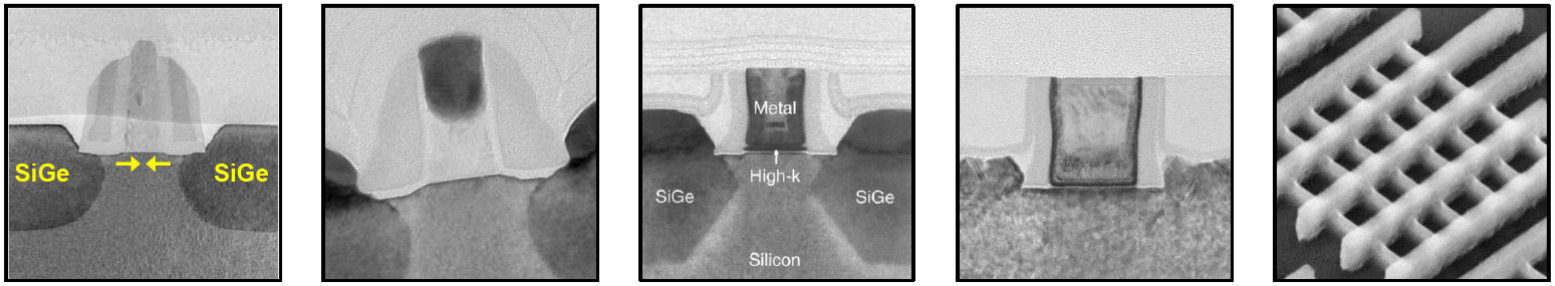
2003	2005	2007	2009	2011
90 nm	65 nm	45 nm	32 nm	22 nm



Invented SiGe Strained Silicon M Bohr (Intel)	2nd Gen. SiGe Strained Silicon	Invented Gate-Last High-k Metal Gate	2nd Gen. Gate-Last High-k Metal Gate	First to Implement Tri-Gate

Strained Silicon

High-k Metal Gate

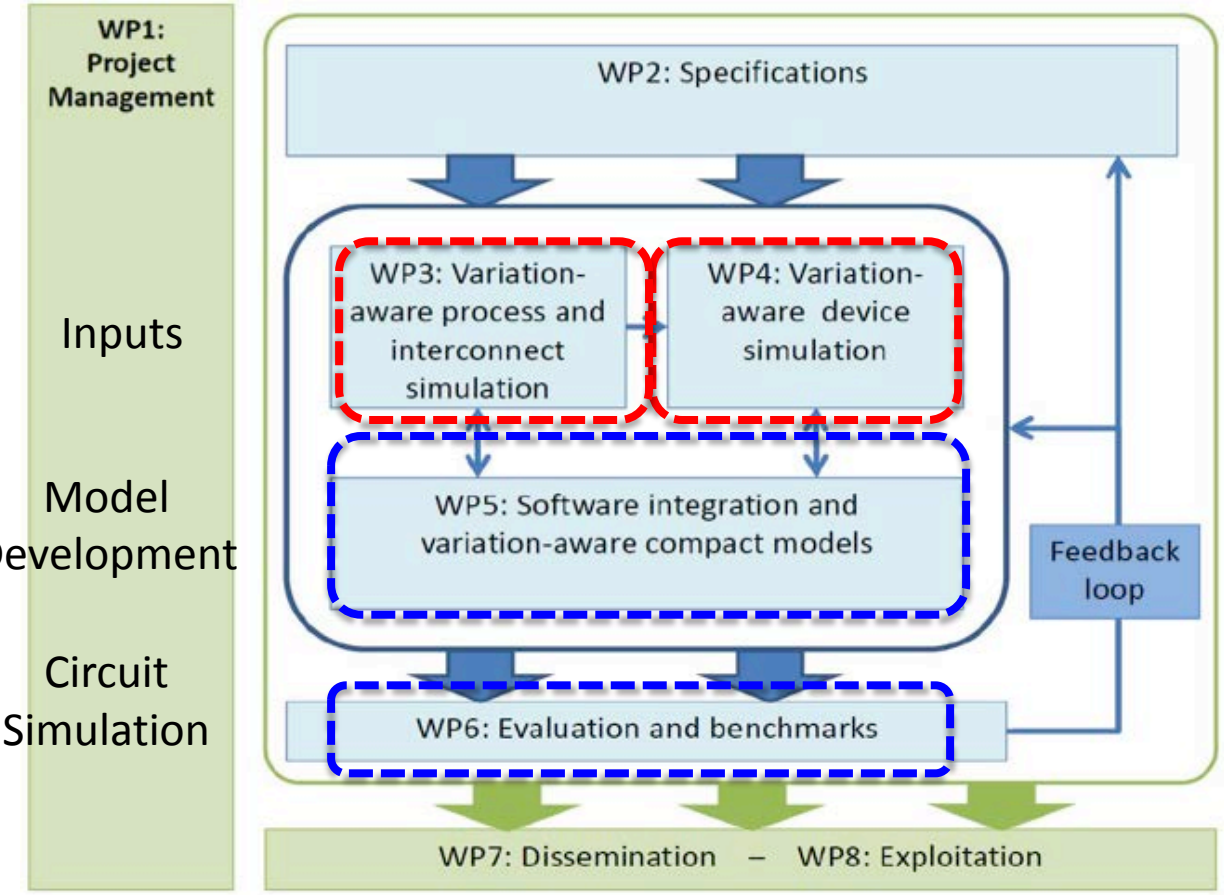
Tri-Gate

New transistor architectures improve performance and can reduce statistical variability

OUTLINE

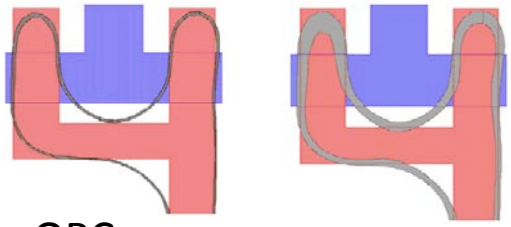
1. Introduction
2. **Modeling Methodology for variability**
3. Interplay of Process and Statistical Variability
4. Conclusions

SUPERTHEME - CONTEXT



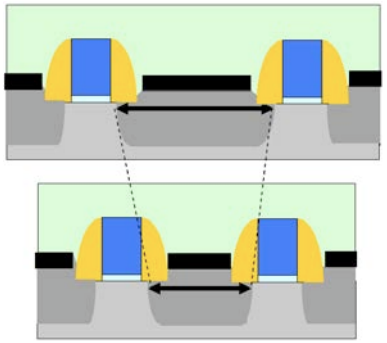
Process Variation - Systematic

- Lithography induced variations

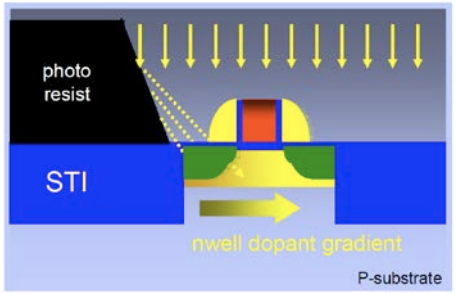


OPC
Intensity variation
Z-axis variation

- Stress induced variations

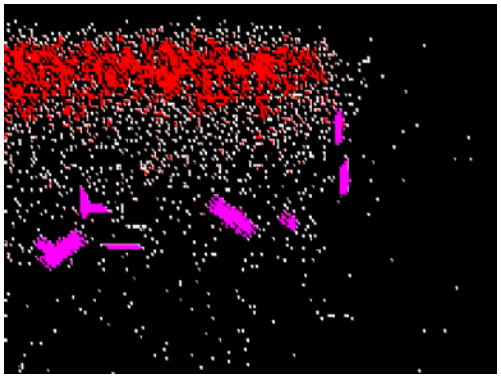


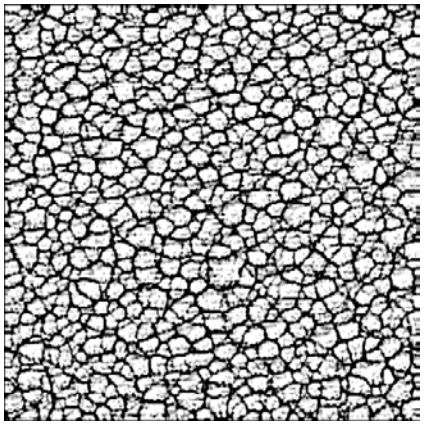
- Well Proximity effects

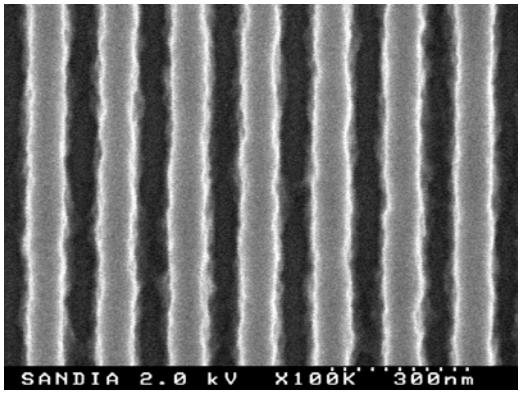


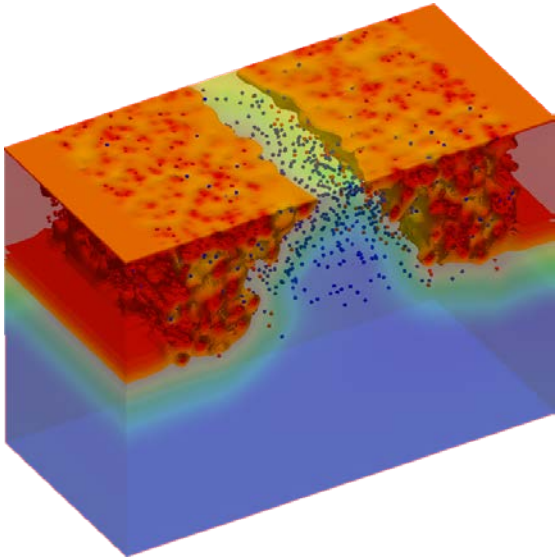
Extensively addressed in previous talks !

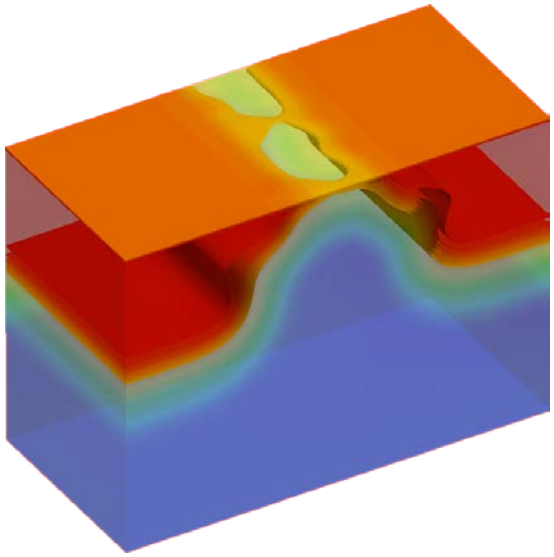
Main sources of Statistical Variability

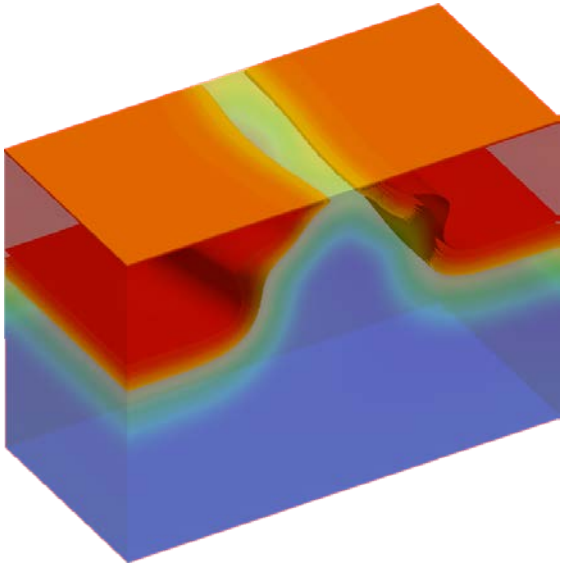










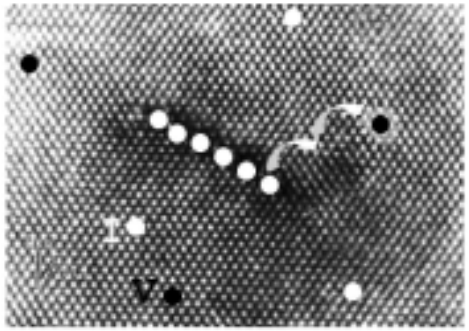


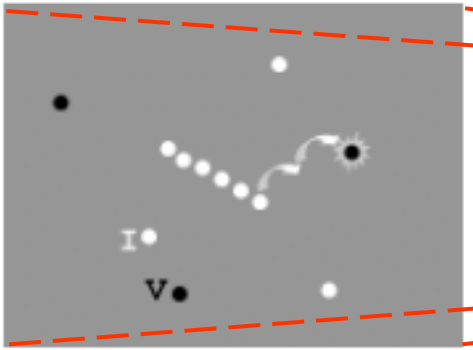
Random discrete dopants

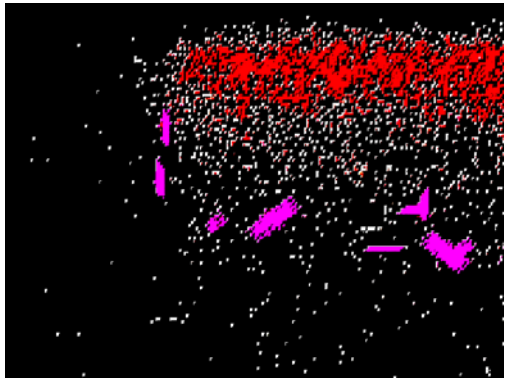
Metal Gate Granularity

Line edge roughness

RDD in Simulation (1)- Atomistic Process Simulation

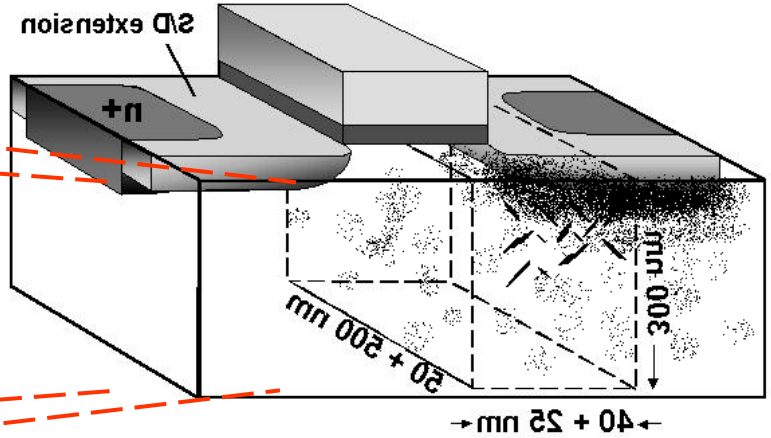






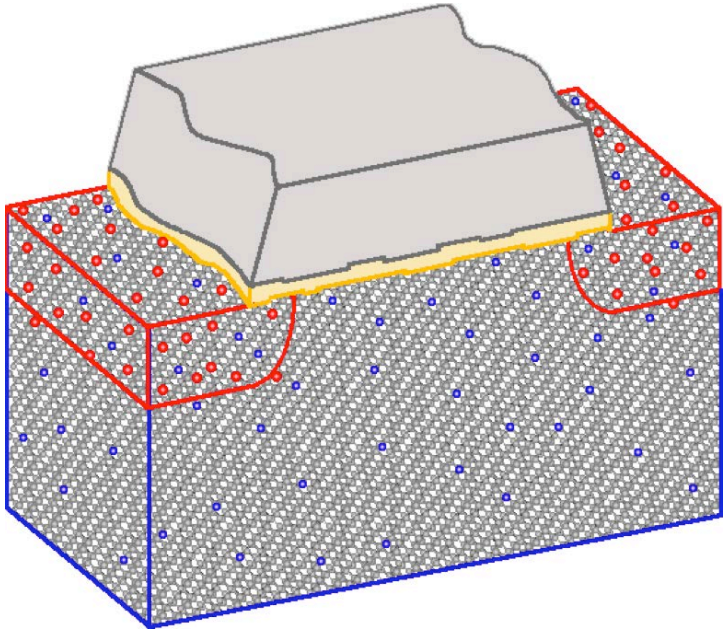
Output

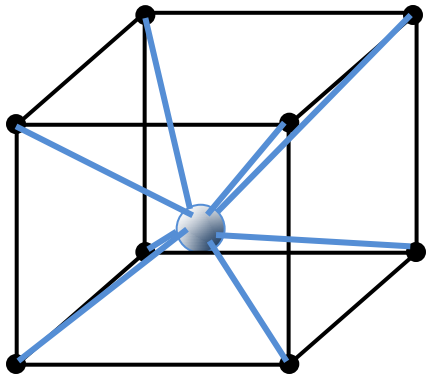
KMC Simulator



DADOS, Synopsys

RDD in Simulation (2)- Poisson Distribution + realistic doping profile

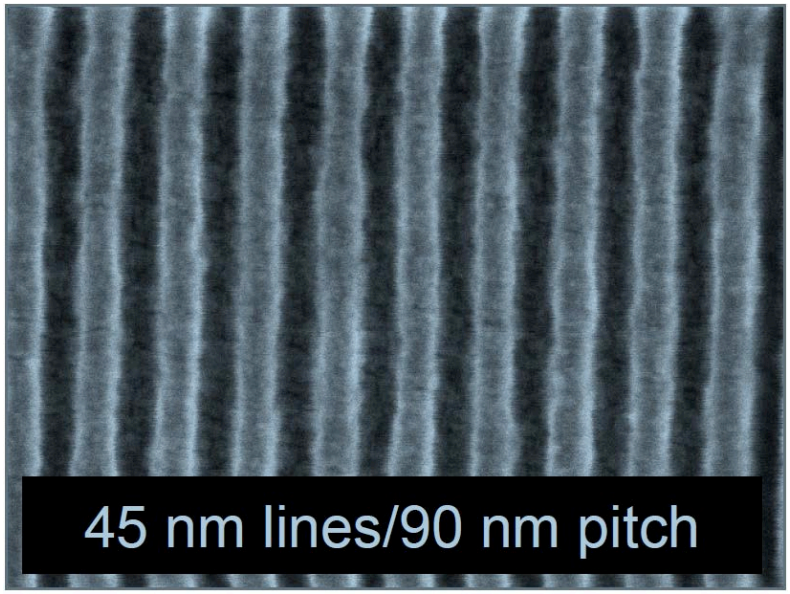




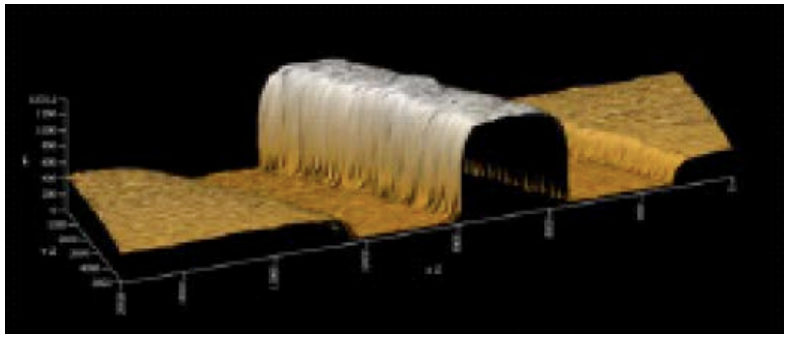
- Cover the simulation domain with the Si lattice
- Visit each lattice site and generate dopant with probability $p_i = N(x_i, y_i, z_i)\Delta V$ where $\Delta V = a_{Si}^3/8$ is the volume associated with each Si atom
- Assign the dopant to the surrounding grid nodes using cloud in a cell approach

A. Asenov et al.

LER in Simulation – Origins

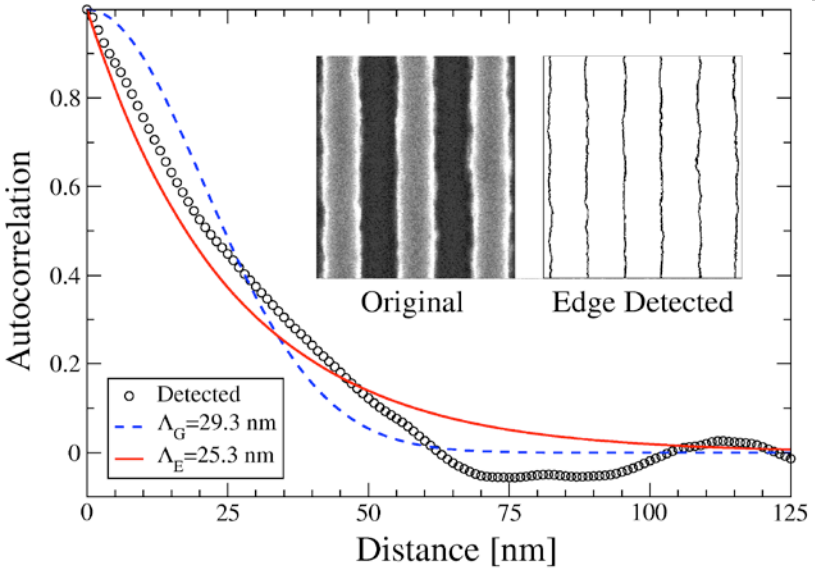


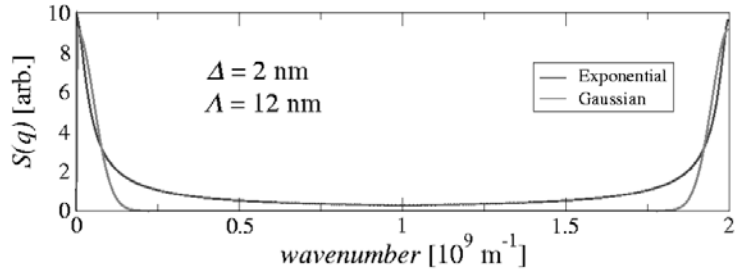
T. Brunner, ICP 2003

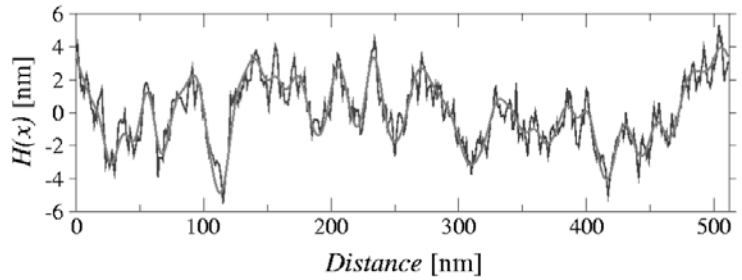


- Fluctuation in the total dose due to light quantisation.
- Fluctuation in photon absorption position.
- Nanoscale non-uniformities in resist composition.
- Statistical variation in the acid-catalysed de-protection.
- Statistical effects in polymer chain dissolution

LER in Simulation – Implementation







- A complex array of N elements is generated according to the power spectrum of the chosen autocorrelation function.

Gaussian

$$S_G(k) = \sqrt{\pi}\,\Delta^2\Lambda e^{-\frac{k^2\Lambda^2}{4}}$$

Exponential

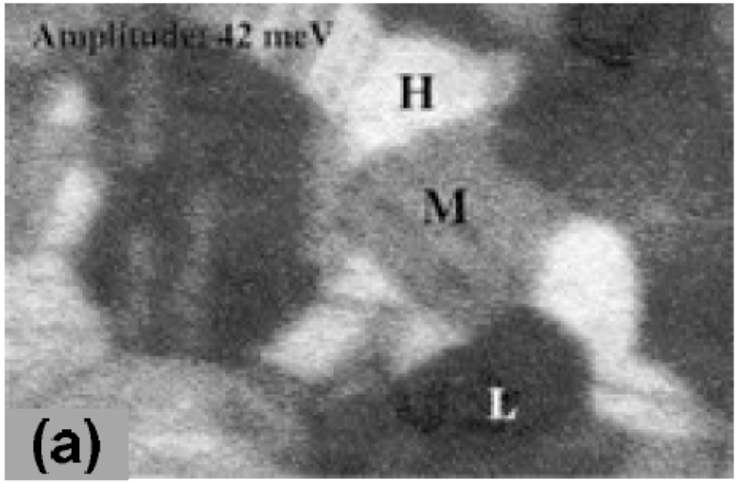
$$S_E(k) = \frac{2\Delta^2\Lambda}{1+k^2\Lambda^2}$$

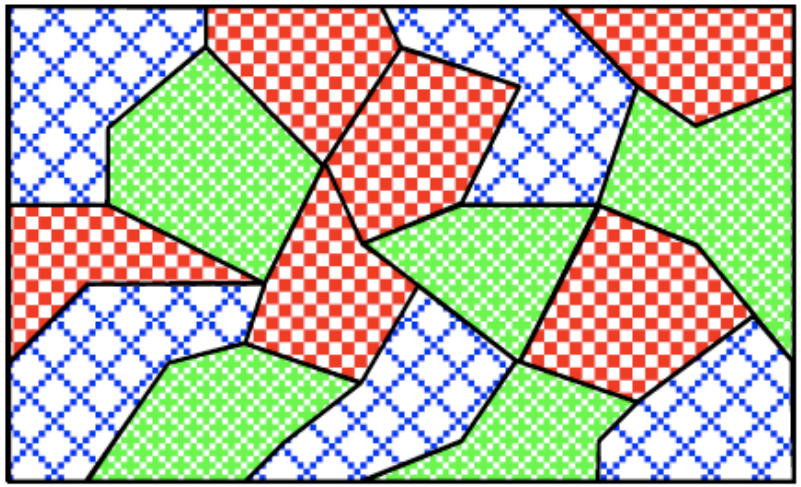
$$k = i\frac{2\pi}{N\,dx}$$

- The phase of the elements is chosen randomly. However only $(N/2-2)$ elements are independent.

A. Asenov et al. 2003

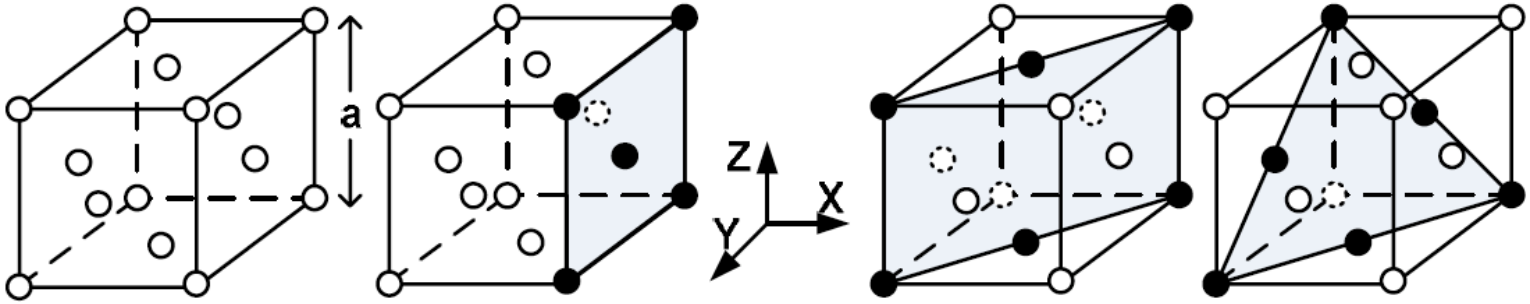
MGG in Simulation - Origins





$\Phi_{111}(L)>\Phi_{100}(M)>\Phi_{110}(H)$

Different surface density at different orientations



<100> <110> <111>

H. Dadgour et al.

MGG in Simulation – Implementation

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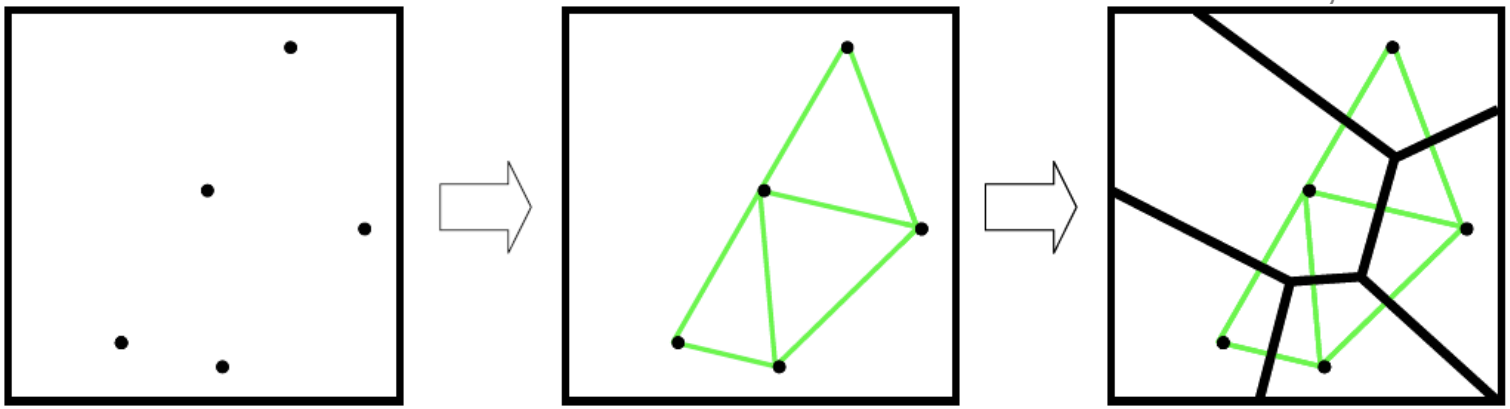
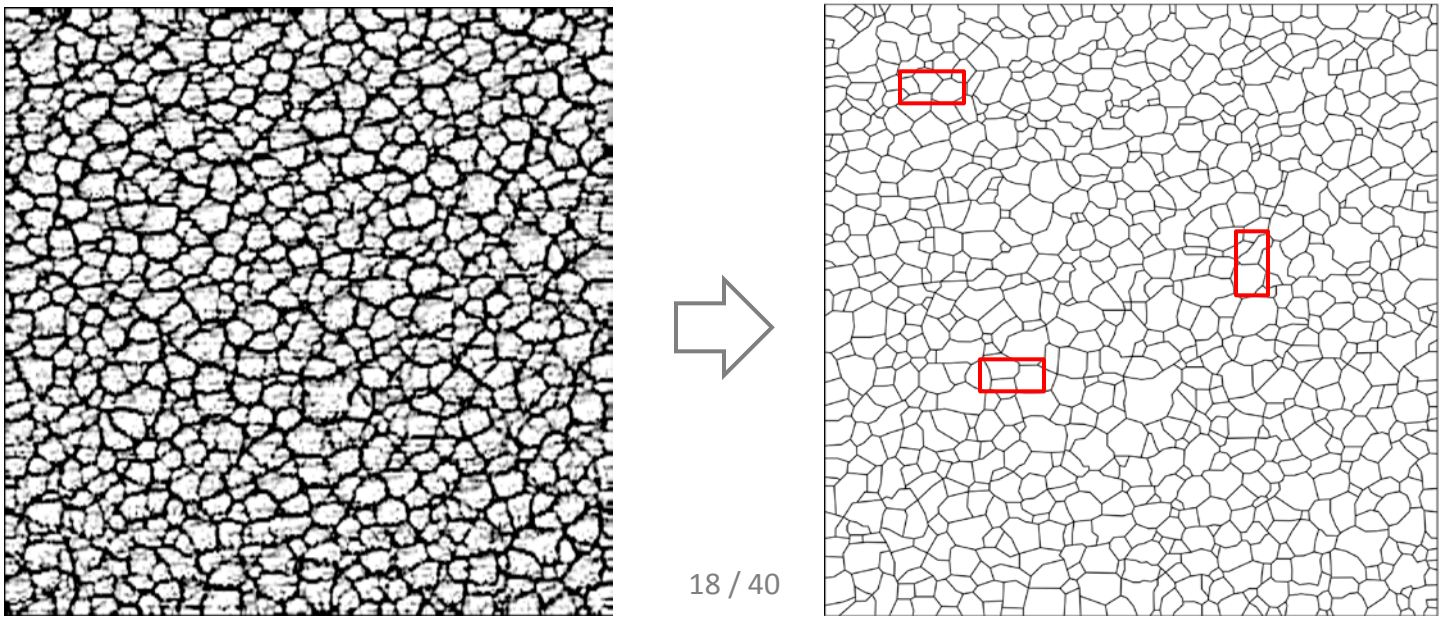
1. 3D Voronoi Geometric Tesselation

A.T. Putra, ISDRS 2007



2. Use of large interdigitise template

A. Brown



OUTLINE

1. Introduction
2. Modeling Methodology for variability
3. **Interplay of Process and Statistical Variability**
4. Conclusions

THE GSS SIMULATION TOOLCHAIN

Full simulation tool chain

- Structure Manipulation/Translation
  - Monolith
- Device Simulation GARAND
  - DD, 3D Full Band MC , 1D Multi-sub-band MC
- Statistical SPICE Modelling
  - Mystic –SPICE Model extraction
  - ModelGEN – Advanced process and statistical aware SPICE Model generation technology
- Circuit Simulation
  - RandomSPICE – Statistical Circuit Simulation Engine
- Toolchain integration
  - Enigma – Automation and Integration framework

SUPERTHEME 20NM MOSFET

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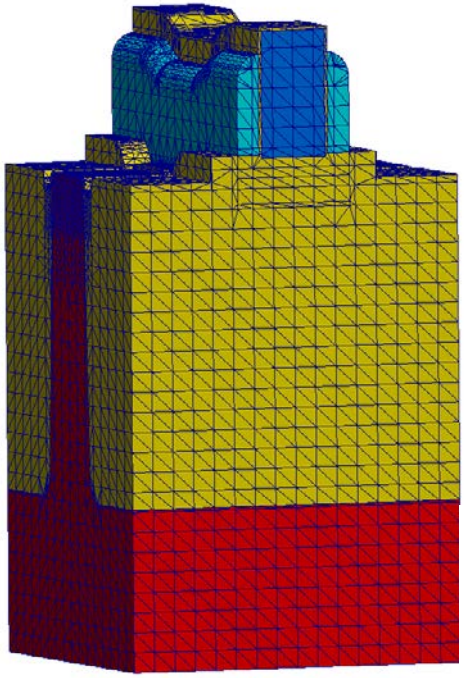
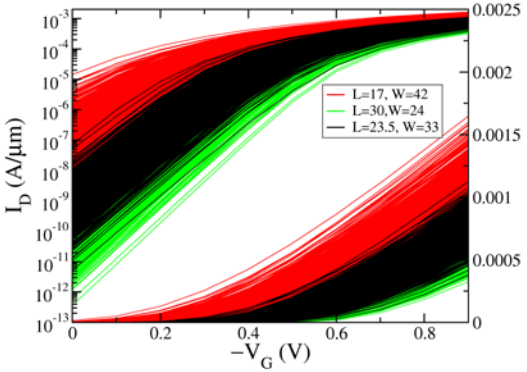
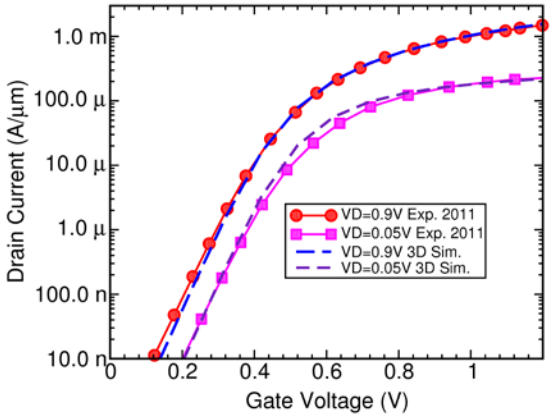
Nominal Device





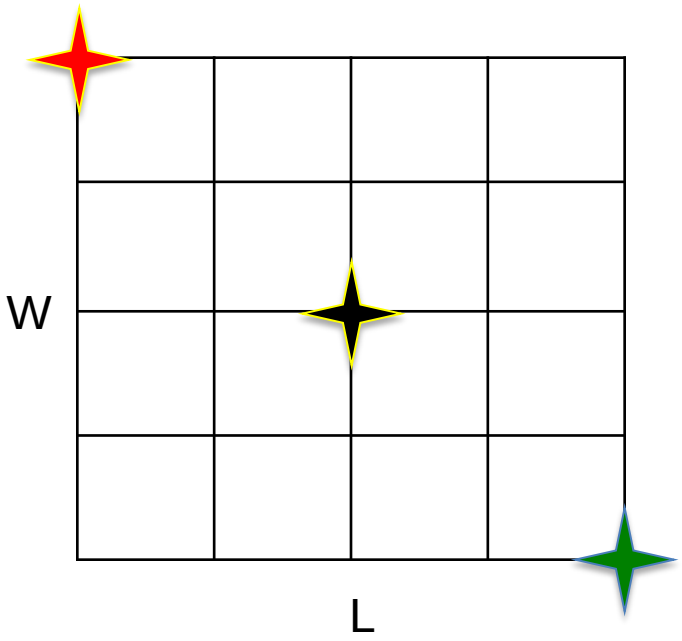


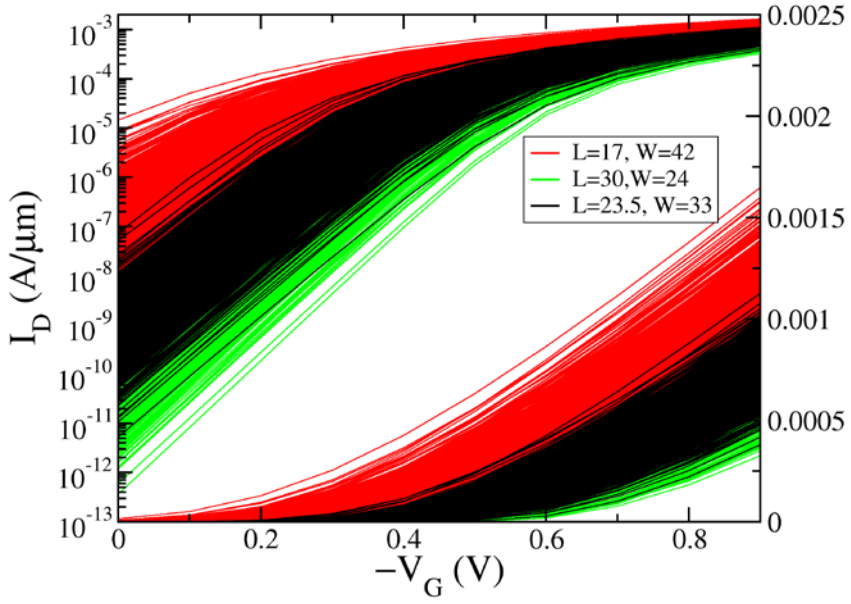
Process simulation
(DrLitho/Sentaurus Process)

Mesh Conversion/Transfer
(GSS Monolith)

Device simulation
(GSS Garand)

Design of Experiments - Interplay between PROCESS and STATISTICAL VARIABILITY





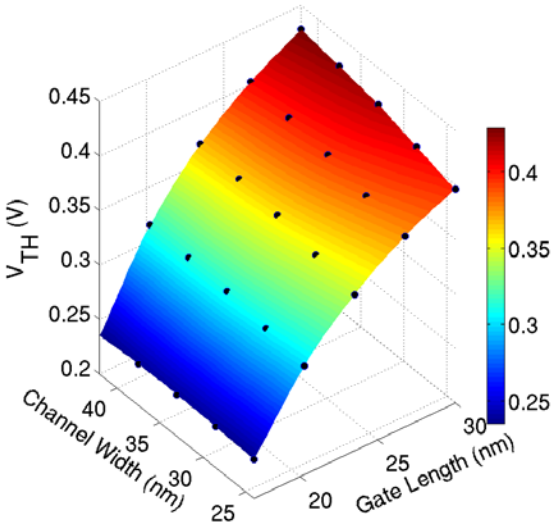
- RDD, LER, MGG
- L_G=17, 20.25, 23.5, 26.75, 30
- W=24, 28.5, 33, 37.5, 42
- 5 × 5 DoE space

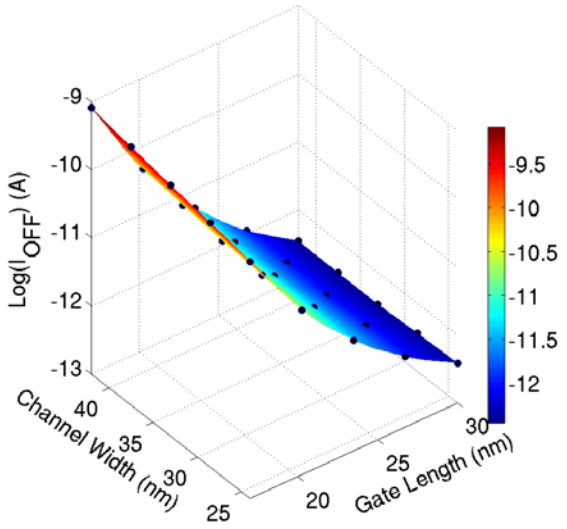
FAST CORNER

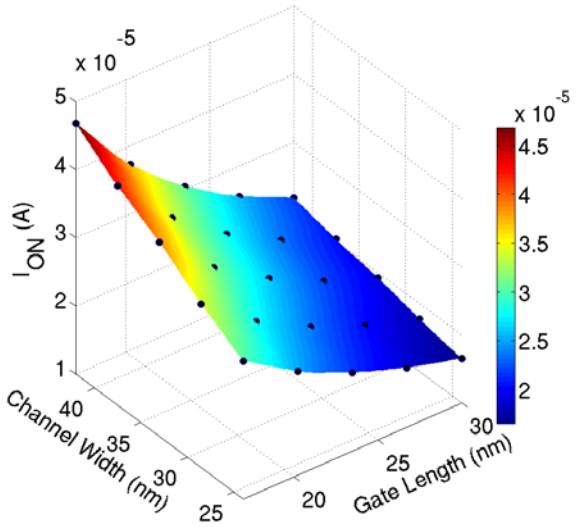
NOMINAL SILICON

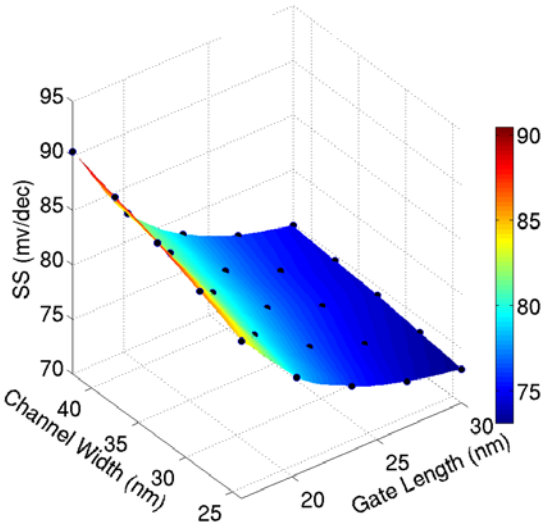
SLOW CORNER

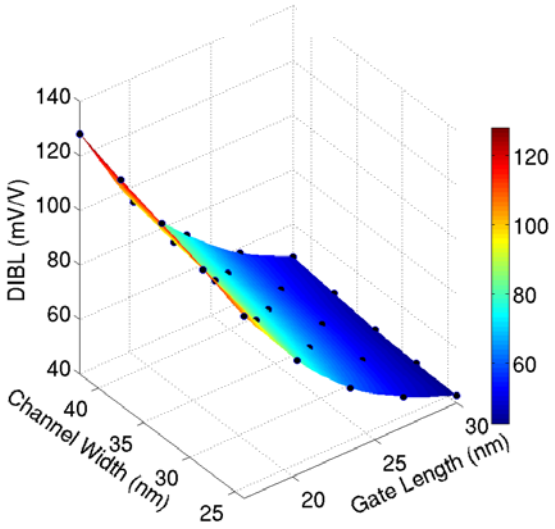
PROCESS VARIABILITY - NMOS



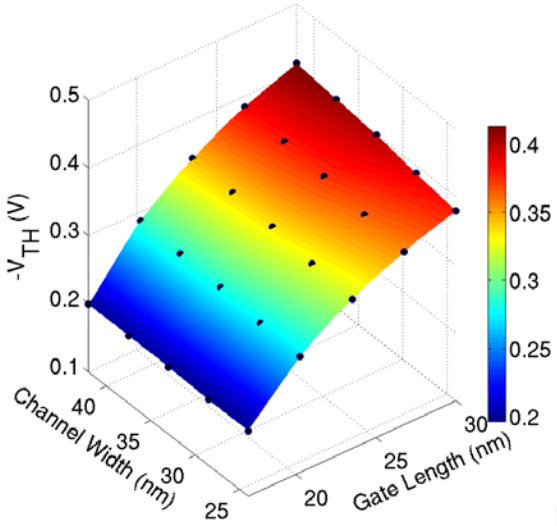


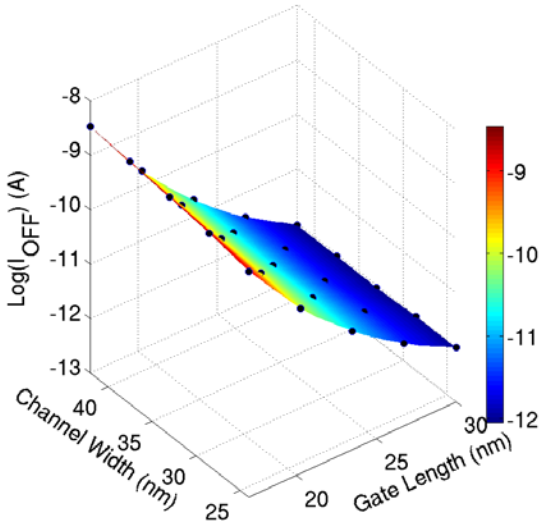


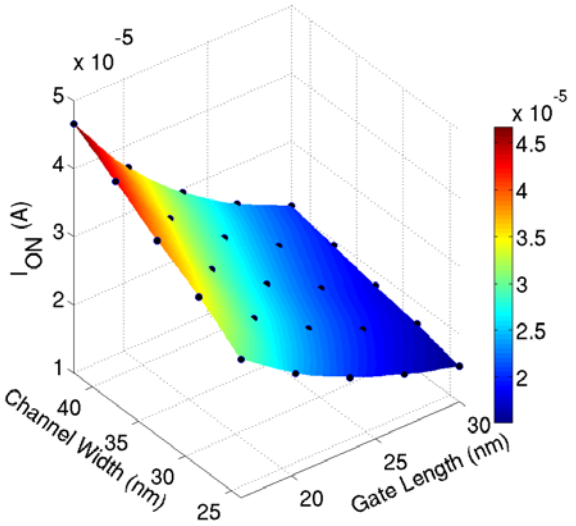


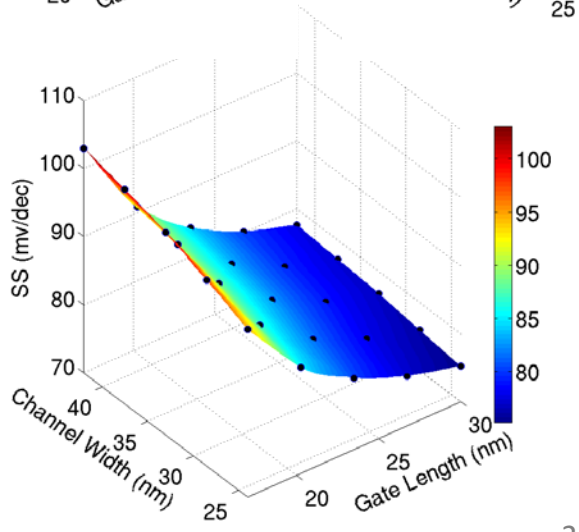


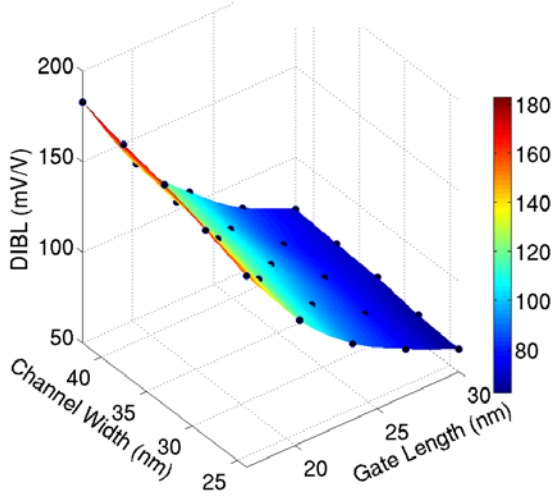
PROCESS VARIABILITY - PMOS



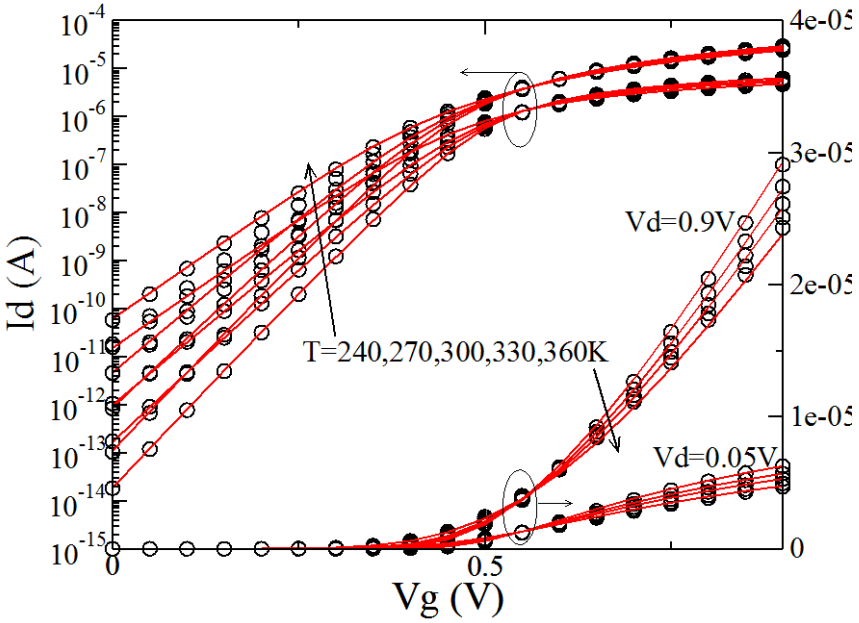




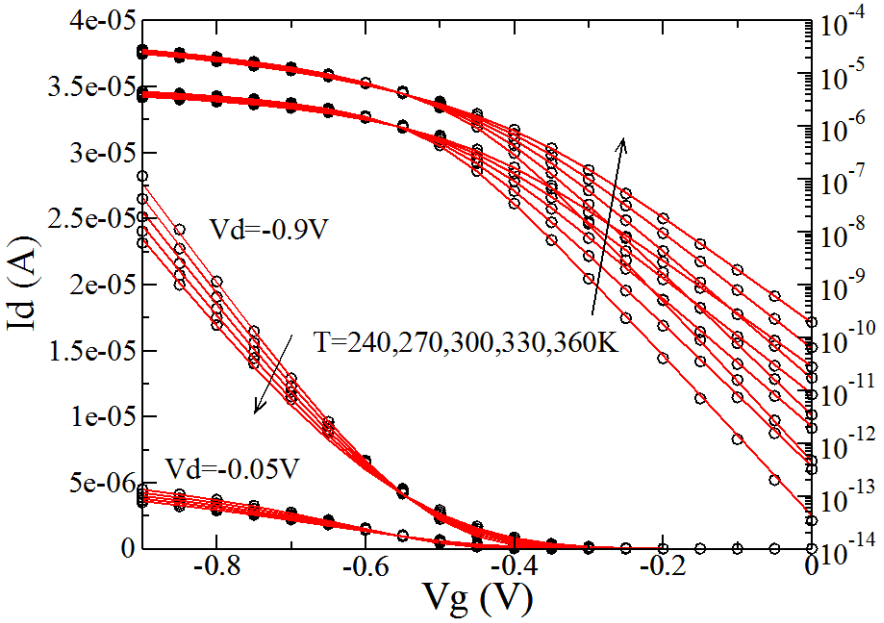




PROCESS VARIABILITY - Temperature



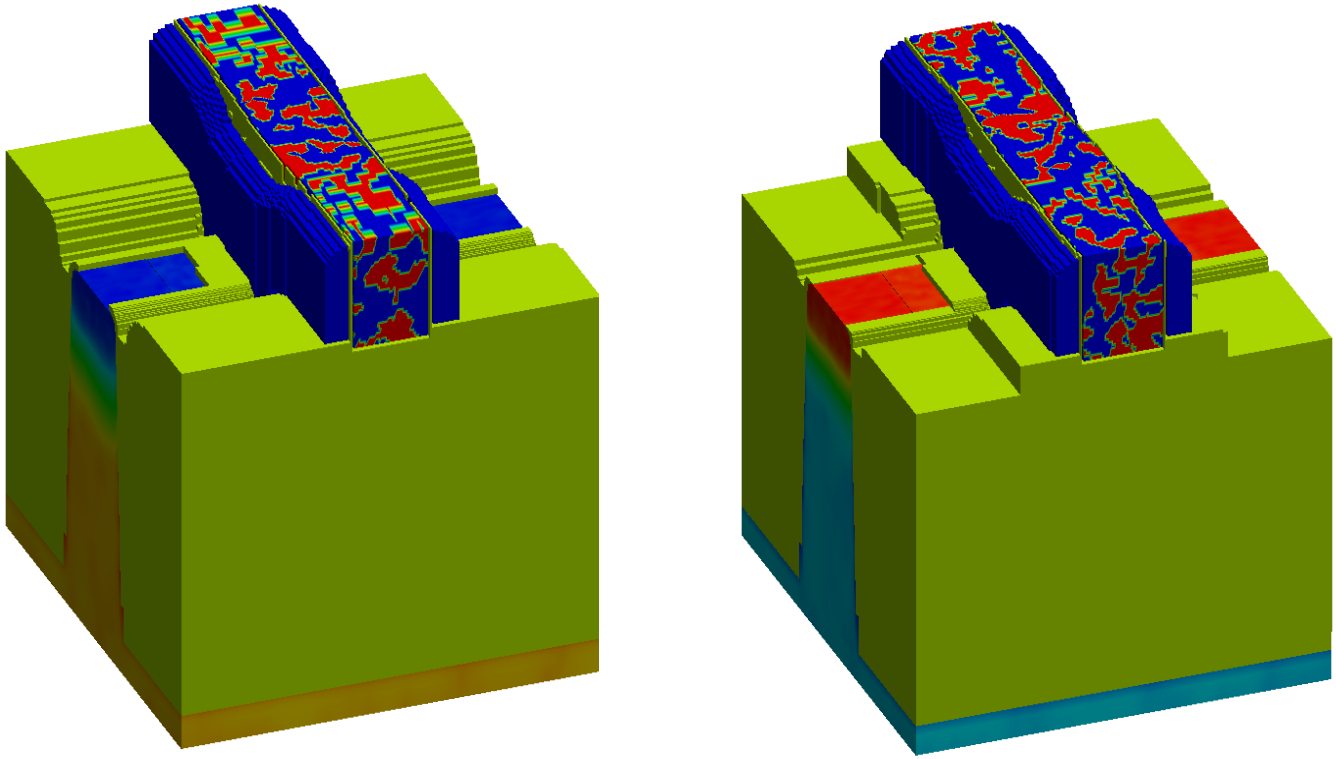
NMOS



PMOS

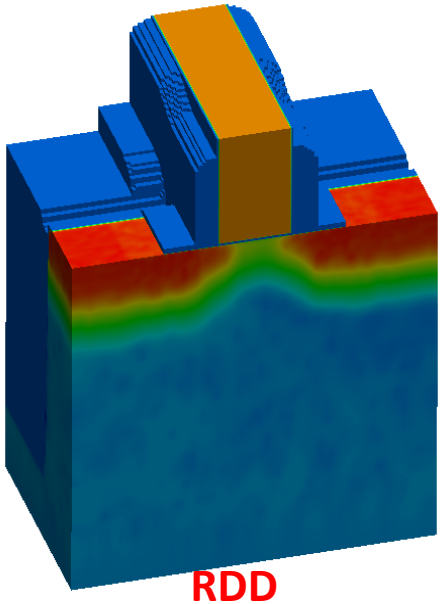
Temperature Variations are treated in the DoE in the same way as Process Variations

STATISTICAL VARIABILITY

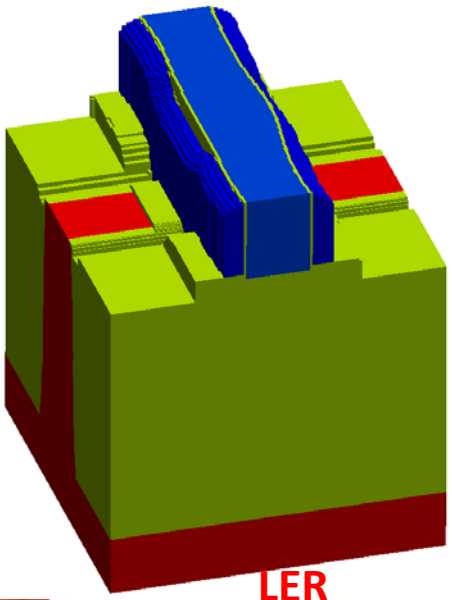


- Nominal L_G=23.5nm, W=33nm
- Realistic MOSFET structures: STI, gate stack
- RDD, LER, MGG variability on top of PROCESS variations

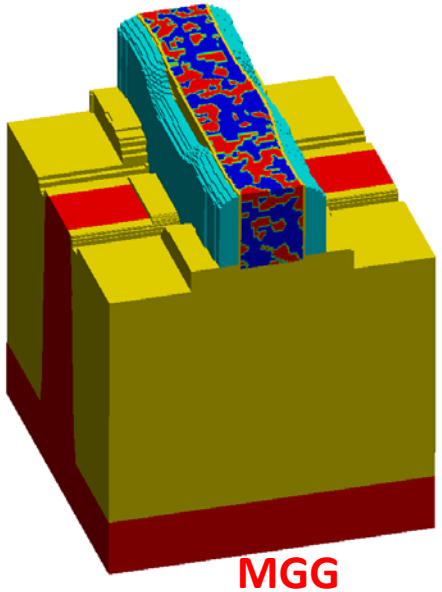
STATISTICAL VARIABILITY



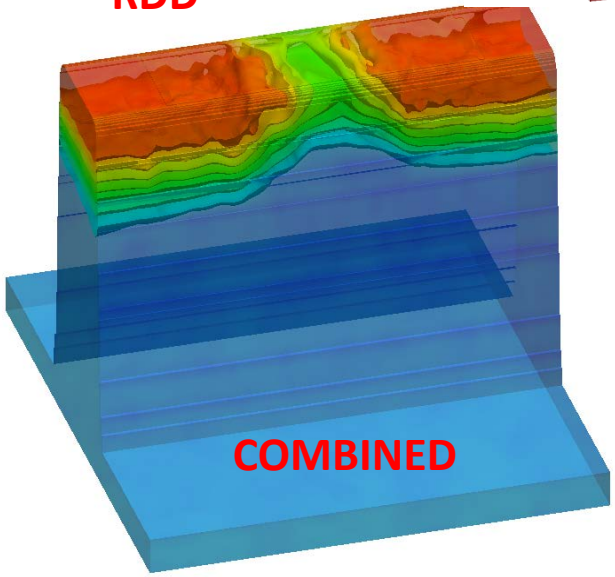
RDD



LER



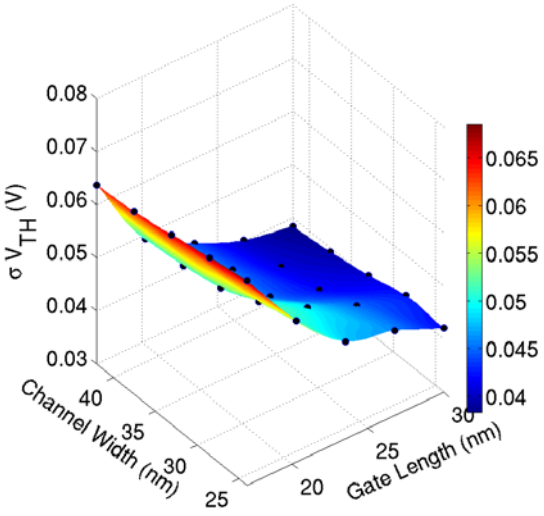
MGG

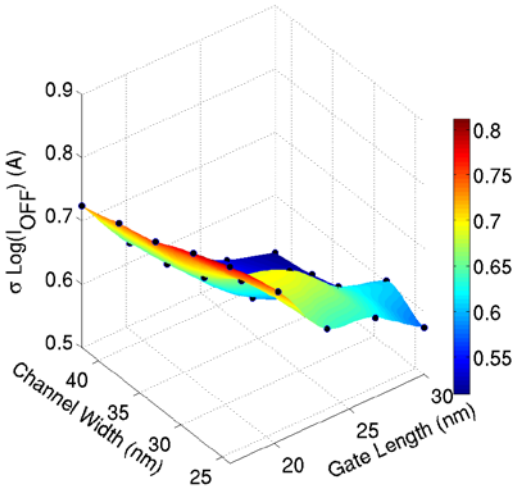


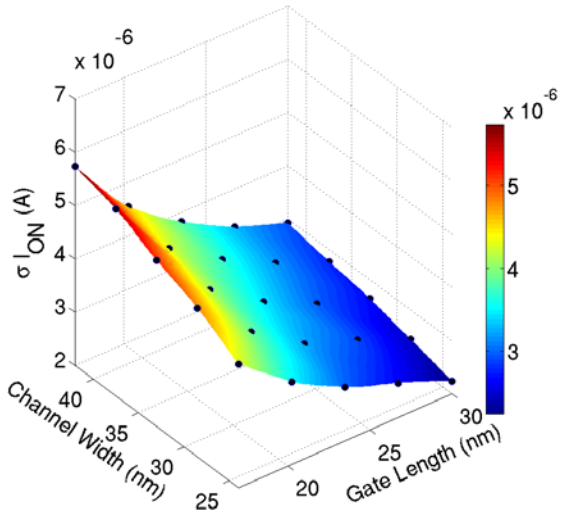
COMBINED

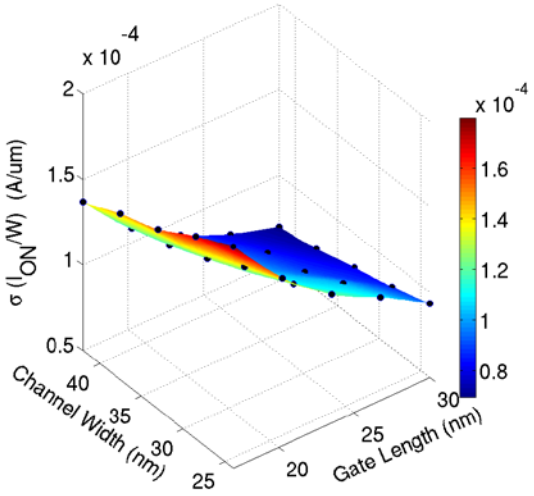
Impact of Single and Combined Variability Sources on Transistor Performance

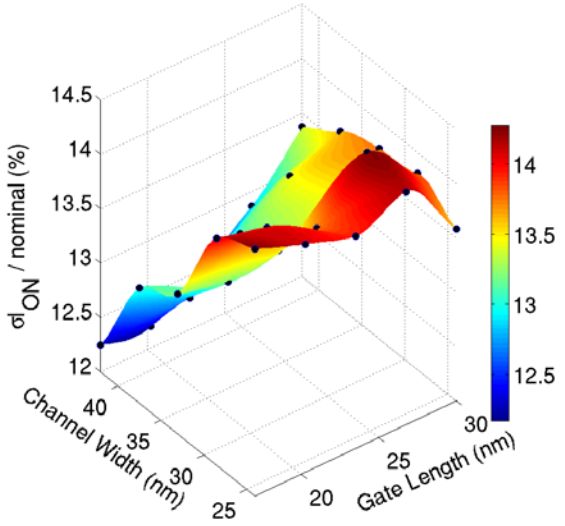
STATISTICAL VARIABILITY - NMOS



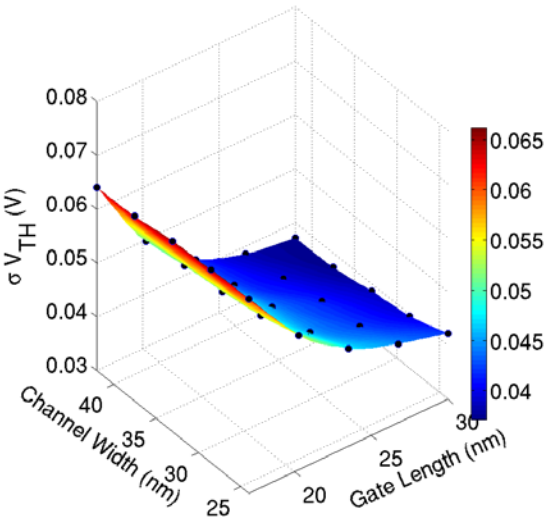


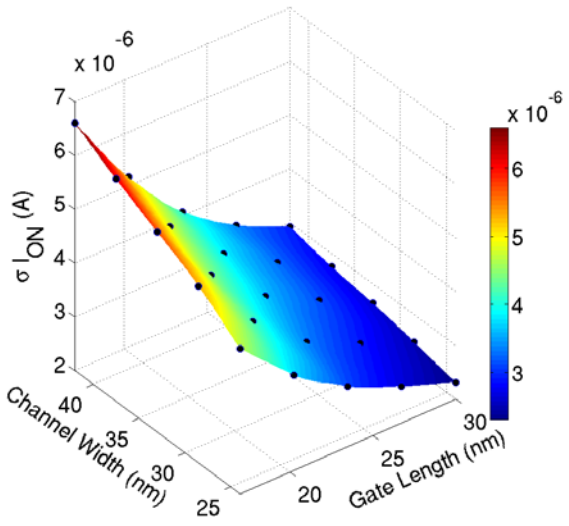


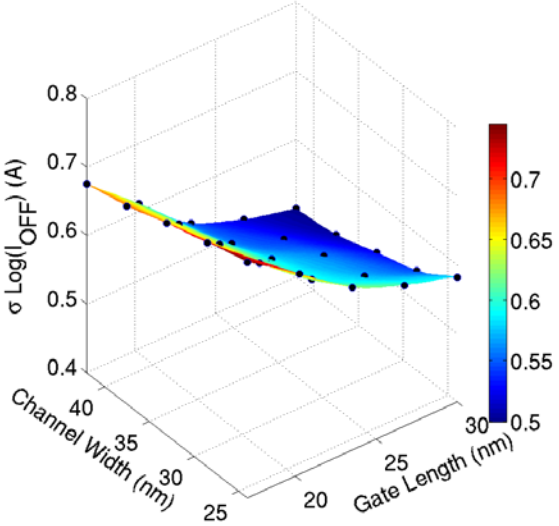


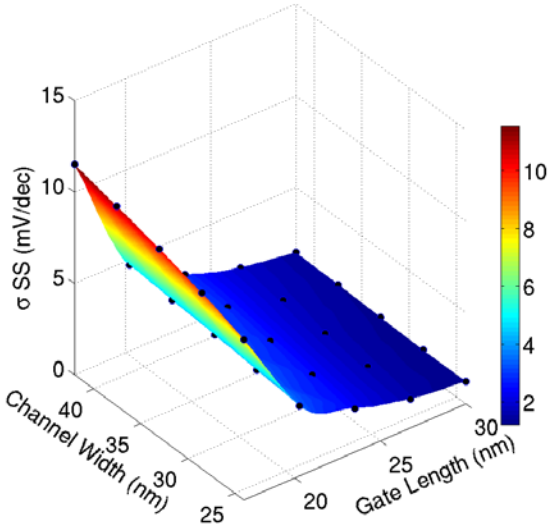


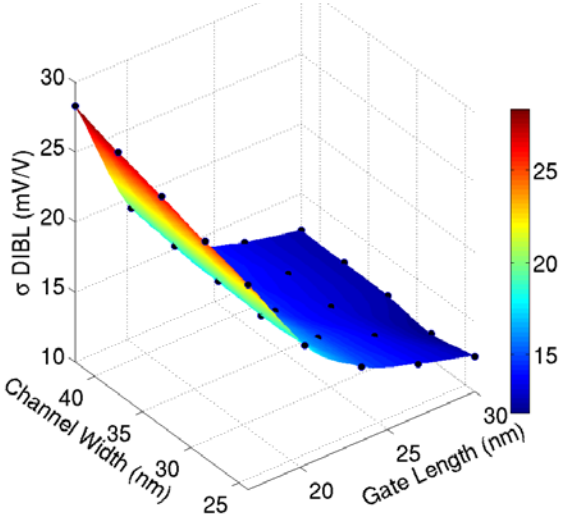
STATISTICAL VARIABILITY - PMOS



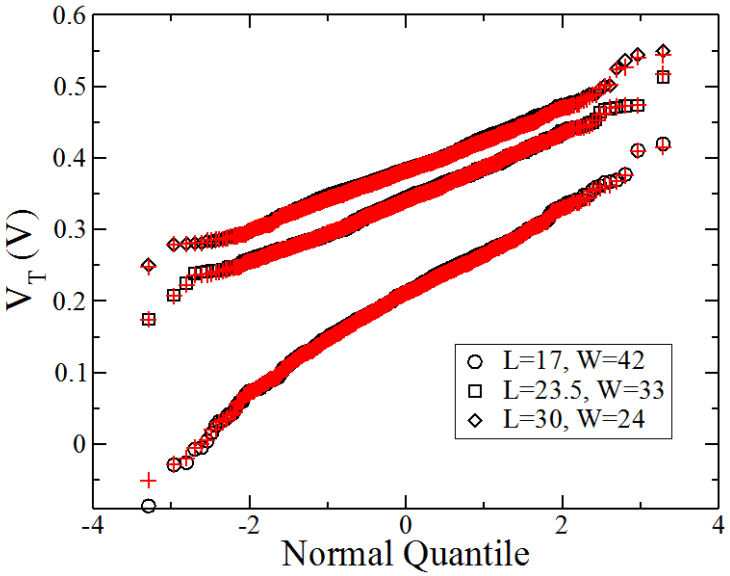




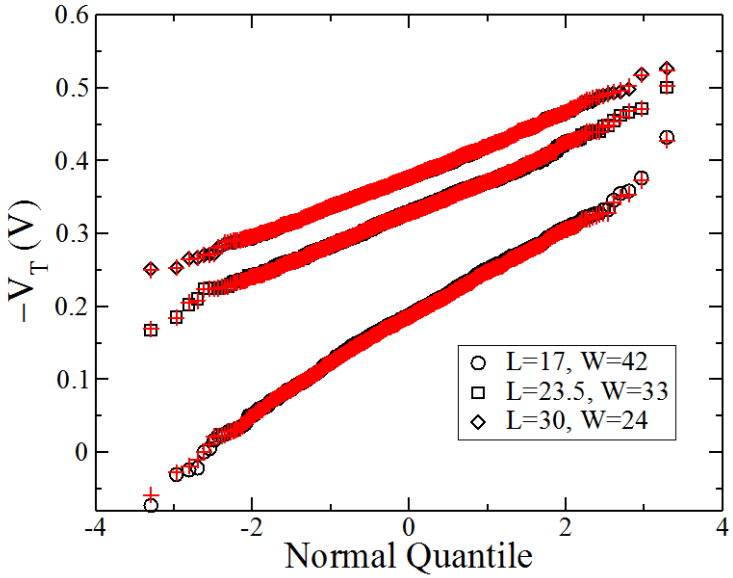




Remarks on the INTERPLAY of PROCESS and STATISTICAL VARIABILITY



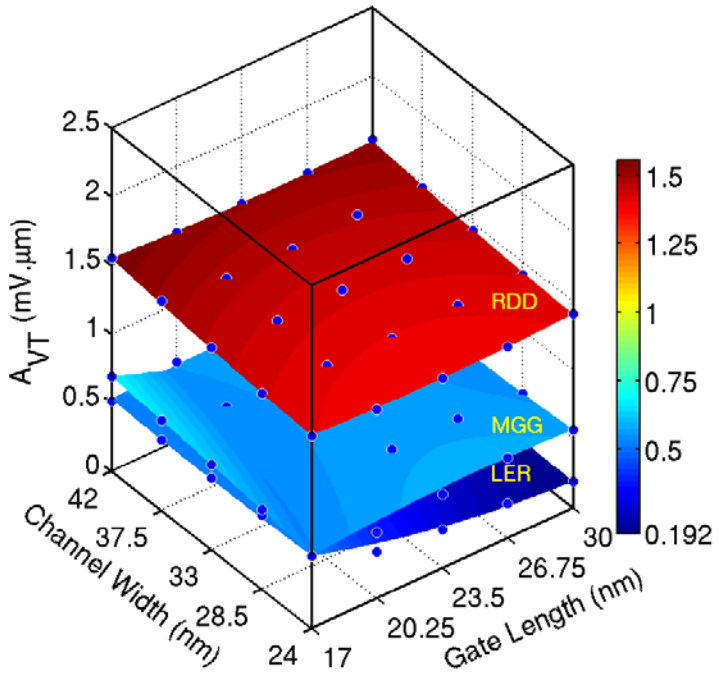
NMOS

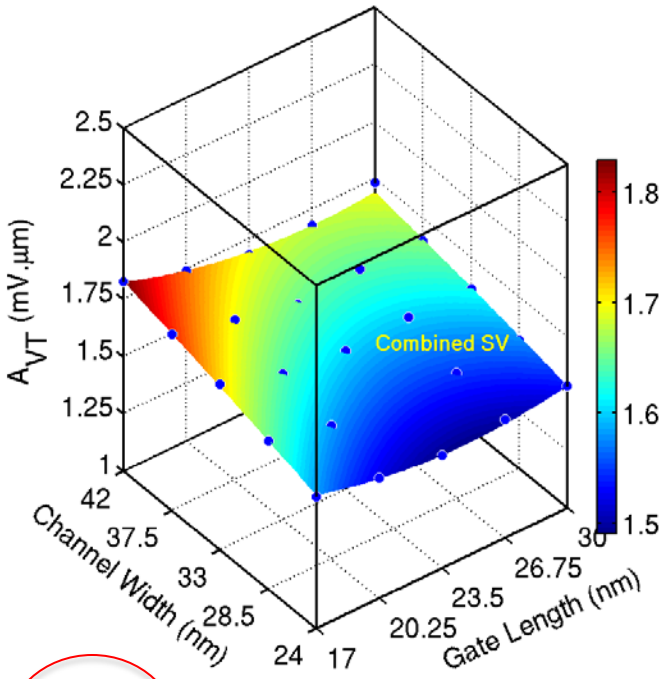


PMOS

Process Variations DO NOT only induce shifts in the AVERAGE Performance BUT they also change the sensitivity to STATISTICAL Dispersion

Remarks on the INTERPLAY of PROCESS and STATISTICAL VARIABILITY





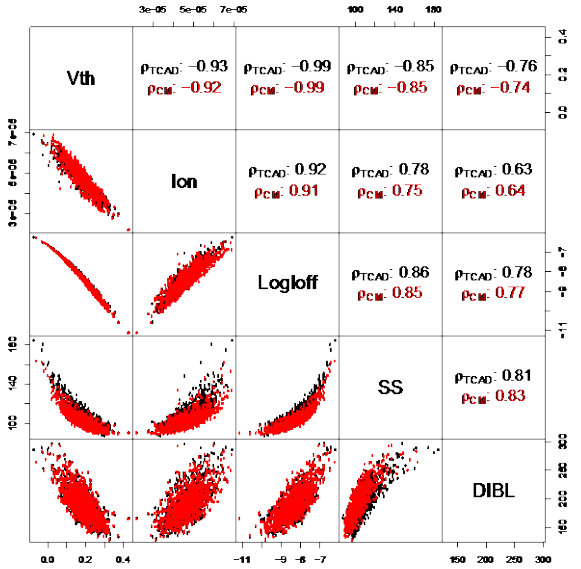
STATISTICAL VARIABILITY

$$\sigma V_T = \frac{A_{VT}}{\sqrt{2WL}}$$

MOSFET MISMATCH

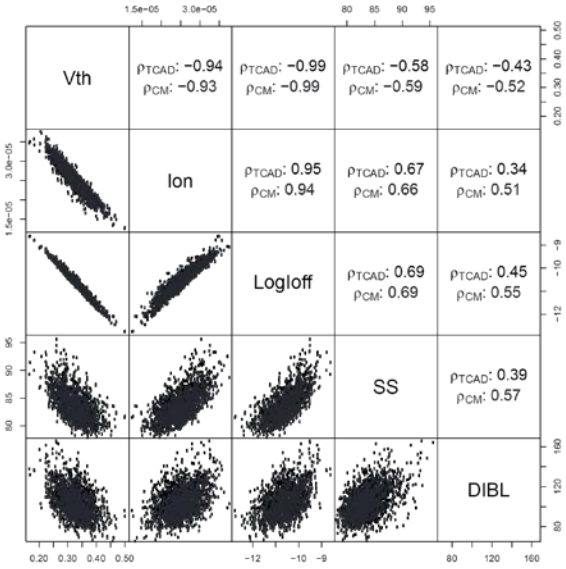
Process Variations DO NOT only induce shifts in the AVERAGE Performance BUT they also change the sensitivity to STATISTICAL Dispersion

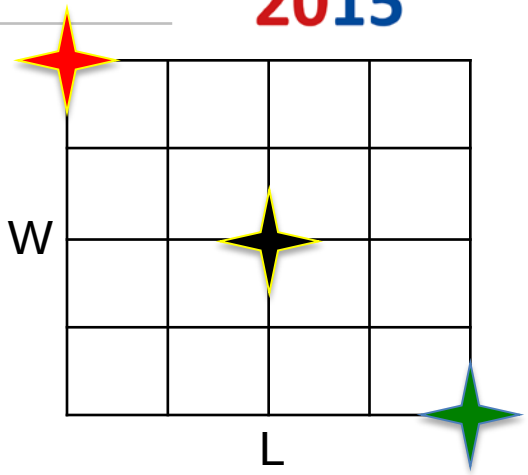
Remarks on the INTERPLAY of PROCESS and STATISTICAL VARIABILITY



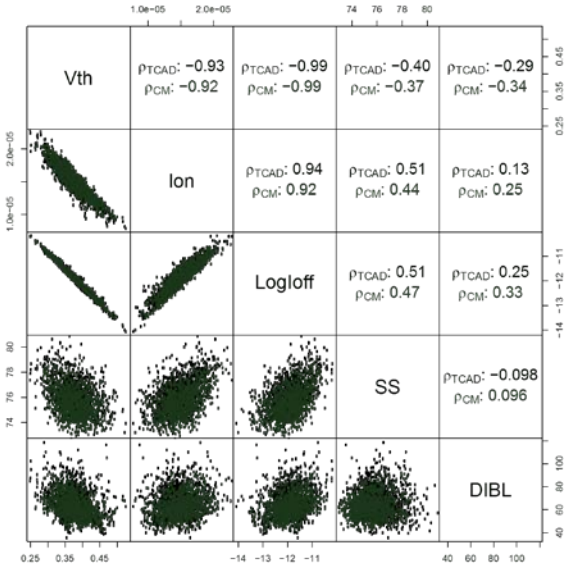
FAST CORNER

NOMINAL SILICON





SLOW CORNER



<u>Process Variations</u> DO NOT only induce shifts in the AVERAGE Performance

BUT they also change the <u>correlation between FOMs</u>

HIERARCHICAL VARIABILITY AWARE SIMULATION METHODOLOGY

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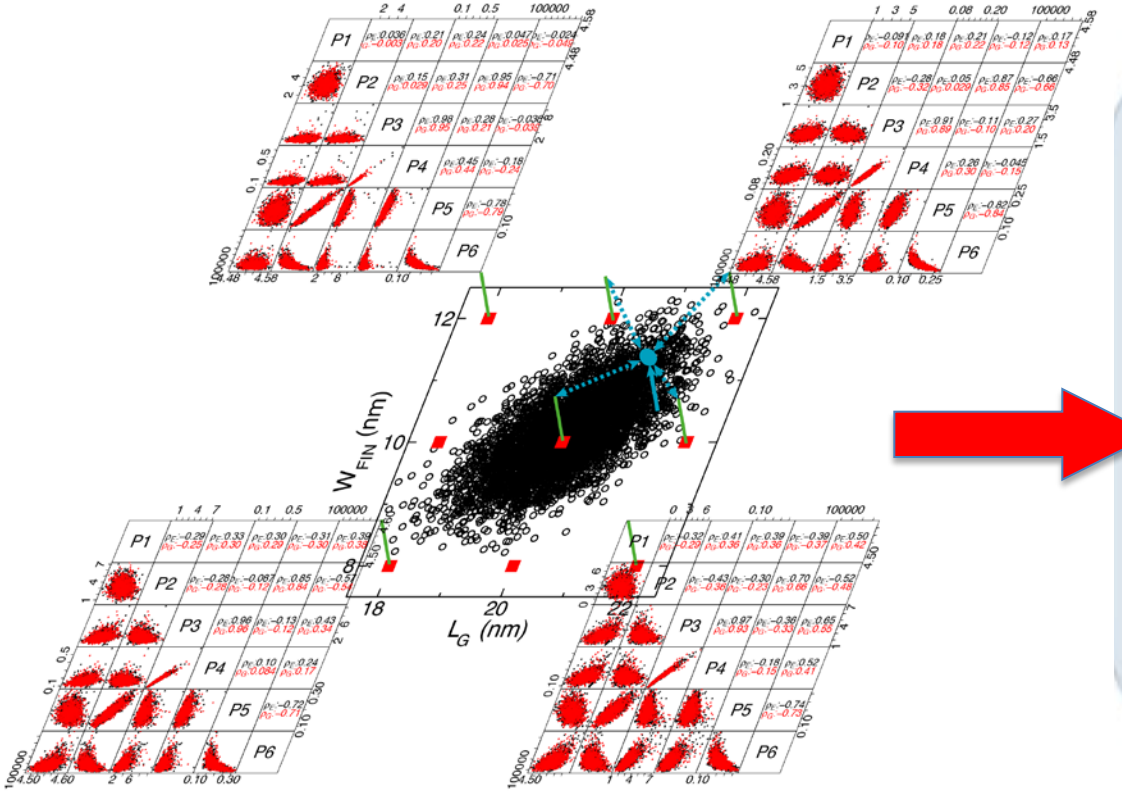

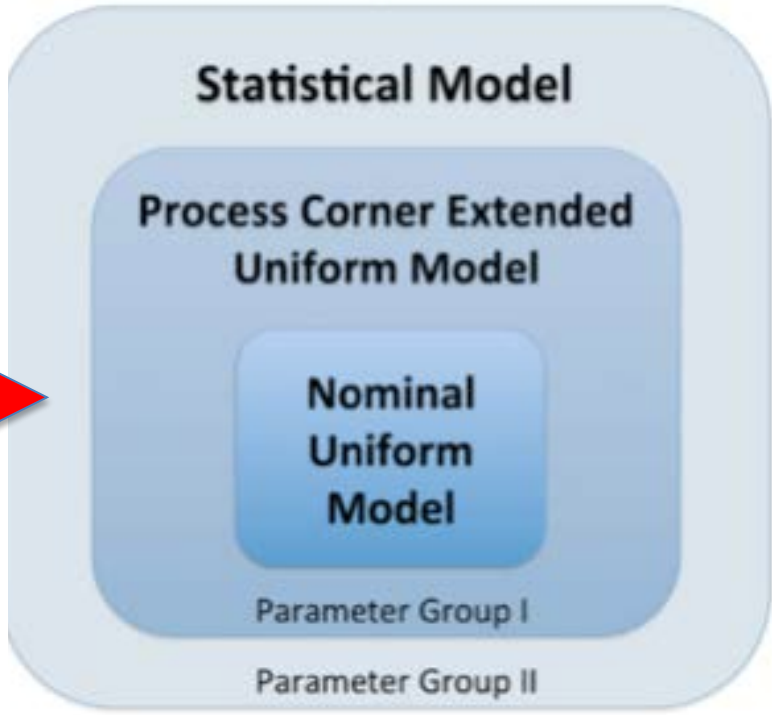

DEVICE to CIRCUIT Hierarchical Simulation

TCAD-based Design-Technology Co-Optimization (DTCO)

OUTLINE

1. Introduction
2. Modeling Methodology for variability
3. Interplay of Process and Statistical Variability
4. **Conclusions**

CONCLUSIONS

- VARIABILITY is a maker or breaker of advanced MOSFET technology.
- Accounting for both PROCESS and STATISTICAL variability (and their interplay) is mandatory for optimizing design margins and developing predictive early-stage PDKs.
- A fully integrated and hierarchical SIMULATION methodology must be adopted to enable a cost-effective DTCO and to shrink time-to-market.

Ben Kaczer, imec

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HIERARCHICAL MODELING OF RELIABILITY AND TIME DEPENDENT VARIABILITY IN THE MORV PROJECT

Conference Sponsors:

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PROJECT MOTIVATION

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- Scope: Timing analysis of complex circuits with aging effects

- State of the art: timing analysis performed using aged liberty files
- With this approach
  - Local, per-node parameters (activity, temperature, voltage), i.e., actual workloads, are not considered
  - As a consequence, timing analysis is pessimistic

- Objective : to develop timing flow aware of per-gate instance parameters
- Benefits :
  - Greater accuracy
  - Reduced pessimism

PROJECT BACKGROUND

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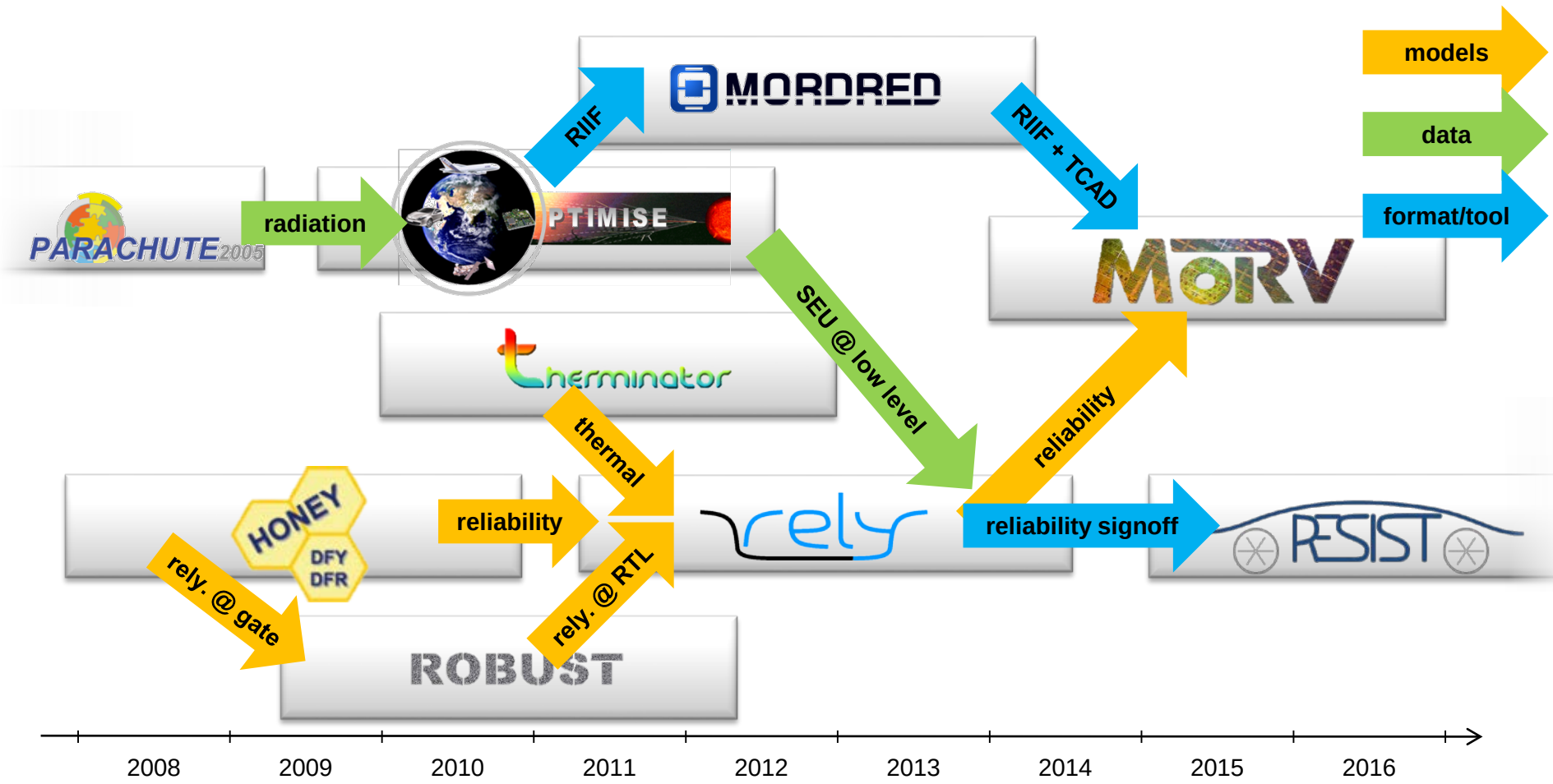

ABSTRACTION HIERARCHY

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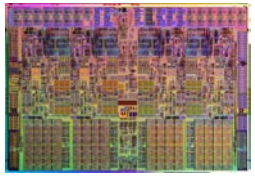
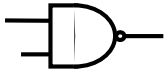
ESL



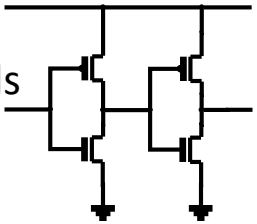
HDL/RTL

ALU

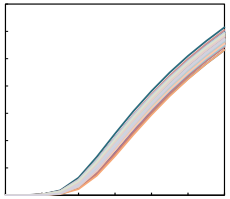
Gates



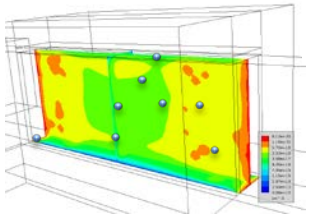
Circuits



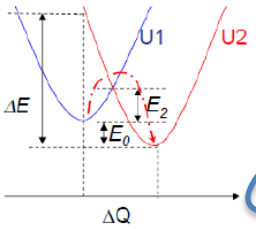
Compact models



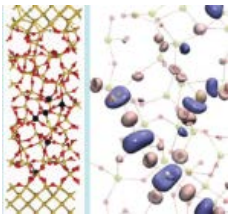
Device transport



Trap kinetics



1st principles



MORDRED

MoRV

OUTLINE

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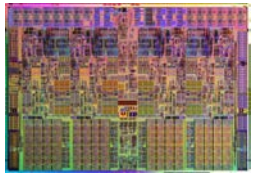
ESL



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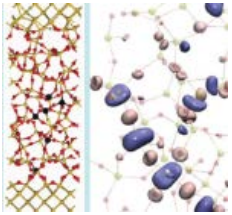
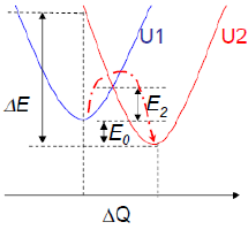
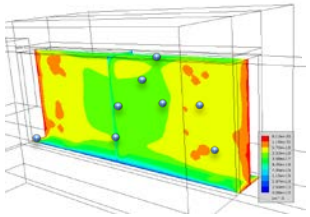
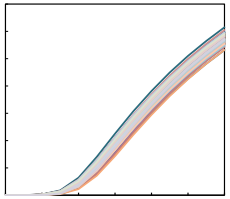
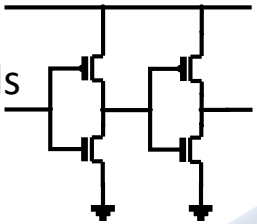
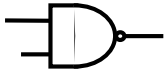












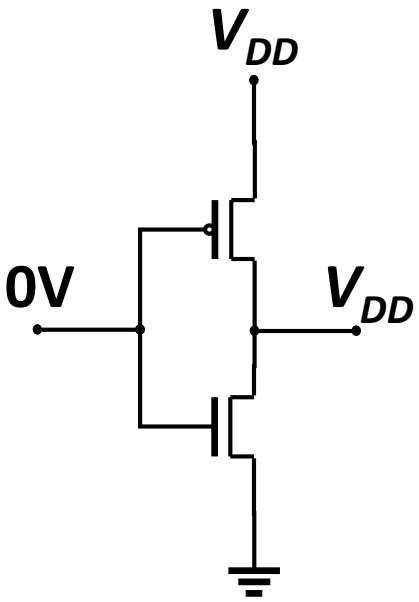
2

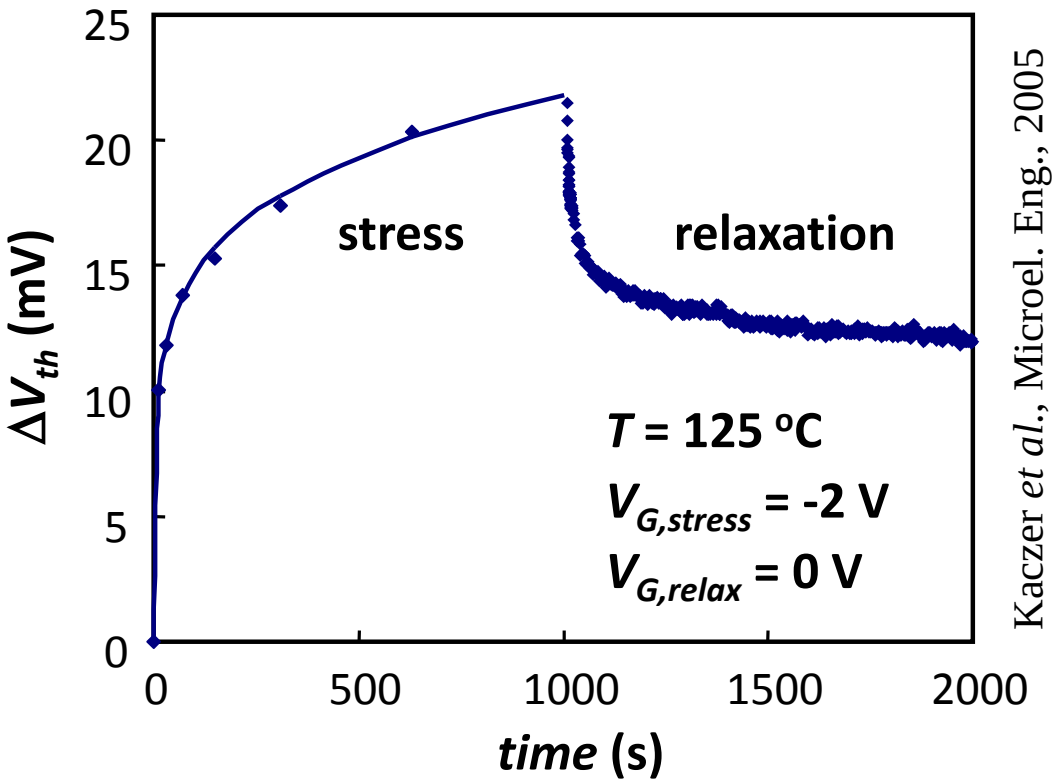
1

BIAS AND TEMPERATURE STRESS: TYPICAL DURING FET OPERATION

ESSCIRC ESSDERC 2015

Example: PFET V_{th} at **N**egative gate **B**ias (and typically at elevated **T**emperature) starts shifting (shows **I**nstability) → **NBTI**





Charging of preexisting and fabricated interface and oxide defects

→ ΔV_{th} and $\Delta\mu$

DEEPLY-SCALED DEVICES: INDIVIDUAL EMISSION EVENTS VISIBLE IN NBTI RELAXATION TRACES

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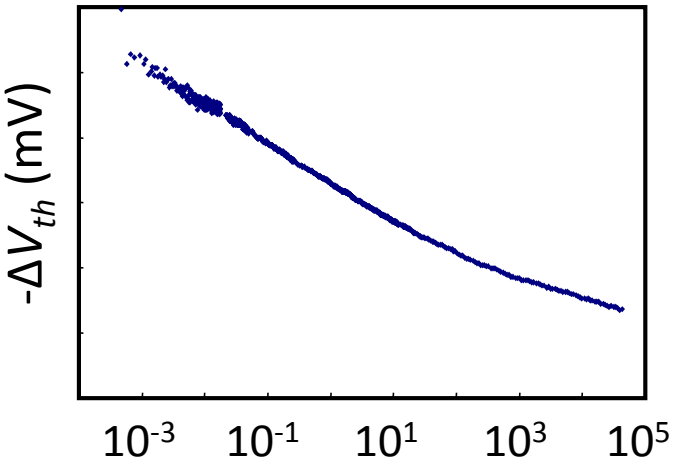
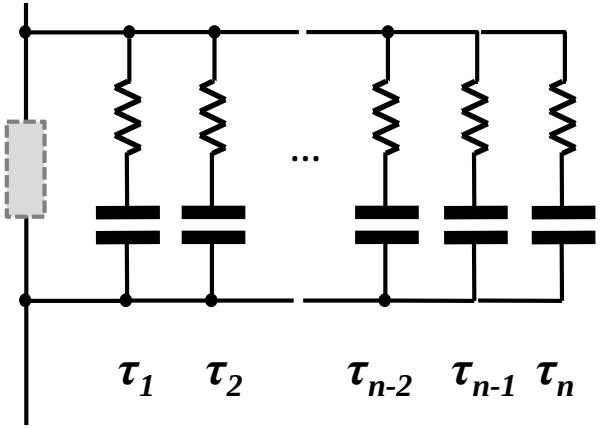
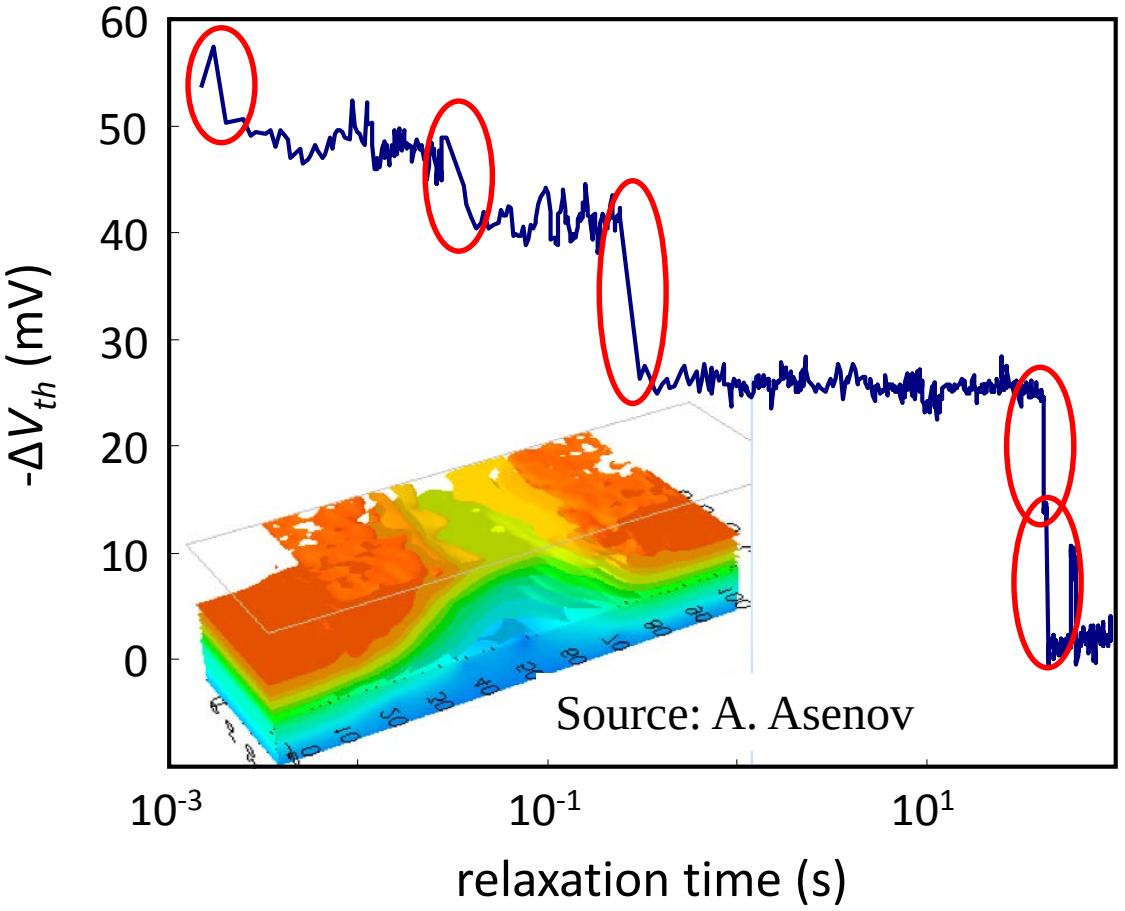
Large pFET



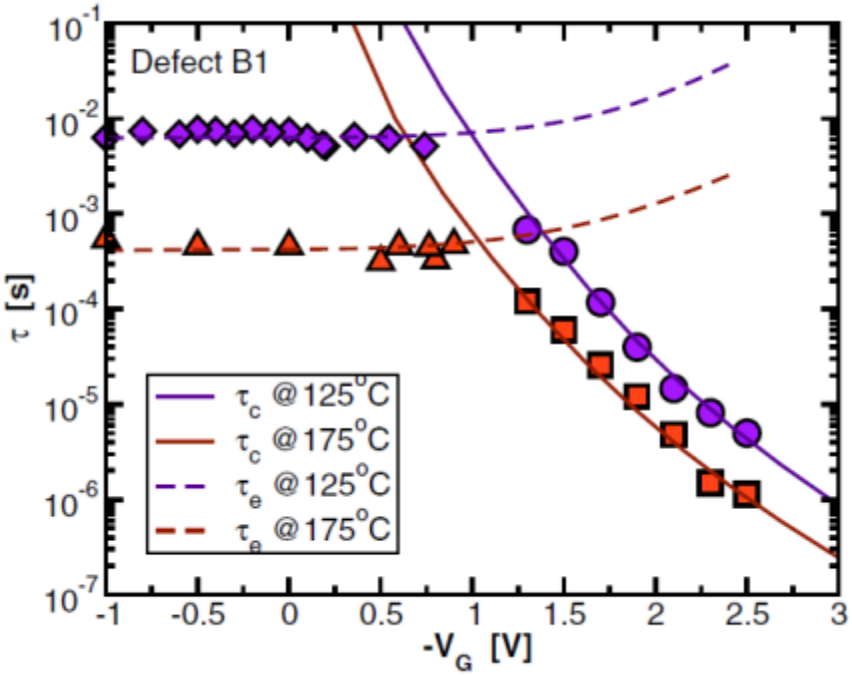


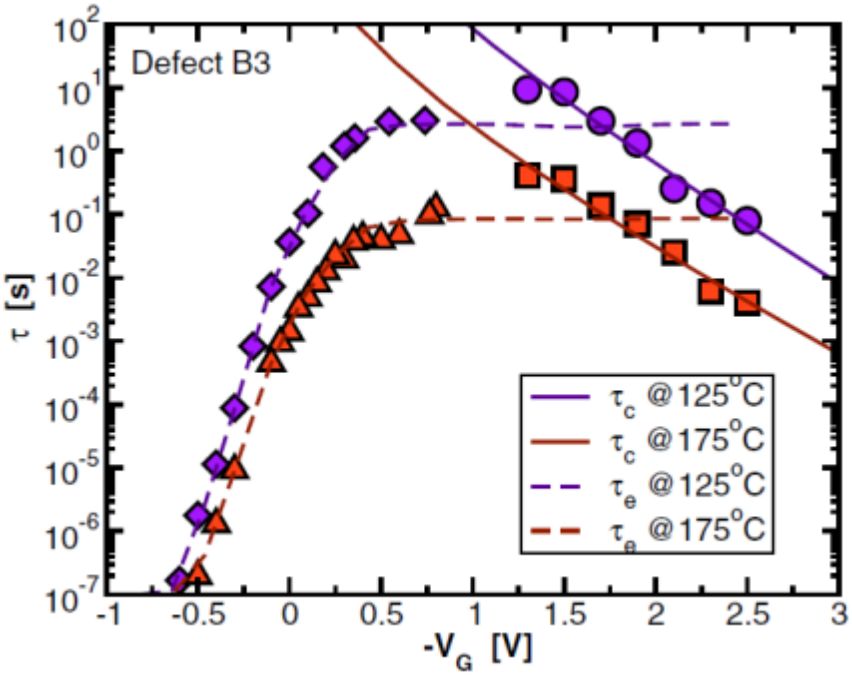
70 × 90 nm² pFET



Kaczer *et al.*, IRPS 2009

TRAP CONSTANTS *V* AND *T* DEPENDENT, DIFFERENT FOR EVERY TRAP





Grasser *et al.*, IRPS 2013

We need to know the **distributions of τ_c(V,T) and τ_e(V,T)**

8

TRAPPING (CAPTURE) AND DETRAPPING (EMISSION): 2-STEP PROCESSES

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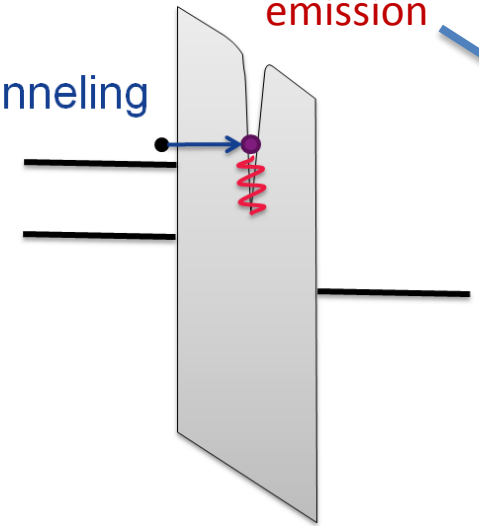
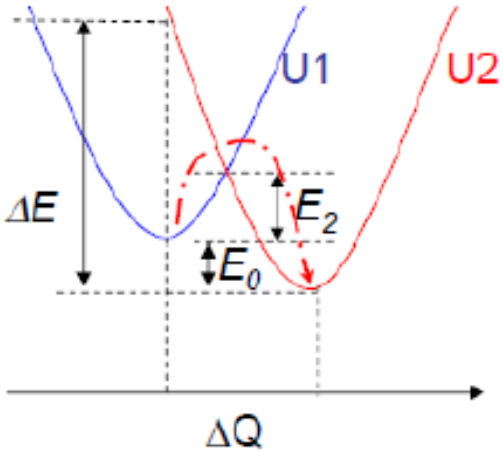
Structural relaxation + phonon emission

$$k_f = \frac{2\pi\rho_M(E_F)}{h}\left[\frac{\pi}{\lambda k_B T}\right]^{1/2}\int_{-\infty}^{\infty}[H_{DA}(\epsilon)]^2 \times \exp\left[-\frac{(\lambda + (E_{app} - E^\circ)e - \epsilon)^2}{4\lambda k_B T}\right] f(\epsilon)\, d\epsilon$$

Tunneling





DESCRIPTION OF DEFECTS

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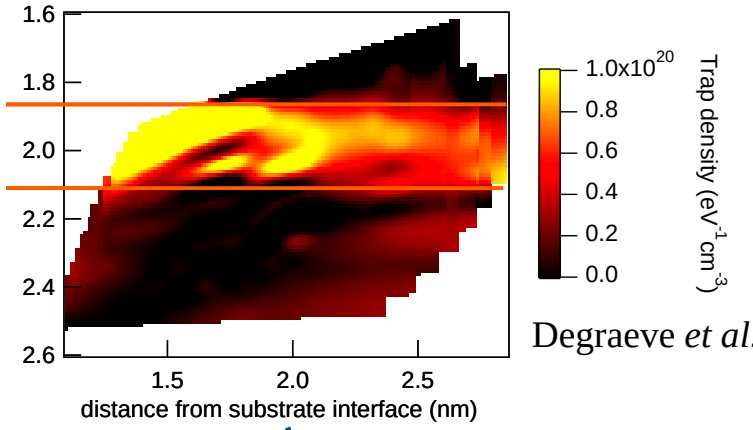
Defects characterized by **distributed** properties:

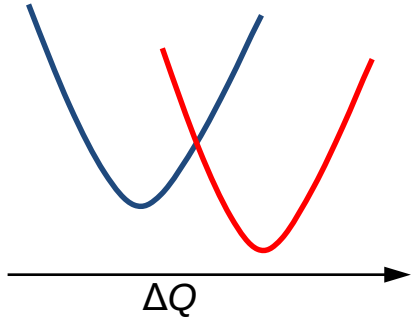
- Energy
  - wrt band gap
  - Structural
- Position in oxide
- Impact on device



Degraeve *et al.*

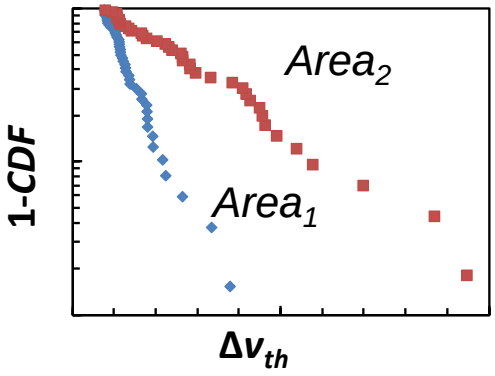
Adopted approach:

- **Discrete defects** (e.g., Sdevice: discrete solution of Grasser, Kaczer *et al.*, IRPS 2009)
- Properties taken from above distributions

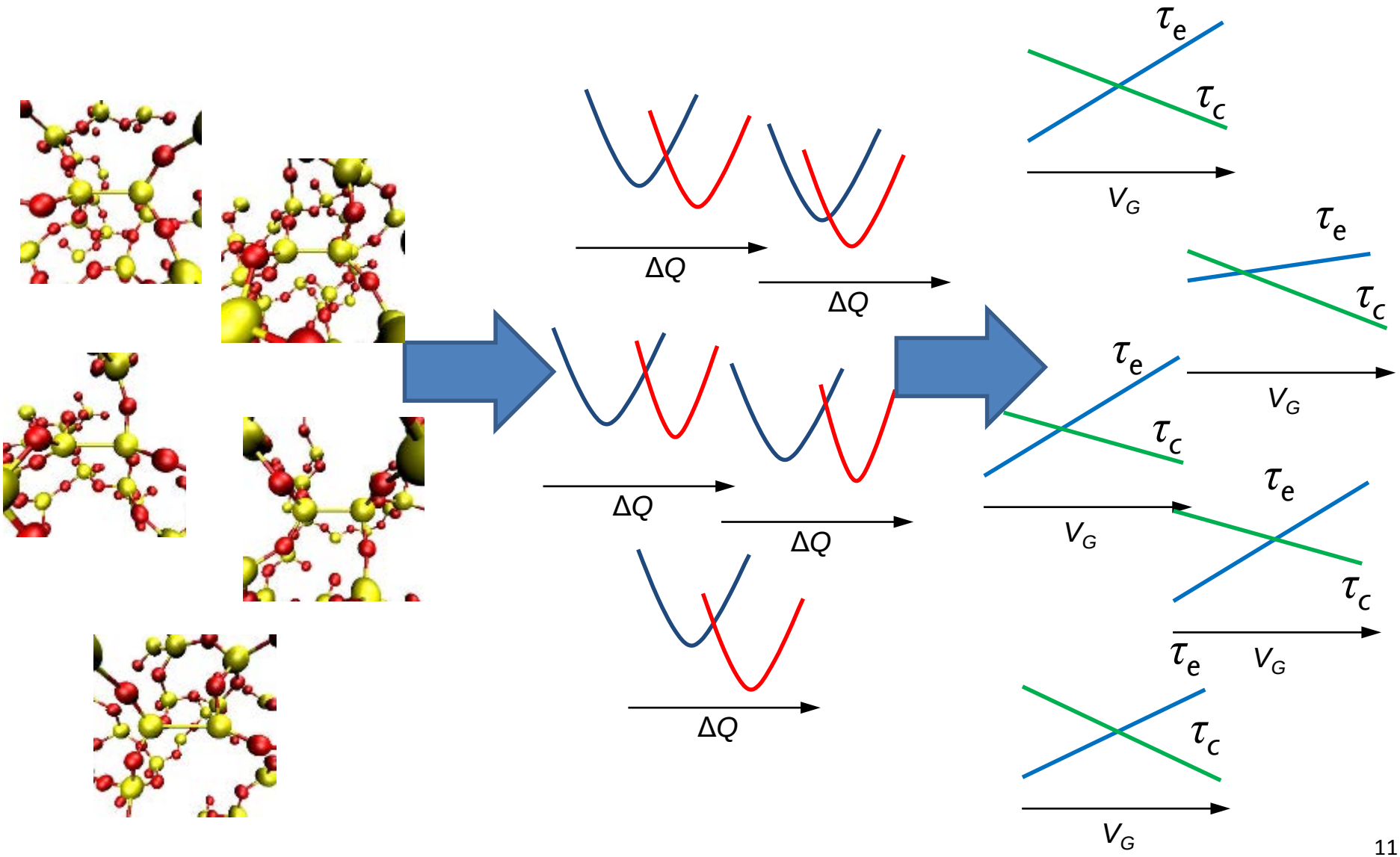


Advantages:

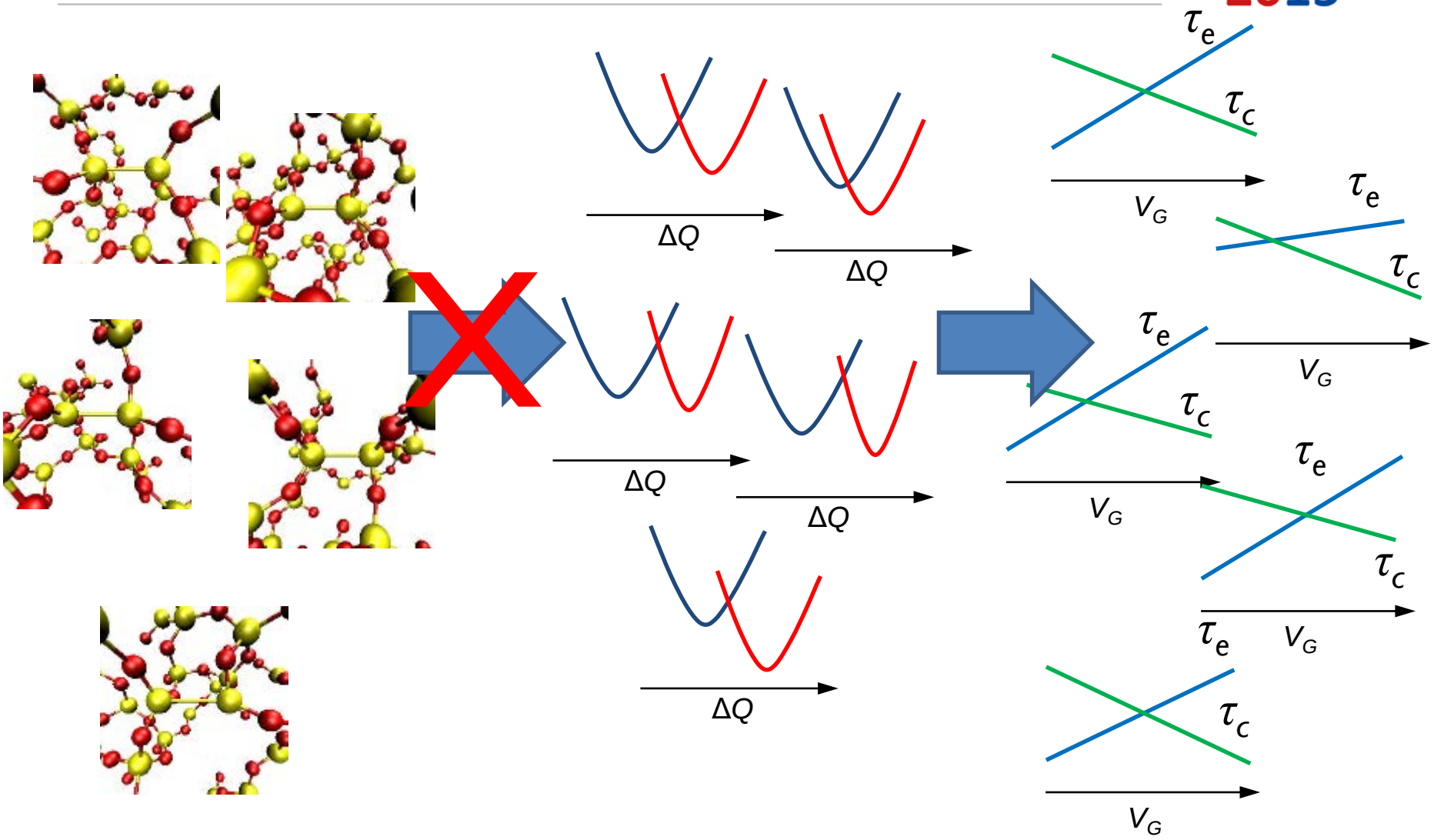
- Low level of abstraction
- Once properly set up, all trap-related effects come out "for free"



STRUCTURAL COMPONENT IN DISCRETE TRAPS APPROACH



PRAGMATIC ASSUMPTION



Assume normal distributions of parabolic well parameters

MEASURED BTI DEPENDENCES MODELED AND REPRODUCED IN TCAD

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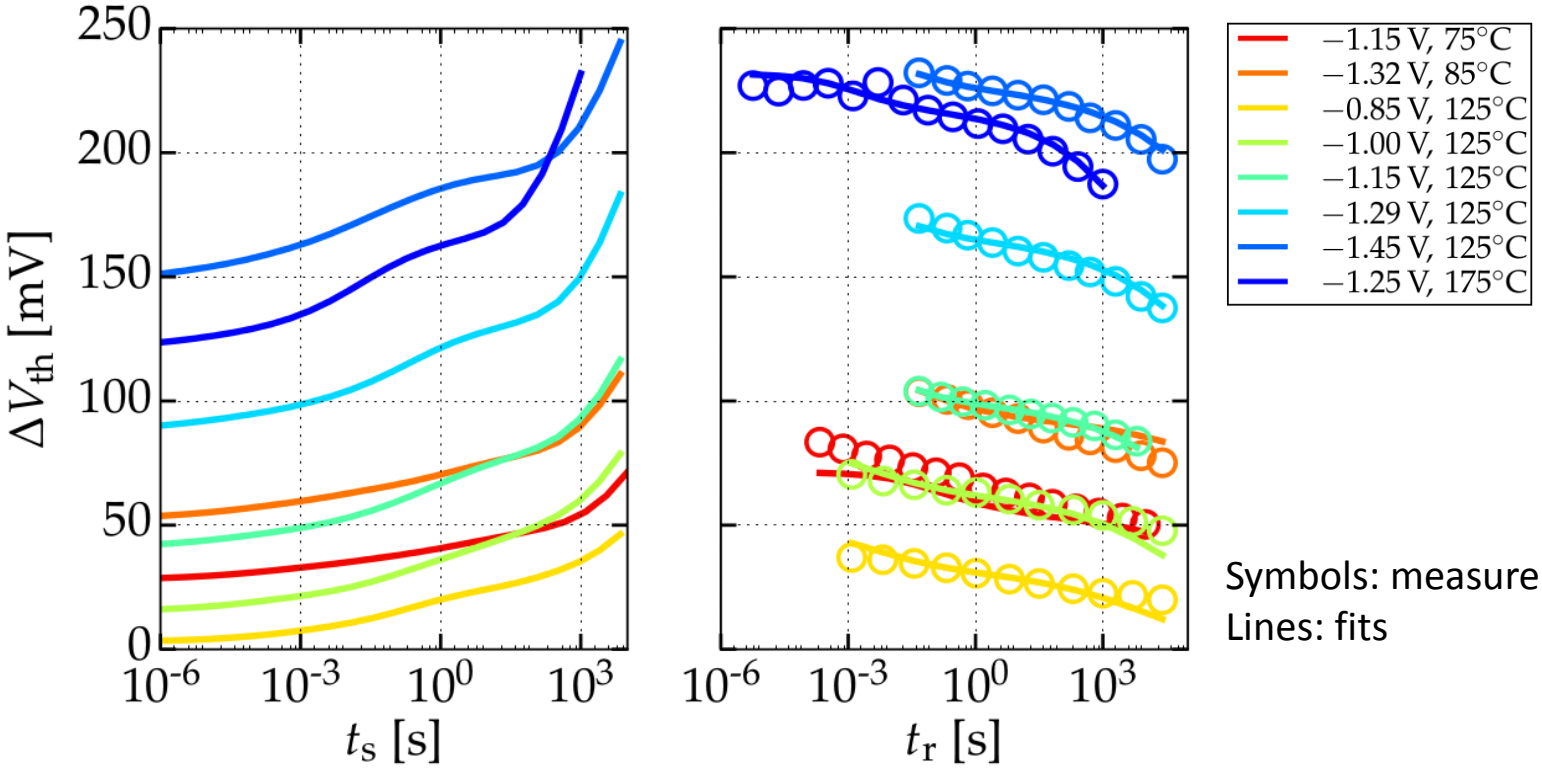
Extended-MSM measurements + “brute force” fitting with ~7000 “bulk” (full Non-radiative Multi-Phonon, NMP) and “interface” (dual-well, DW) defects

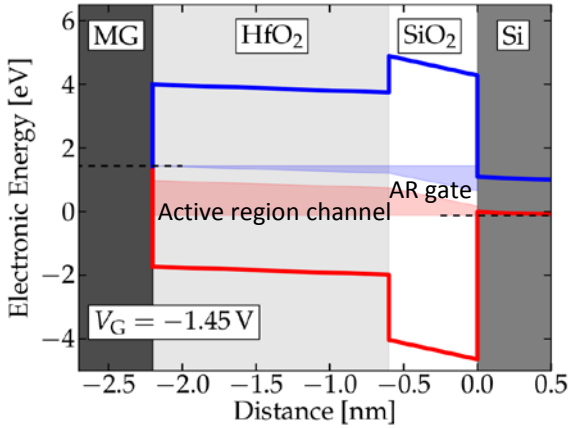


Symbols: measurements
Lines: fits

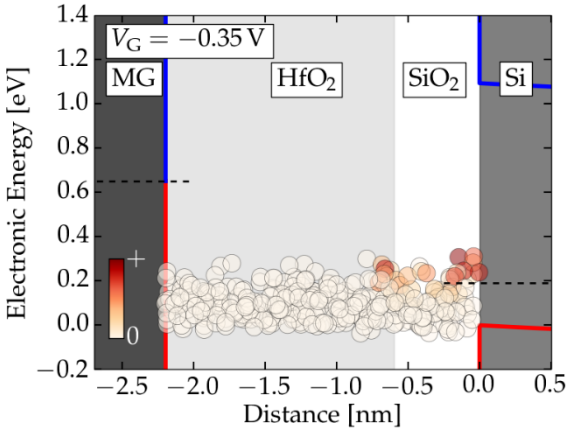
http://www.globaltcad.com

Courtesy G. Rzepa, TUW

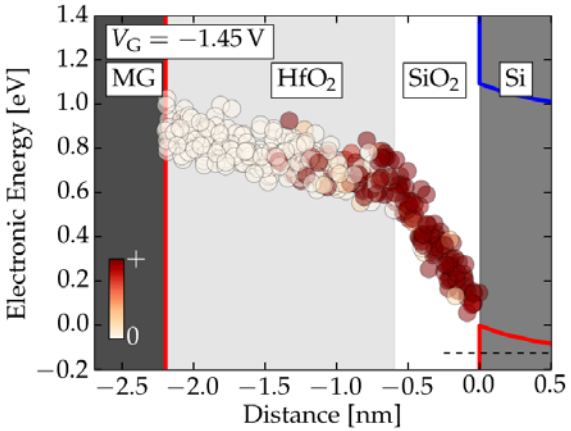
EXAMPLE OF FITTING



V_G = -0.35V

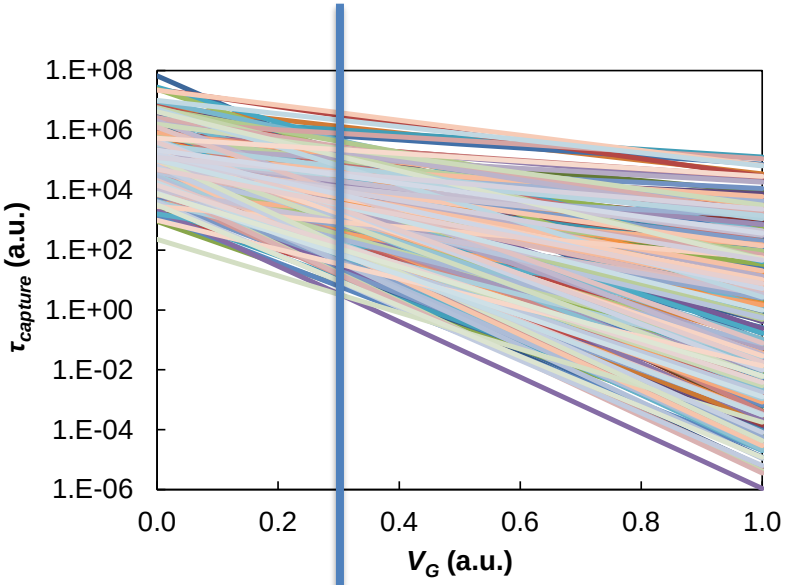


V_G = -1.45V



Courtesy G. Rzepa, TUW

RTN BEHAVIOR CAN BE REPRODUCED



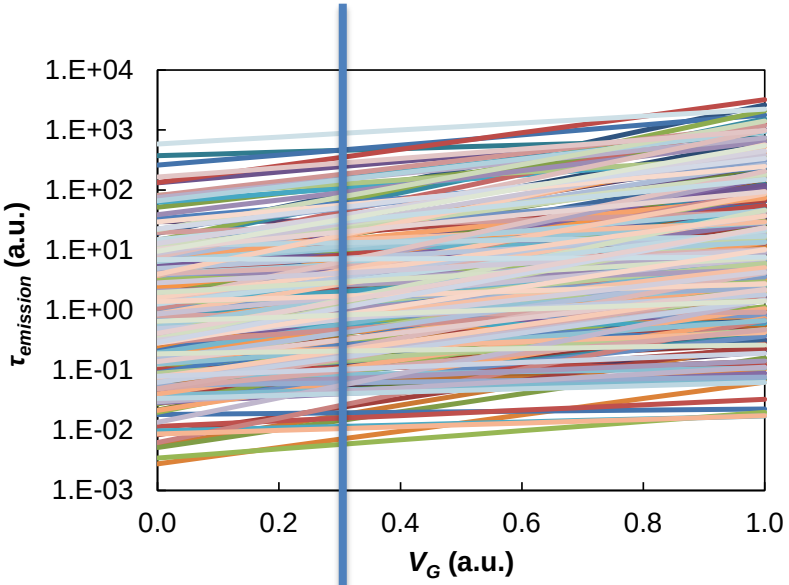
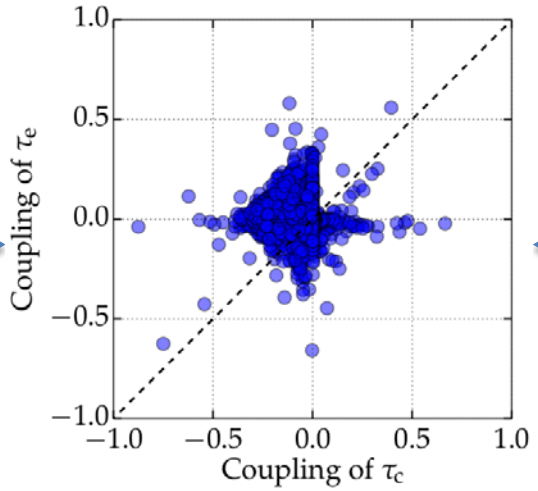
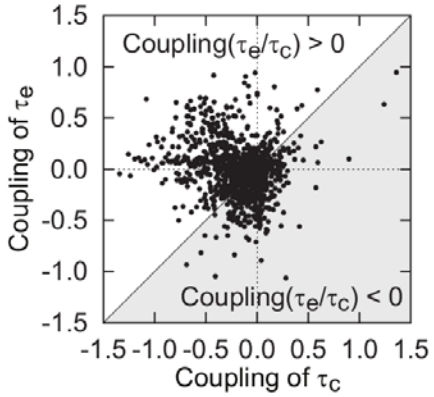


illustration only



RTN Measurement



Miki *et al*, IEDM 2012

$$\text{Coupling} = \frac{kT}{q}\frac{\partial \ln \tau}{\partial V_G}$$

"slope" of $\tau(V)$ plot

SAME APPROACH ALLOWS CONNECTION TO BTI AND "CET MAPS" (LARGE DEVICES)

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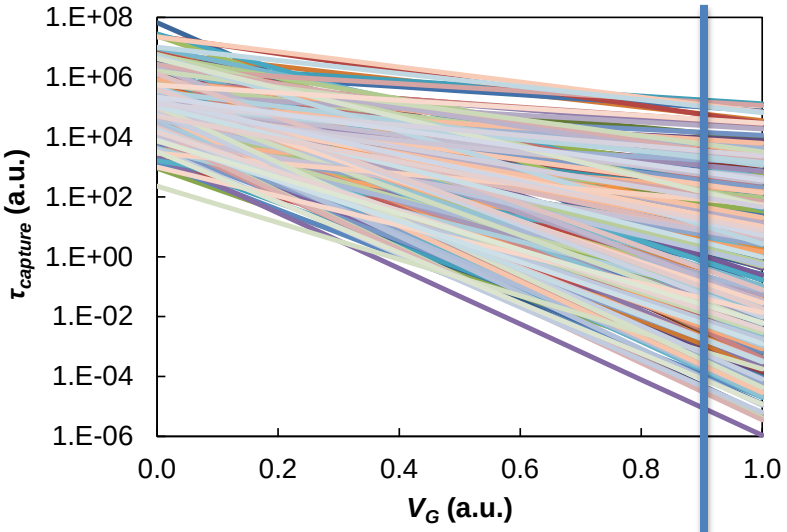


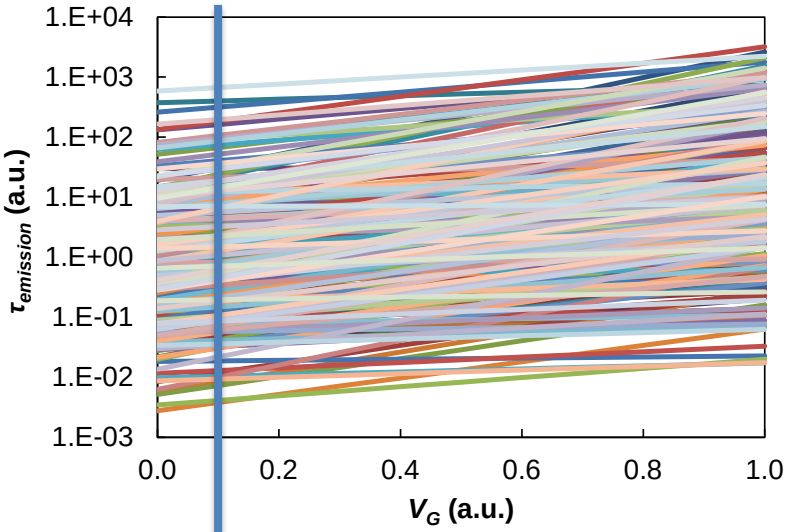
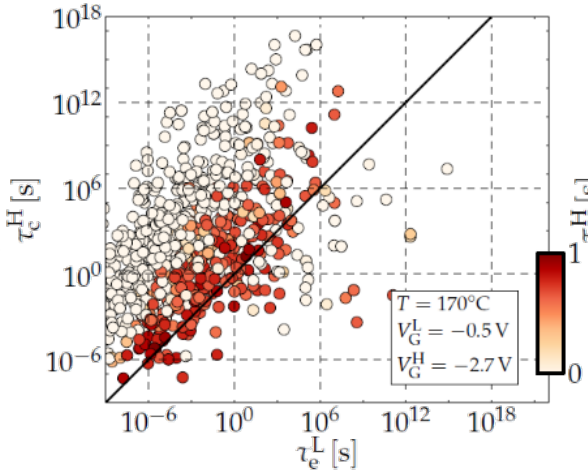
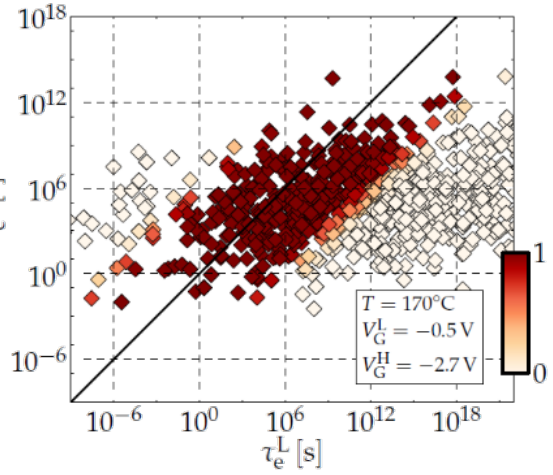


illustration only

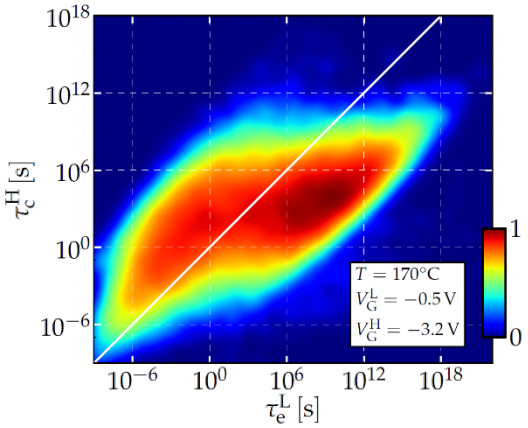
Bulk (NMP)



Interface (DW)

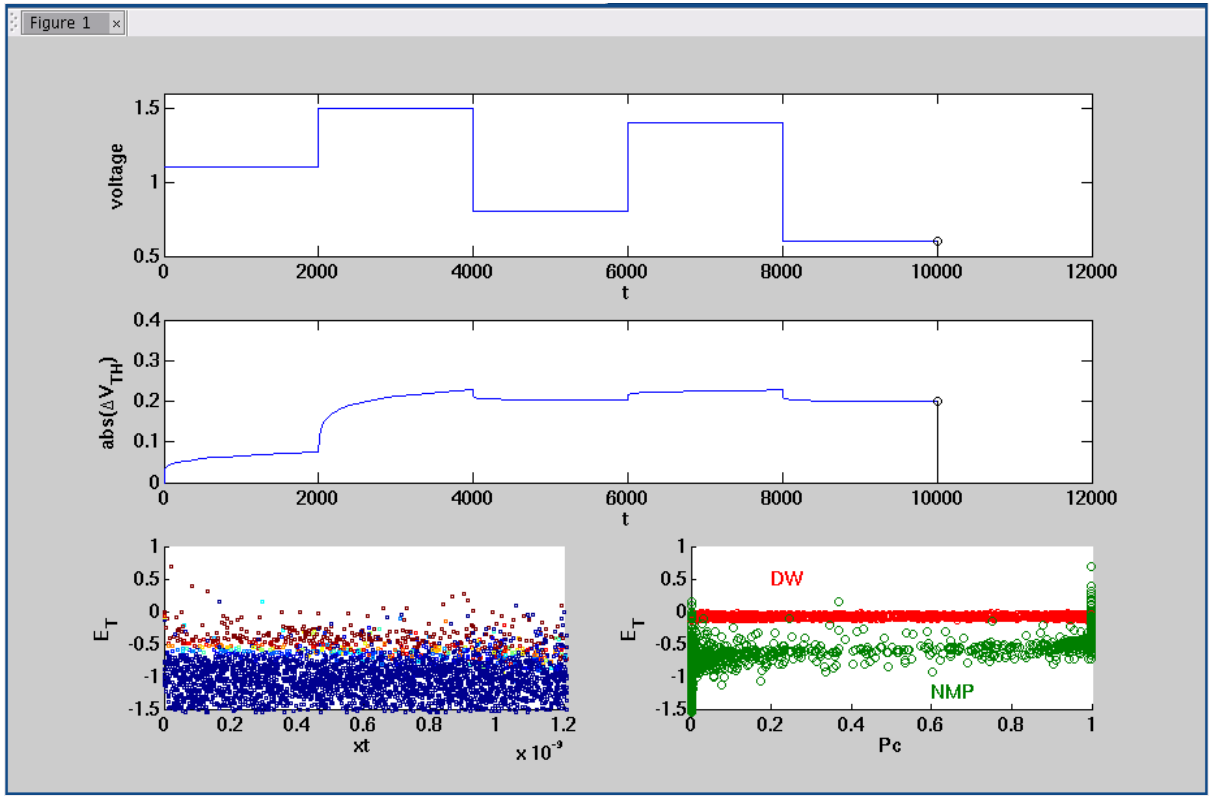


Capture/Emission Time (CET) Map



Rzepa *et al.*, SISPAD 2014

DEGRADATION DURING ARBITRARY $V_G(t)$ WAVEFORM CAN BE SIMULATED



- Trap occupation probability $P_c(t)$ calculated for every trap

(possible for constant and periodic phases, see e.g. Rodopoulos *et al.*, TDMR 2014; Giering et al., IIRW2014)

- Only impact on V_{th} considered
- In small devices with a handful of defects, variability naturally reproduced

DEEPLY-SCALED DEVICES CONTAIN ONLY A HANDFUL OF DEFECTS

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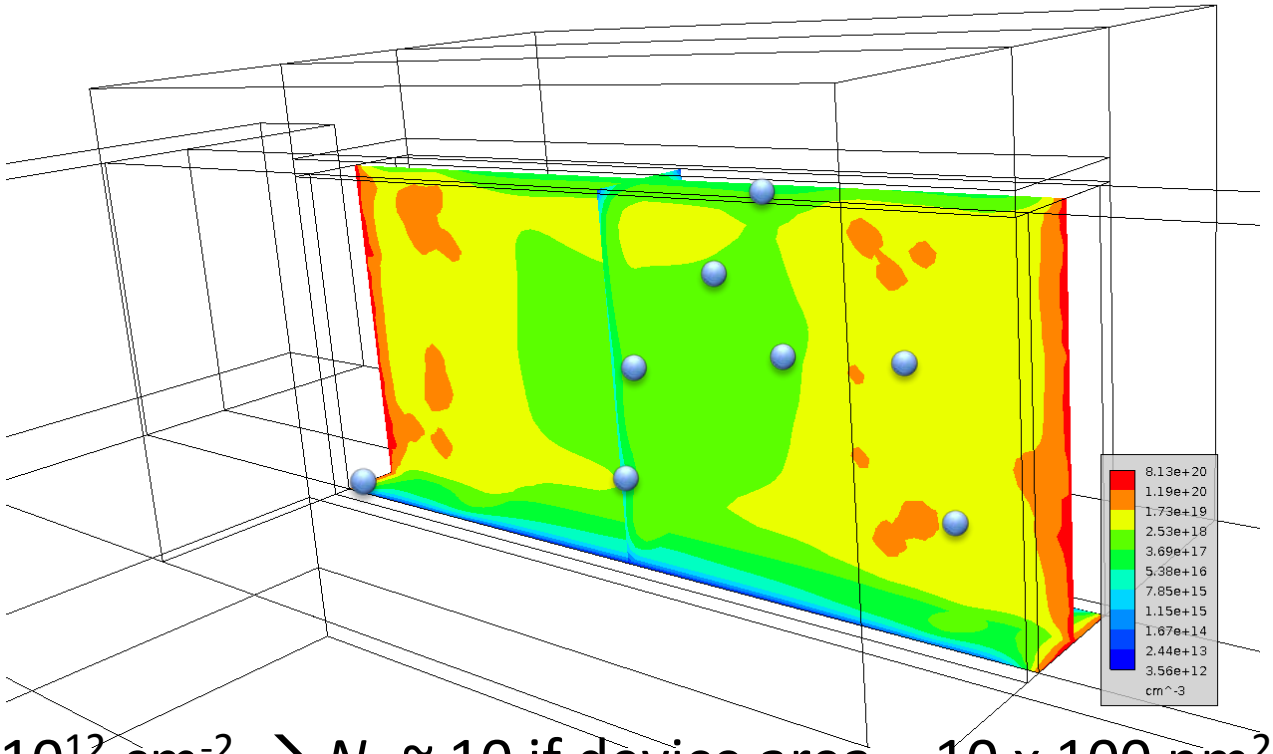
In deeply-downscaled technologies, only a handful of stochastically-behaving defects will be present in each device



Courtesy of M. Bina, TUWien

N_{ot} = 10^{12} cm^{-2} → N_T ~ 10 if device area = 10 x 100 nm^2

ΔV_{th} due to charged defects will be different in each device

→ **time-dependent variability** in addition to time-0 variability

INDIVIDUAL DEFECTS RESULT IN TIME-DEPENDENT VARIABILITY

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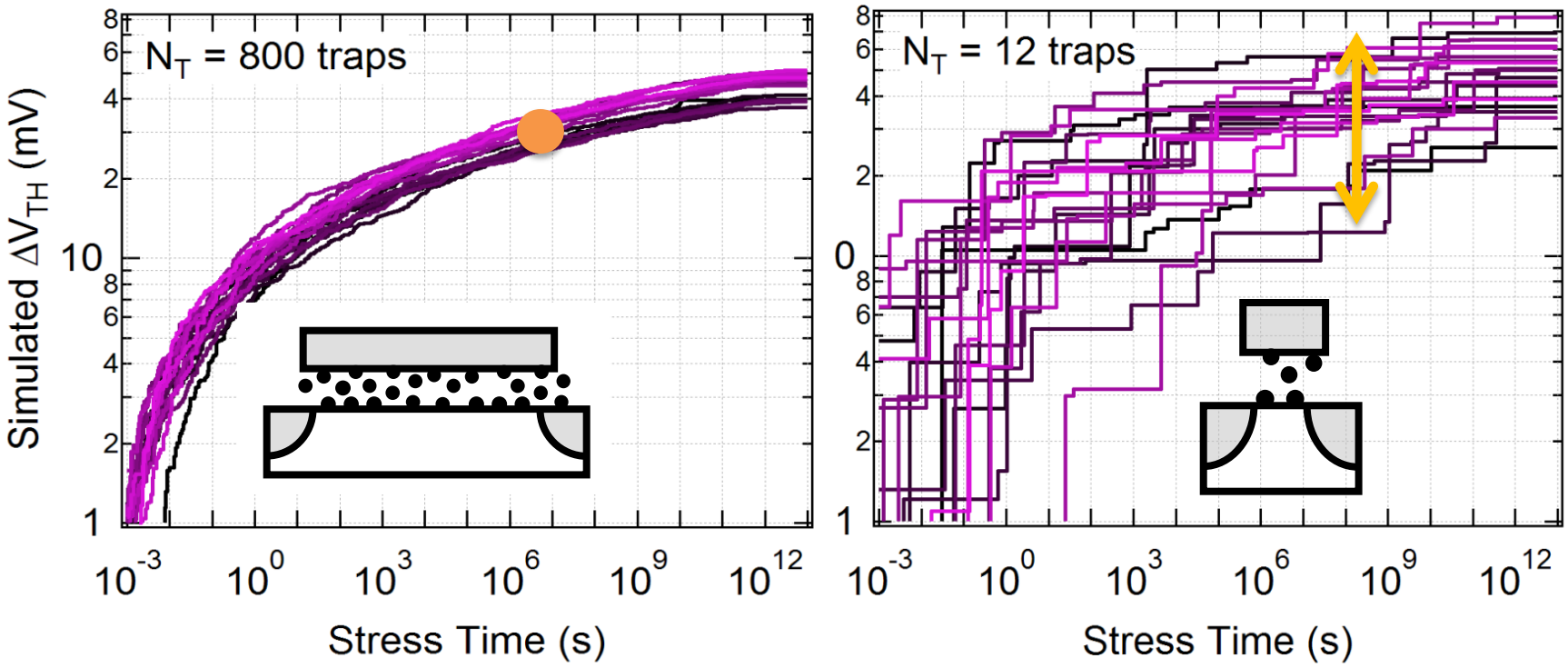

Grasser *et al.*, IEDM 2010

- Individual devices contain Poisson-*distributed* number of defects
- Individual defects have exponentially *distributed* impact on device

→ As opposed to large devices, the ΔV_{th} in deeply-scaled devices will be distributed

- Behavior naturally reproduced in the chosen discrete-defect approach

OUTLINE

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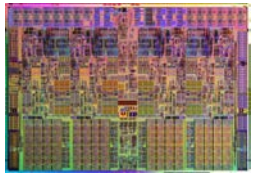
ESL



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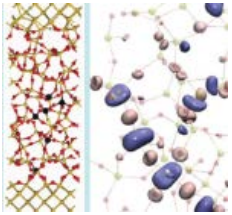
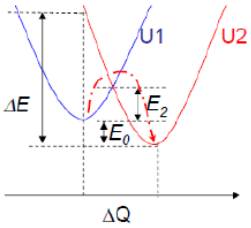
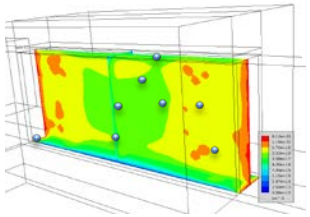
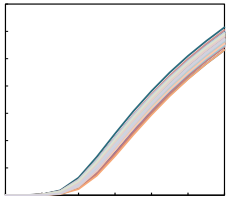
Trap kinetics

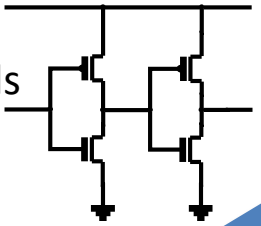
1st principles

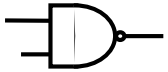












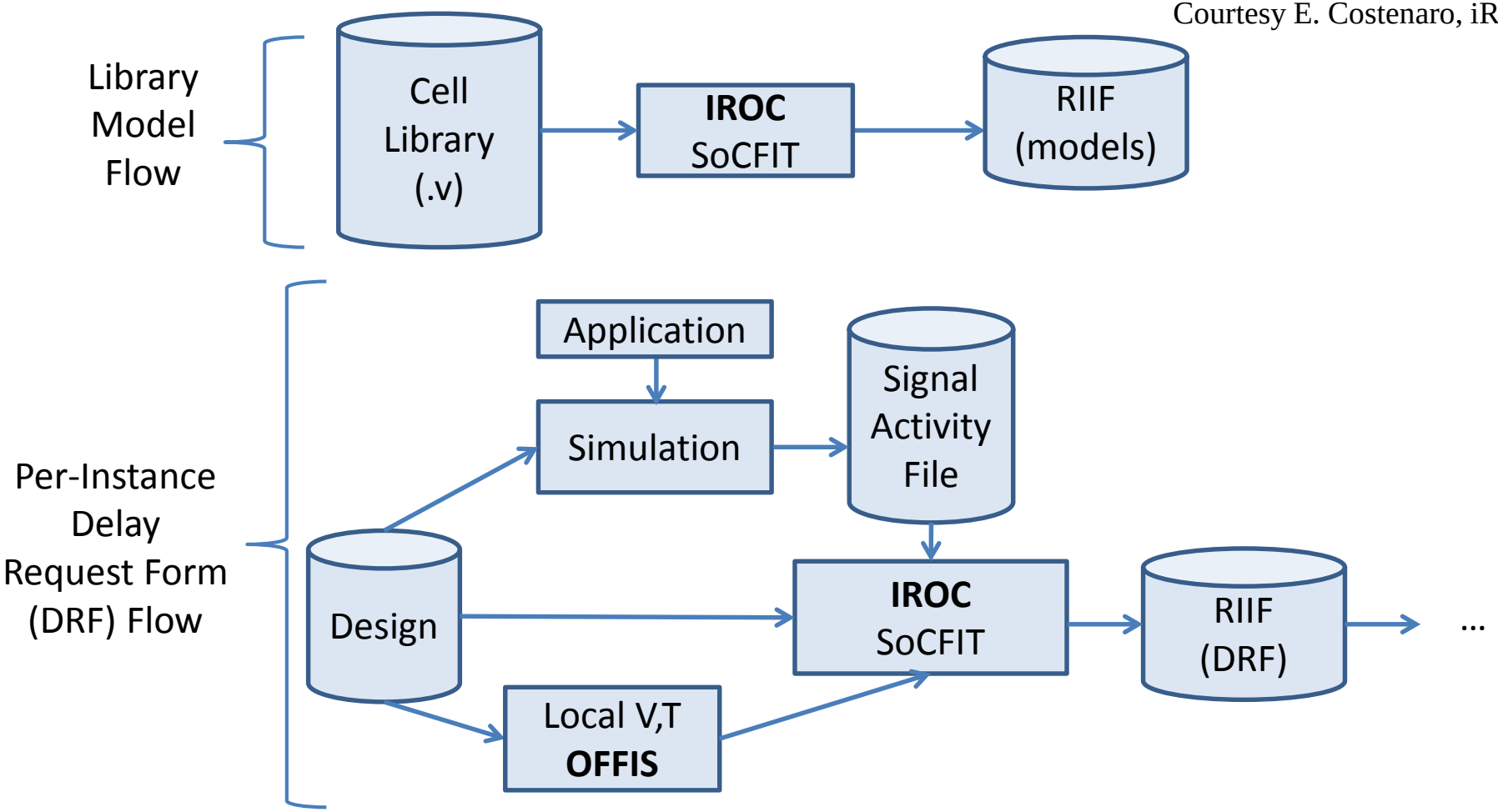
2

1

LIBRARY AND GATE LEVEL FLOW

ESSCIRC ESSDERC 2015

Courtesy E. Costenaro, iROC



- SoCFIT is IROC's internal chip-level reliability tool
- A cell library can be converted into per-cell type reliability models (RIIF)
- GLN of a design can be read, converted to per-instance **D**elay **R**equest **F**orms (DRF in RIIF)

EXAMPLE LIBRARY RIIF MODEL

ESSCIRC ESSDERC 2015

Courtesy E. Costenaro, iROC

```
component AND2_X1;
   // Operating parameters
   parameter VCC = 1.0;
   parameter TEMP = 25;

   parameter A_INP_ACTIVITY; // activity on A-input
   parameter B_INP_ACTIVITY; // activity on B-input
   parameter Y_OUT_ACTIVITY; // activity on Y-input

   // Failure modes (radiation induced)
   fail_mode SET_25ps = 10 ; // FIT
…
   fail_mode SET_150ps = 1; // FIT
 //-------------------------------------------------
 // Failure modes (EM induced)
   fail_mode EM_Y_STUCK = 0.02; // per-gate EM FIT rate
 //-------------------------------------------------
   // Added delay due to BTI
   parameter A_Y_RISE_INC_DELAY = 0;  // incr. delay (ps)
   …
   parameter B_Y_FALL_INC_DELAY = 0; // incr. delay (ps)
endcomponent // AND2_X1
```

- Generic RIIF model for a gate.
- By default assume nominal VCC and temperature.
- Default activity factor is unknown.
- BTI effect is modelled as incremental delay on each timing arc

REFINING LIBRARY GATES TO INSTANCES

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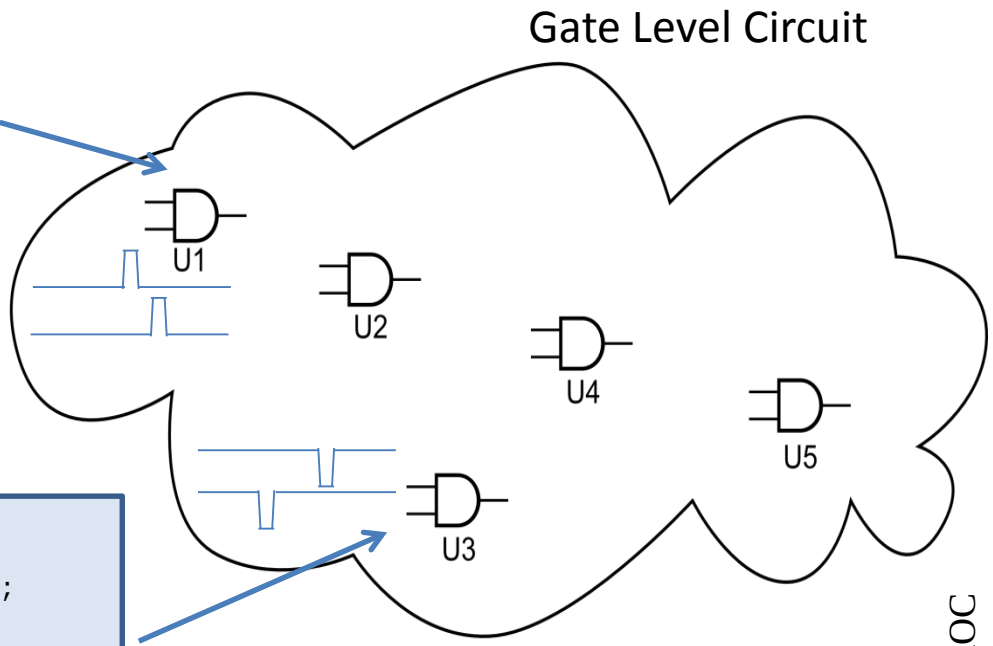
RIIF models refined on per Instance basic

```
component U1 extends AND2_X1;
   parameter VCC = 0.97;
   parameter TEMP = 85;

   parameter A_INP_ACTIVITY = 0.1;
   parameter B_INP_ACTIVITY=0.1;
   parameter Y_OUT_ACTIVITY=0.0;

endcomponent // U1
```

```
component U3 extends AND2_X1;
   parameter VCC = 0.91;
   parameter TEMP = 95;

   parameter A_INP_ACTIVITY = 0.9;
   parameter B_INP_ACTIVITY=0.9;
   parameter Y_OUT_ACTIVITY= 0.9;

endcomponent // U3
```



- By simulating gate-level circuit, activity factors for each instance are extracted
- Each instance's unique characteristics form a DRF = **D**elay **R**equest **F**orm

Courtesy E. Costenaro, iROC

INSERTING DEGRADATION

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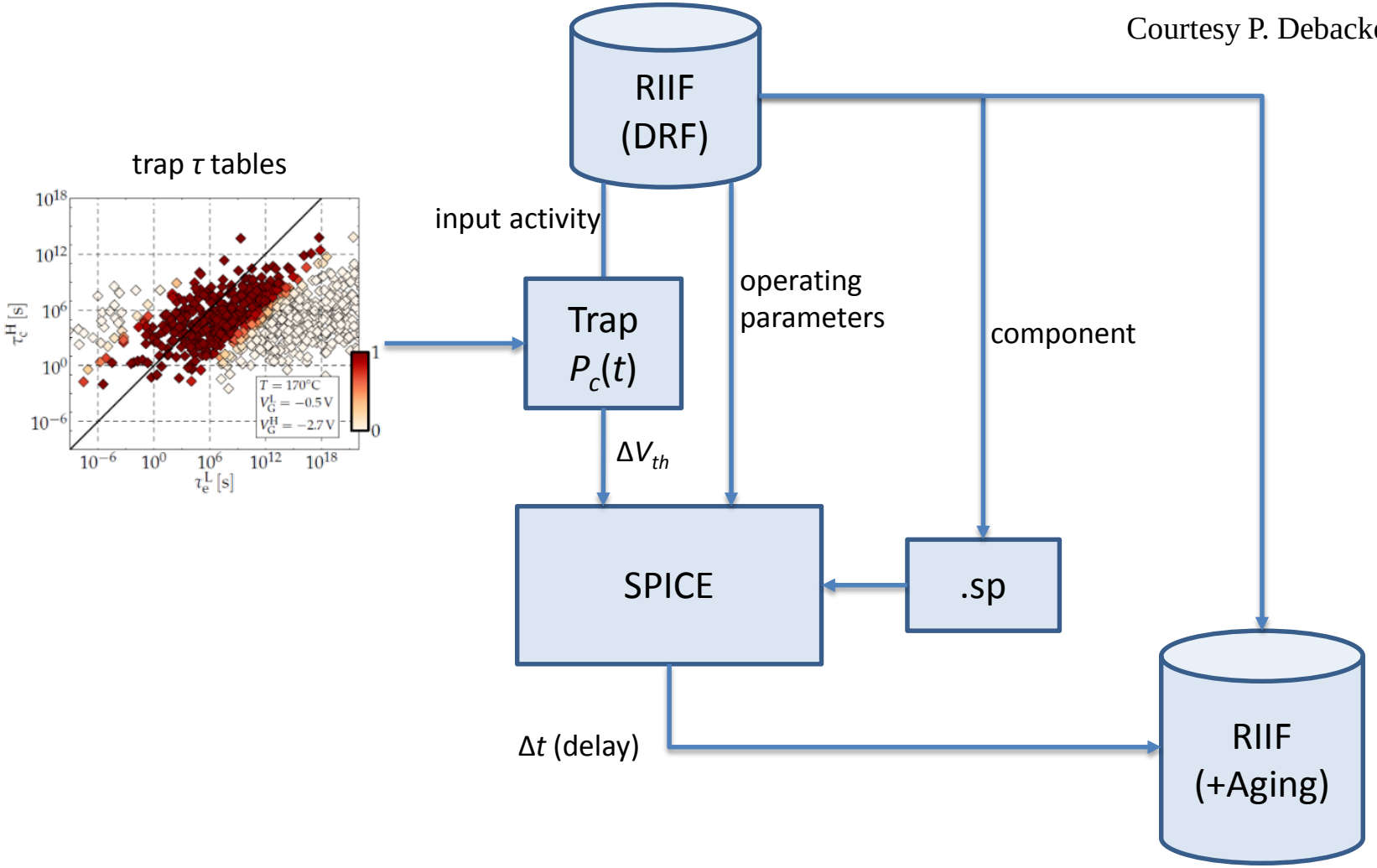
Courtesy P. Debacker, imec

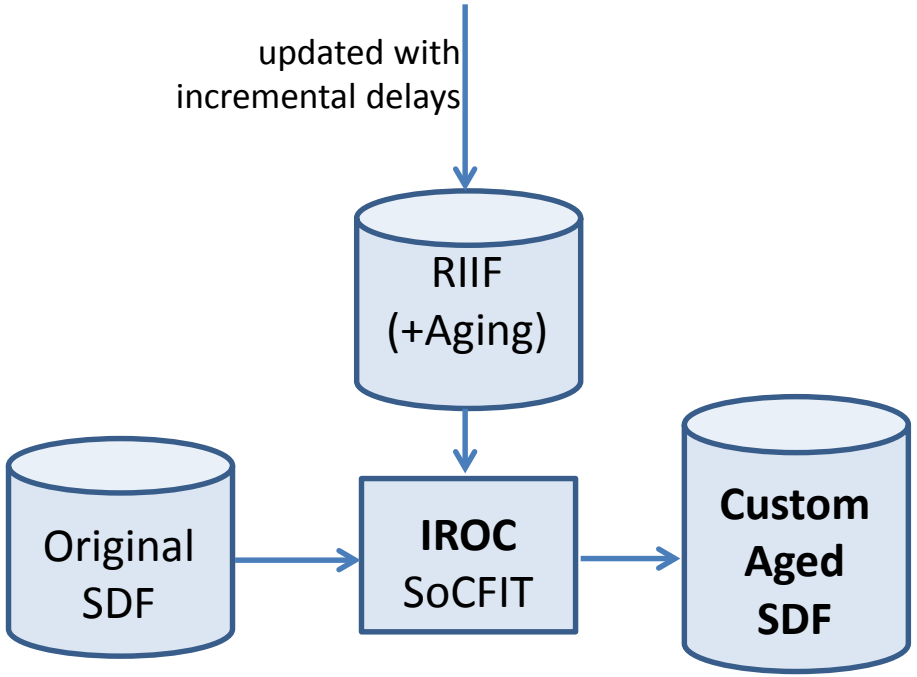


- In practice, more elaborate spice-level preprocessing schemes are used to reduce runtimes
- **In small devices with a handful of defects, variability is naturally generated**

WORKLOAD-SPECIFIC AGING INFORMATION PROPAGATED INTO THE FLOW

ESSCIRC ESSDERC 2015

Courtesy E. Costenaro, iROC

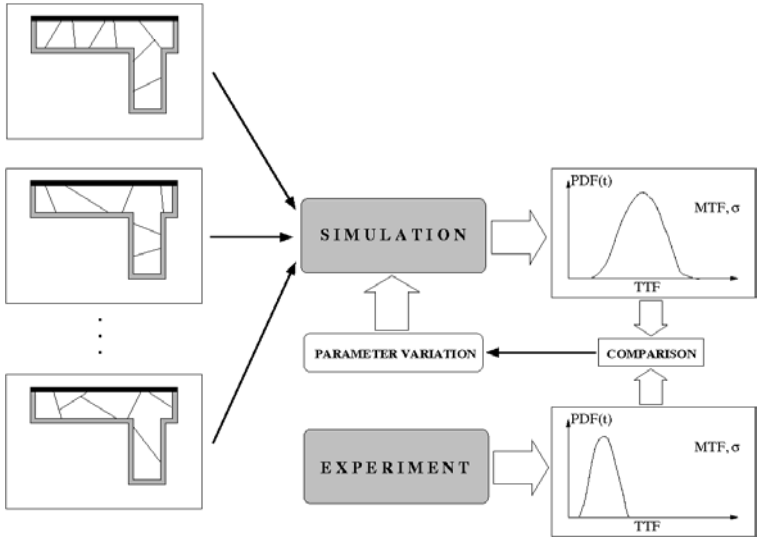


- Simulating gate-level circuit, activity information for each instance is extracted
- Also includes generating per-instance voltage and temperature information (OFFIS)
- Each instance's unique characteristics form a
  - DRF = **D**elay **R**equest **F**orm (in RIIF format)

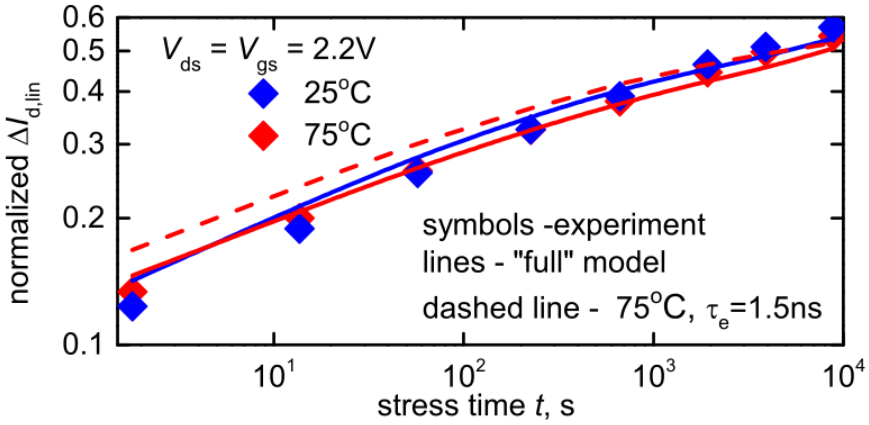
ALSO CONSIDERED IN MORV

- Electromigration
- Hot-carrier degradation

…



Ceric *et al.*, SISPAD 2015



Tyaginov *et al.*, EDL, submitted

SUMMARY

ESSCIRC ESSDERC 2015

EU project MoRV hierarchy has been reviewed, allowing inserting aging and variability into large-scale simulations

PARTNERS

ESSCIRC ESSDERC 2015

Partially funded by EU Project

Rainer Minixhofer, ams AG

ESSCIRC ESSDERC 2015

VARIABILITY SIMULATION WITHIN SUPERTHEME

Covering variability from unit process up to circuit level for mixed-signal circuits

Conference Sponsors:

JOANNEUM RESEARCH

IEEE

SSCS

amu

Infineon

NXP

TU Graz

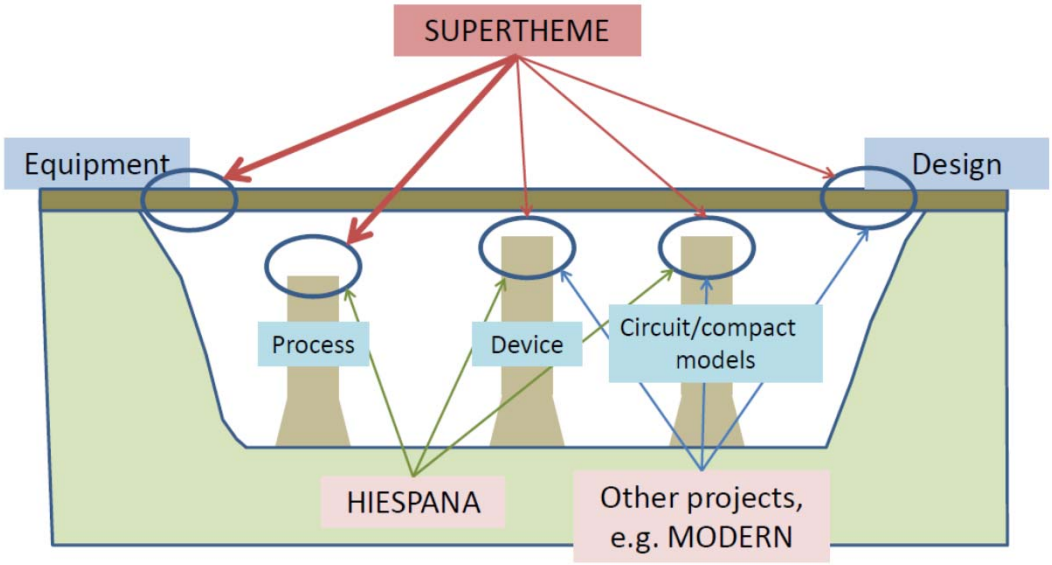
OUTLINE

1. Introduction: Multi-hierarchical simulation strategy for variability
2. Description of benchmarks and results
    1. System Level
    2. Circuit Level
    3. Circuit Element Level
    4. Process Level
3. Conclusions and Outlook

1

INTRODUCTION: MULTI-HIERARCHICAL SIMULATION STRATEGY FOR VARIABILITY

FROM EQUIPMENT TO DESIGN



- Use existing frameworks (especially HIESPANIA and MODERN) to finalize „bridge“ from Equipment to Design
- Take HPA(high performance analog) parameters as benchmarks to assess environment built up during project

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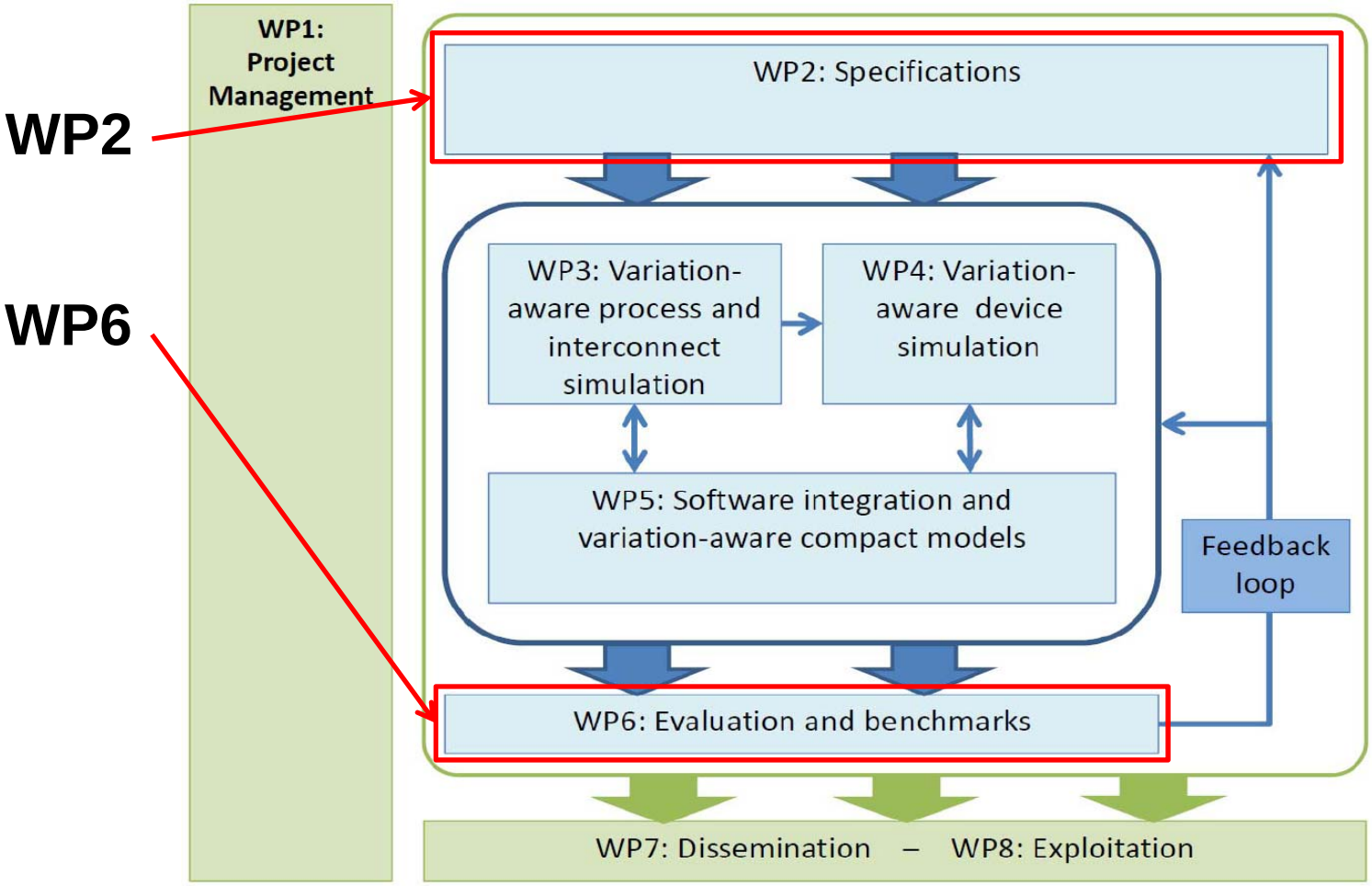
SUPERTHEME WORKPLAN CONTEXT



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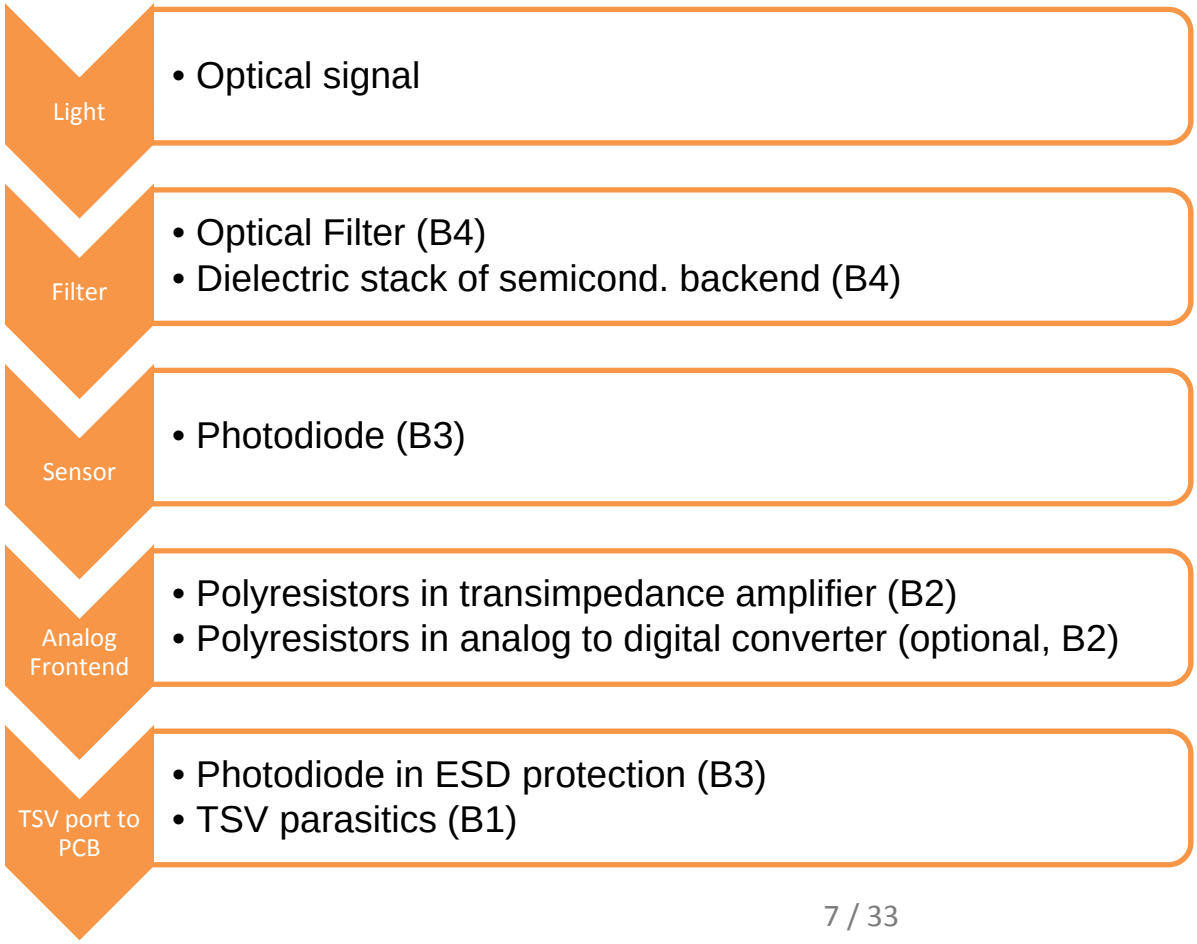
2

DESCRIPTION OF BENCHMARKS AND RESULTS

STRUCTURE OF BENCHMARK



- Classical SoC design
- Covers relevant analog area
- Highly relevant market for ams
- Complementary to More Moore ITRS
- Representative high performance analog benchmark

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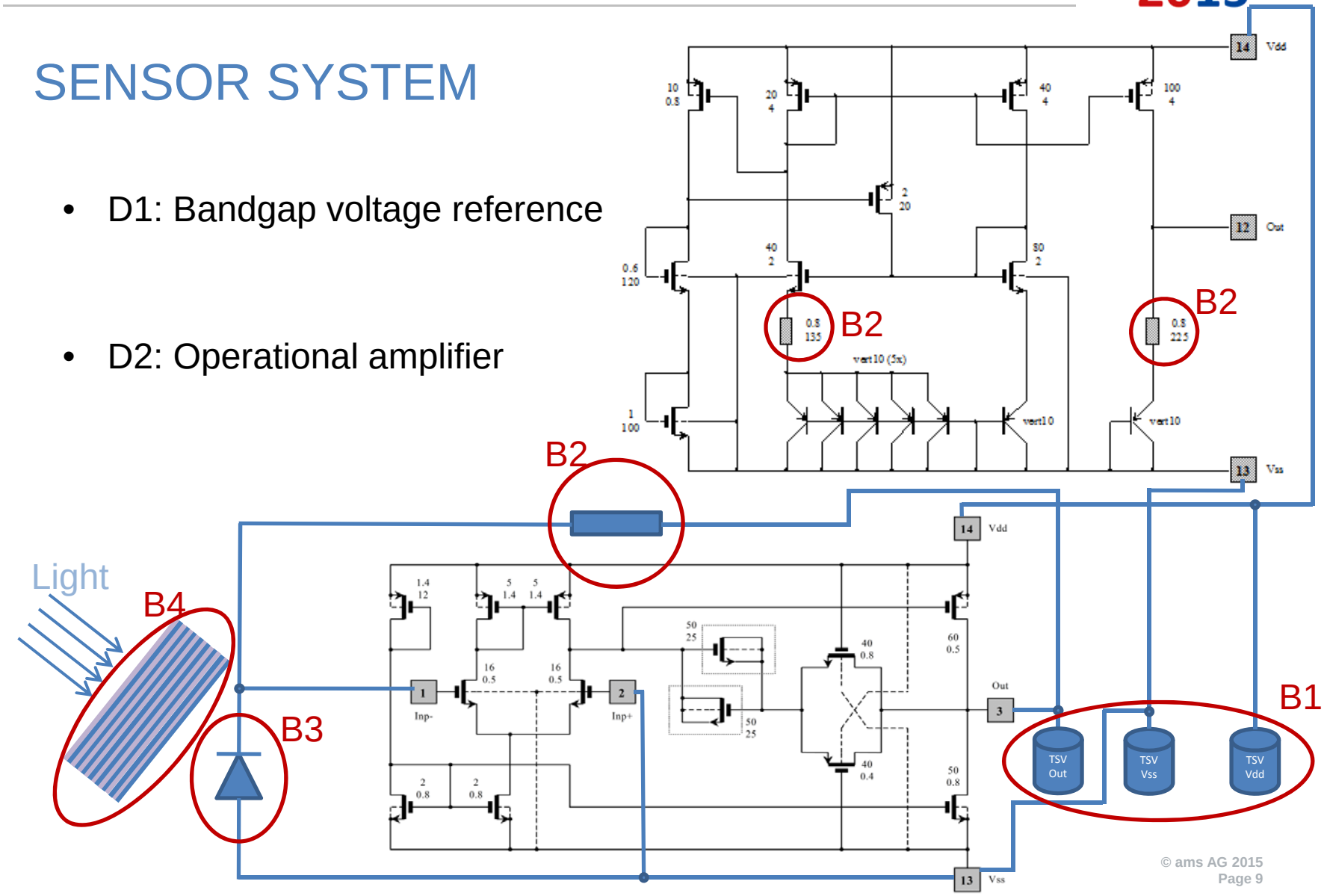
2.1

VARIABILITY ON SYSTEM LEVEL

SENSOR SYSTEM

- D1: Bandgap voltage reference
- D2: Operational amplifier



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VARIABILITY SOURCES

Label	Benchmark	Expected output	Relevant simulation features before device simulation
B1	Electrical performance and reliability of Through Silicon Vias (TSVs)	Variability of R/C and max. current density	Shape of TSV etch / shape of isolation deposition / shape of conductor deposition / electrical conductor properties
B2	Electrical performance of polycrystalline silicon resistors	Variability and matching of sheet resistance	Polysilicon morphology (grain size/grain shape/resistor shape) / doping distribution incl. segregation
B3	Electrical performance of junction diodes	Variability of blocking voltage and optical sensitivity	Doping distribution within device / contacts position and shape
B4	Optical performance of dielectric stacks	Variability and roughness of stack layers	Layer roughness / layer thickness / layer composition

- Selection of benchmark components
- Covers broad range of analog design components
- Good balance btw. relevance and complexity
- Representative demonstrators for other analog applications

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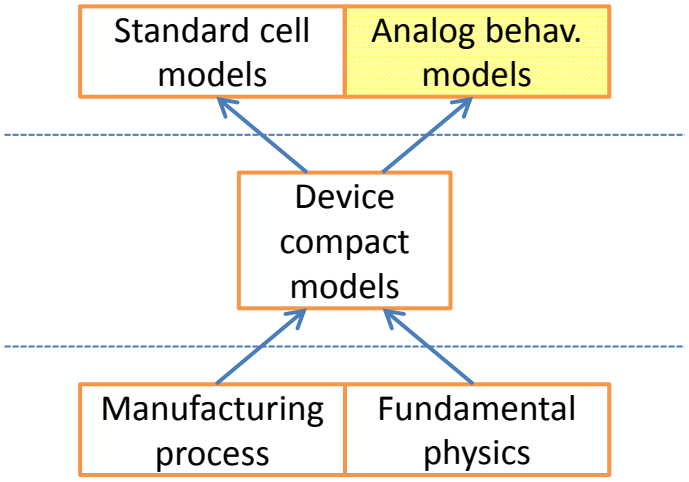
2.2

VARIABILITY ON CIRCUIT LEVEL

IP-BLOCK BENCHMARK D1 AND D2

Motivation and Goals

- Simulation of benchmark SoC circuit and comparison with measurement data
  - B1 – B4 as well as D1 and D2
- Use of SUPERTHEME results in circuit design
  - Transfer of variability information from process variations and atomic-level random fluctuations to higher levels of abstraction
    - Digital design: standard cells
    - Analog design: analog sub-blocks
- Model requirements
  - Gaussian and non-Gaussian distributions
  - Arbitrary correlations



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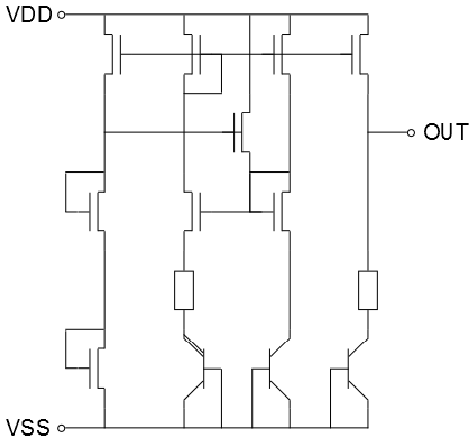
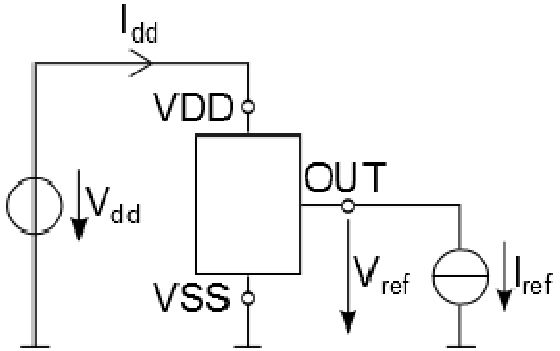
D1: BANDGAP VOLTAGE REFERENCE

Basics





- Behavioral model

$$V_{ref}{}^{*} = A_1 + A_2 V_{dd}{}^{*} + A_3 T^{*} + A_4 (T^{*})^{2^{*}} + A_5 I_{ref}{}^{*} + A_6 V_{dd}{}^{*} T^{*}$$

$$I_{dd}{}^{*} = A_7 + A_8 V_{dd}{}^{*} + A_9 T^{*} + A_{10} (T^{*})^{2}$$

with

$$V_{ref}{}^{*} = \frac{V_{ref} - V_{ref,0}}{V_{ref,0}},\ V_{dd}{}^{*} = \frac{V_{dd} - V_{dd,0}}{V_{dd,0}},\ T^{*} = \frac{T - T_0}{T_0},\ I_{ref}{}^{*} = \frac{I_{ref} - I_{ref,0}}{I_{ref,0}},$$

$$I_{dd}{}^{*} = \frac{I_{dd} - I_{dd,0}}{I_{dd,0}}$$

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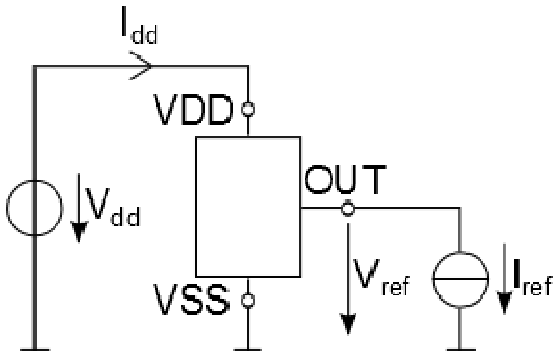
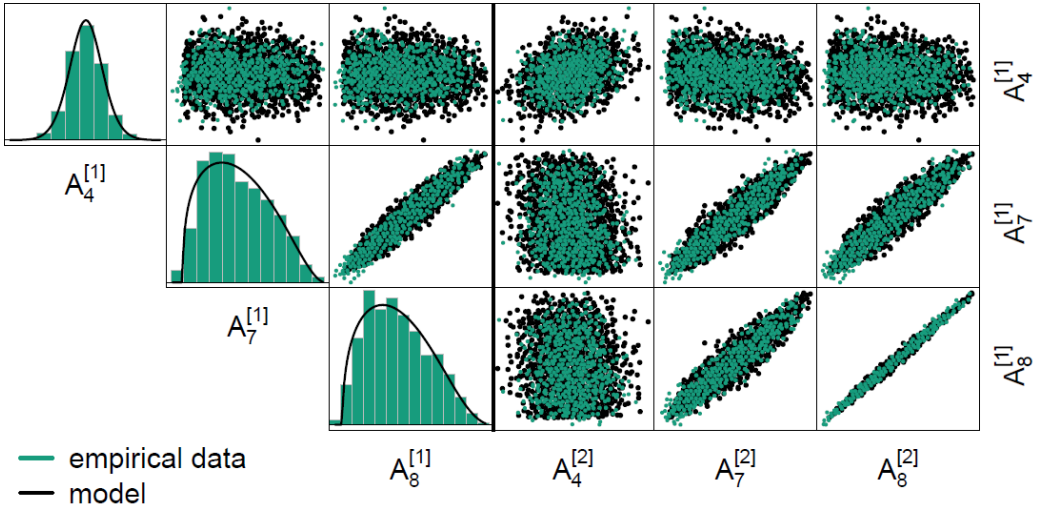
Page 13

D1: BANDGAP VOLTAGE REFERENCE

Variation-Aware Behavioral Model

- Model calibration: coefficients $A_1 \ldots A_{10}$ determined from circuit simulations varying V_{dd}, T, and I_{ref}
- Variation-aware model characterization: repetition of model calibration for MC samples of process parameters
- Variation-aware behavioral model: 10-dimensional random variable **A**

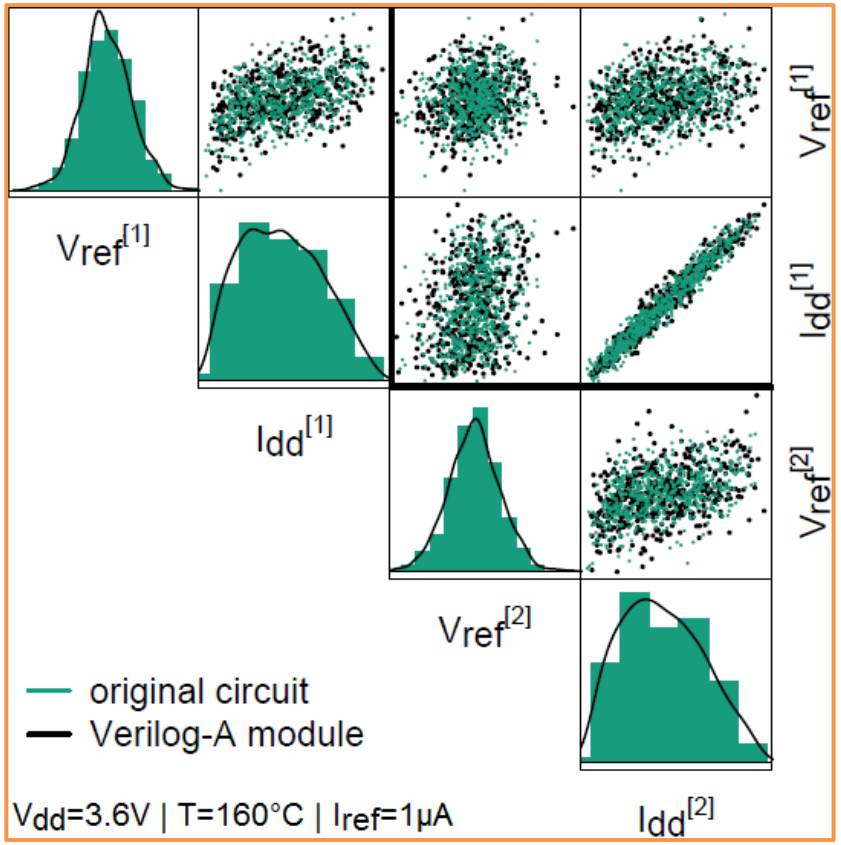




D1: BANDGAP VOLTAGE REFERENCE

Validation

- Comparison of circuit simulations and Verilog-A model evaluations for various combinations of V_{dd}, T, and I_{ref}
  - No significant differences between circuit representations
  - No significant differences between bandgap instances
  - 4X speed-up with Verilog-A model (7.2s instead of 33s for 500 samples)



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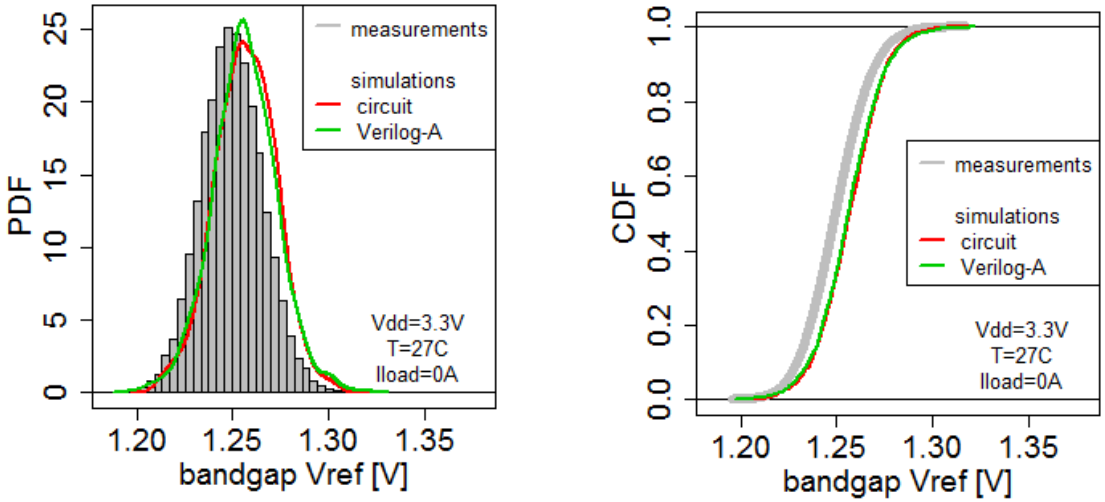
D1: BANDGAP VOLTAGE REFERENCE

Measurements vs Simulations

- Comparison of ams measurement results and simulations



- 0.5% mean shift
- Standard deviations practically identical

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D1 AND D2

Variability sources

Benchmarks B1 to B4 Empirical models vs. equipment parameters:

- R_{TSV}, C_{TSV}
- $R_{polysilicon}$
- BV_{diode}, C_{diode}, Responsivity
- Filter variability

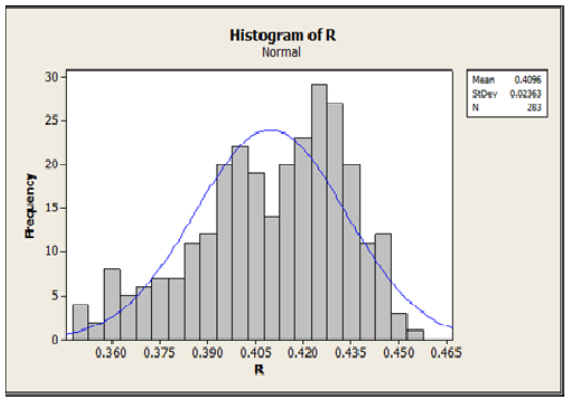
Simulation level

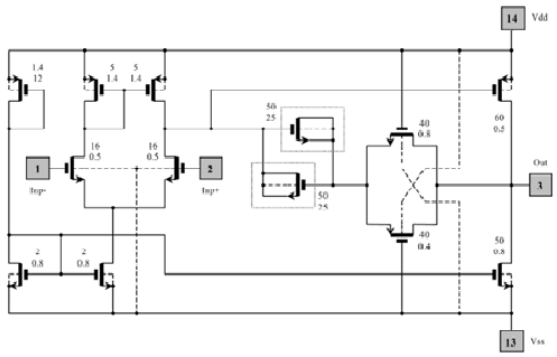
Empirical model included into Monte Carlo Spice simulation Analog Benchmarks D1, D2

Analysis

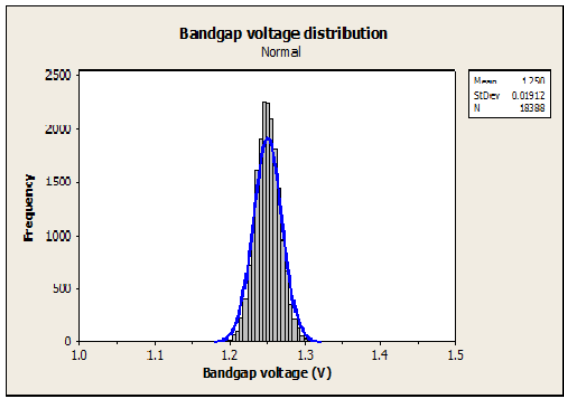
Sensitivity analysis of B1-B4 benchmarks on electrical parameters output of analog circuits D1 – D2

Comparison to electrical measurement distribution of electrical output





D1: Bandgap voltage reference



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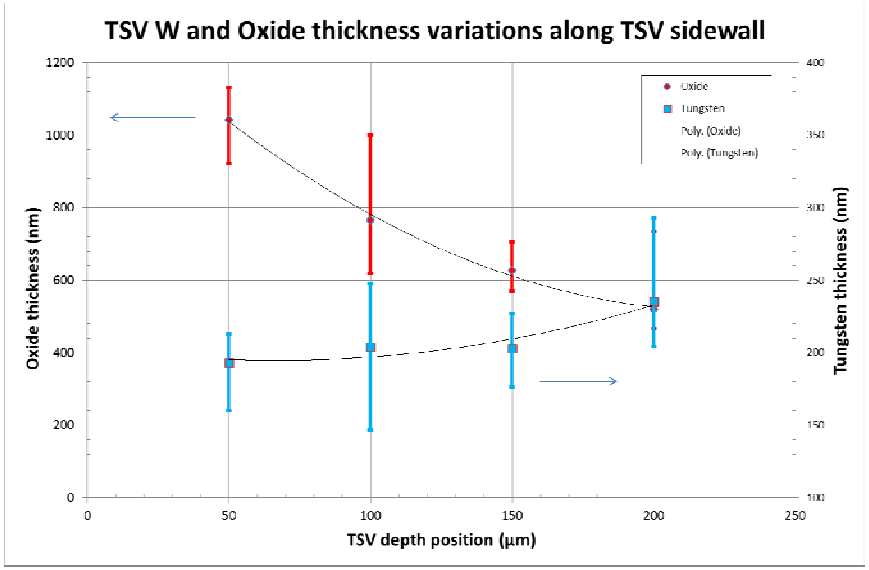
2.3

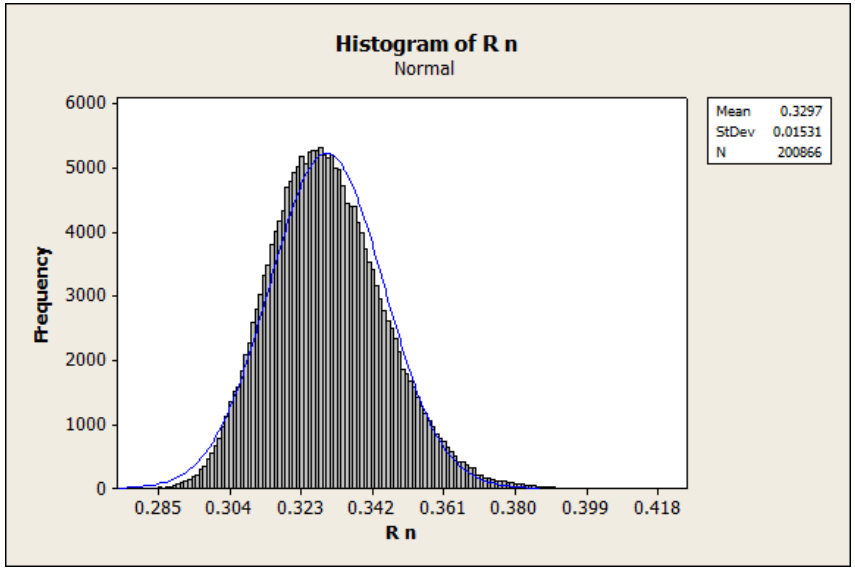
VARIABILITY ON CIRCUIT ELEMENT LEVEL

BENCHMARK B1

TSV processing

TSV resistance variation modelled vs. oxide and tungsten thickness variability observed in TEM images.





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BENCHMARK B2

Polycrystalline resistor

Variability sources

Furnace temperature gradient
Grain size statistical distribution

Simulation level

3D Grain structure is converted into netlist by adding additional nodes: Volume Centroid and Face Centroid

Electrical Structure is assumed to consist of Grain interior and Grain boundaries

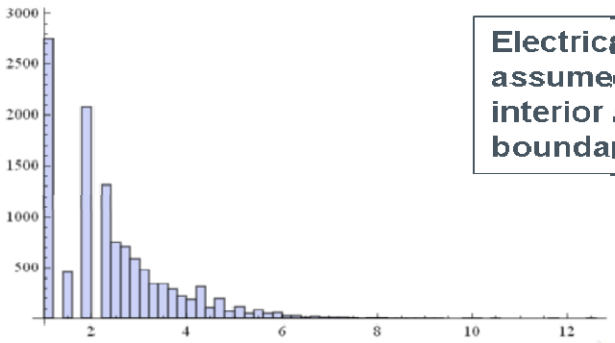
Responses surface modelling

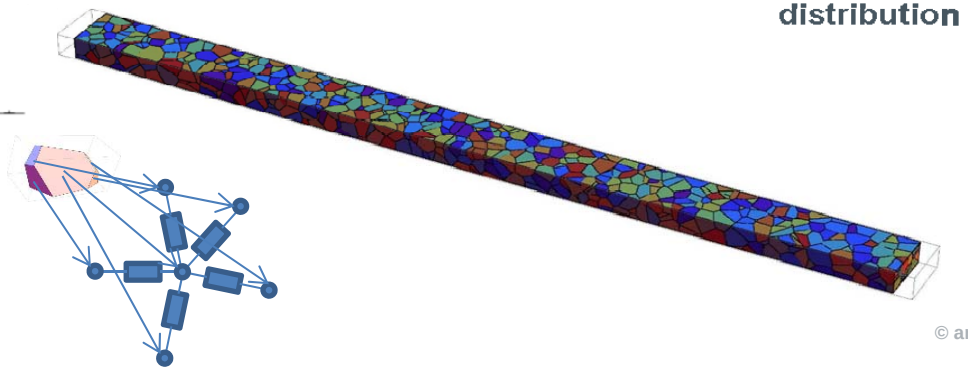
R

Analysis

Global sensitivity analysis on grain size

Comparison to poly-silicon resistance distribution





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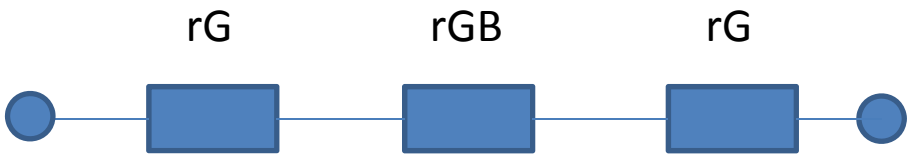
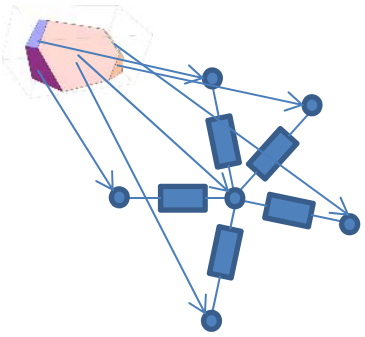
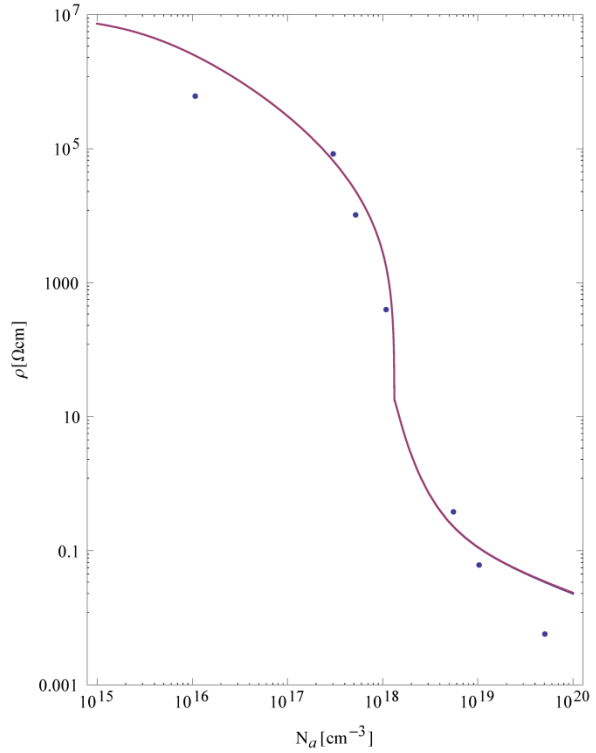
BENCHMARK B2

Polycrystalline resistor

- Further replace connection nodes at grain faces by additional resistor rGB
- Model rG with single crystal properties and rGB with amorphous material properties (Mott formalism, Khondker Model)
- Comparison to data collected on shortloops







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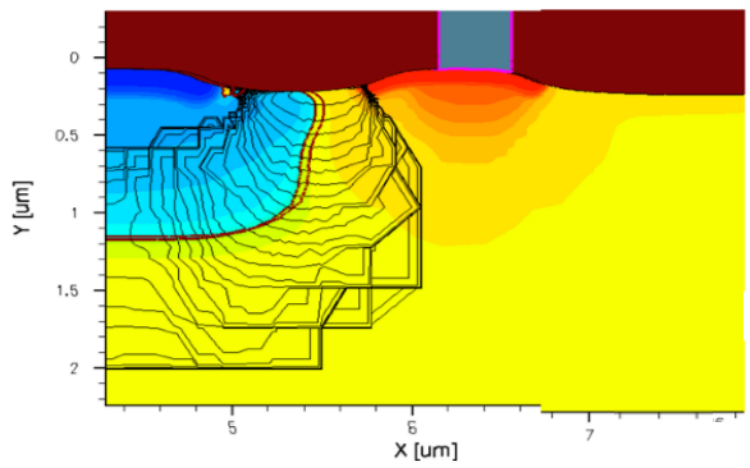
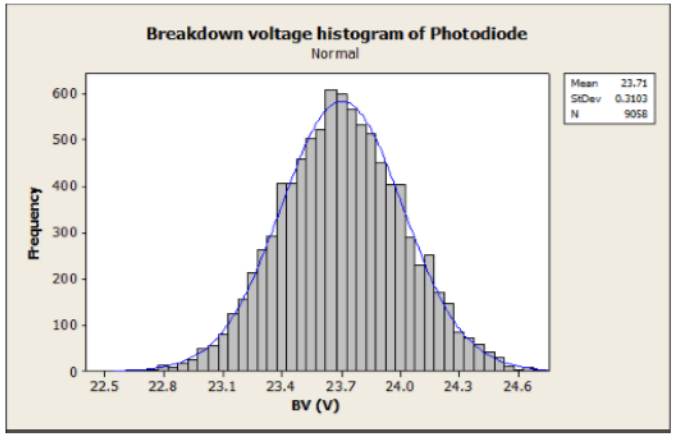
BENCHMARK B3

Photodiode & Reference diode

Variability sources	Simulation level	Responses surface modelling	Analysis
CD variation Implantation condition variation Oxide thicknesses	Synopsys TCAD Process, device Optical TMM simulation	BV Capacitance Optical responsivity	Comparison to online measurement of BV, C





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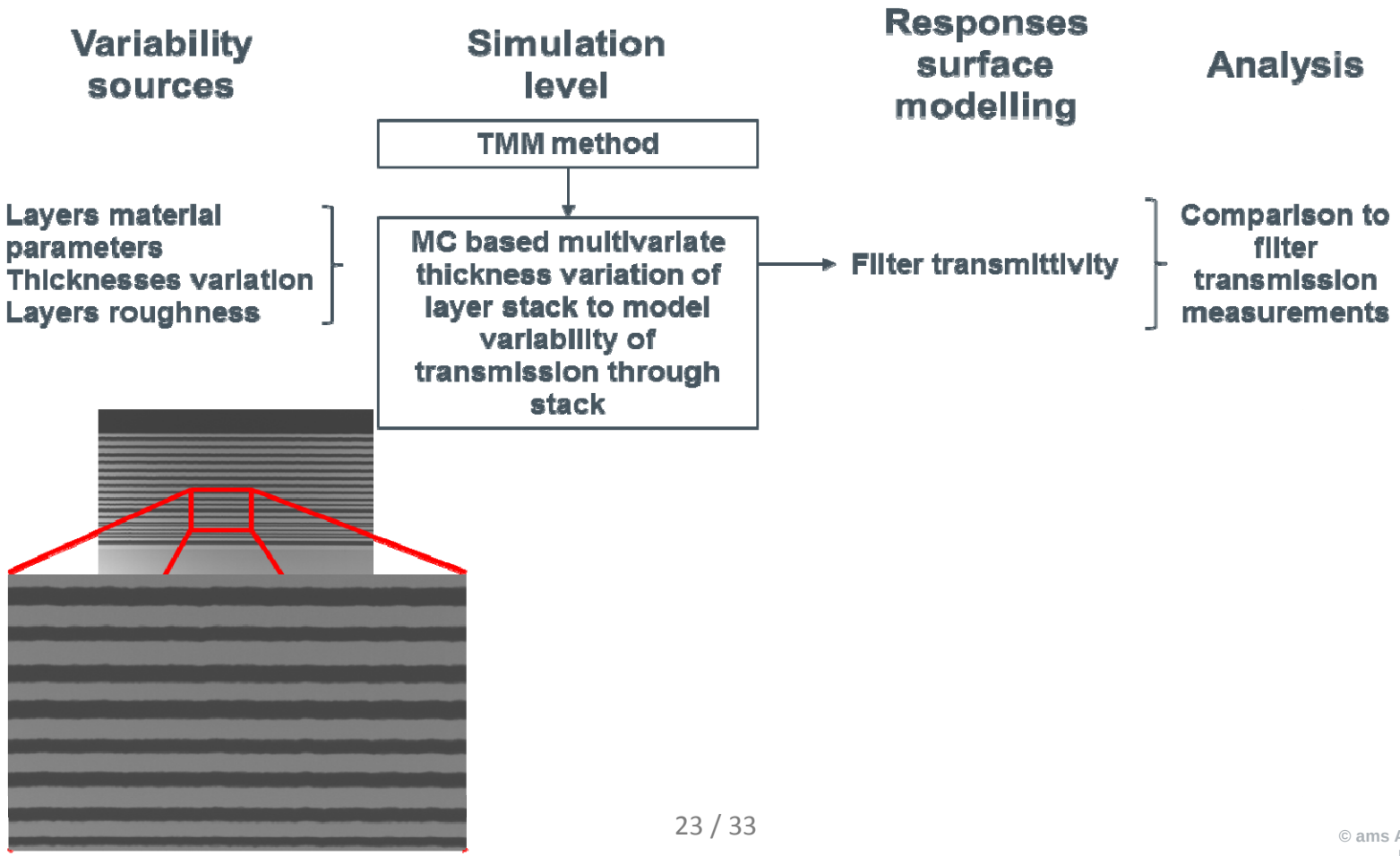
BENCHMARK B4



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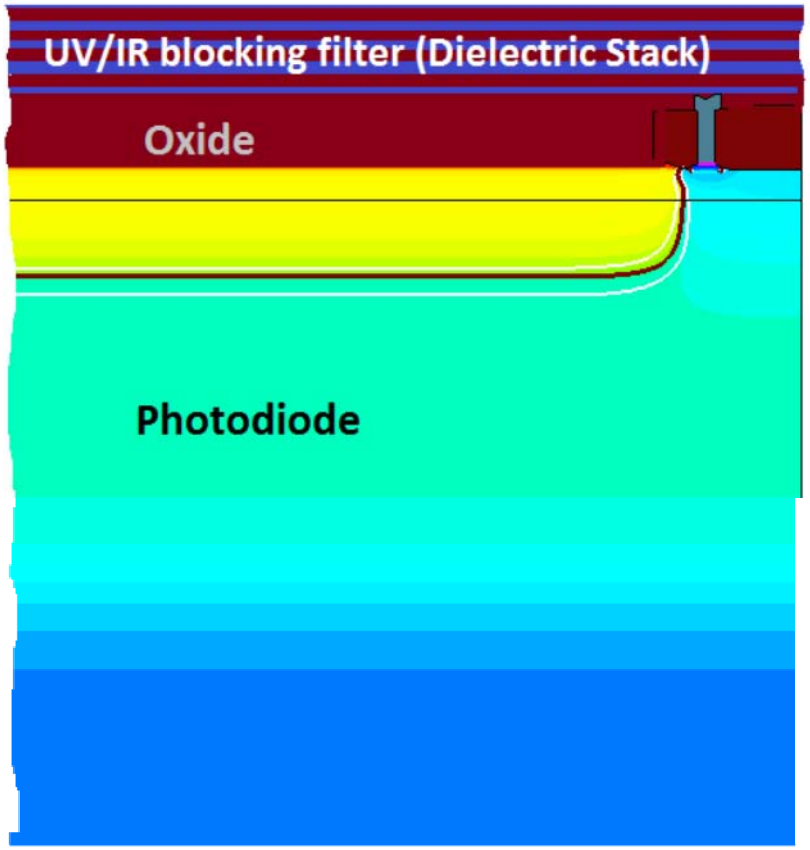
BENCHMARK B3 AND B4: PHOTODIODE + FILTER

UV/IR blocking filter + Photodiode



- 1. Dielectric thickness vs. transmission
  (1D TMM simulation with Mathematica)
- 2. Filter stack equipment simulation (DEP3D)
- 3. Filter + photodiode simulation
  (1D TMM simulations with TCAD)
- 4. Process variability: CD, overlay, implant dose/energy,Oxide thickness, substrate, epi-thickness
- 5. Investigation:
  - Photodiode: “Process variability” vs “Responsivity, Blocking voltage”
  - Filter + photodiode: responsivity

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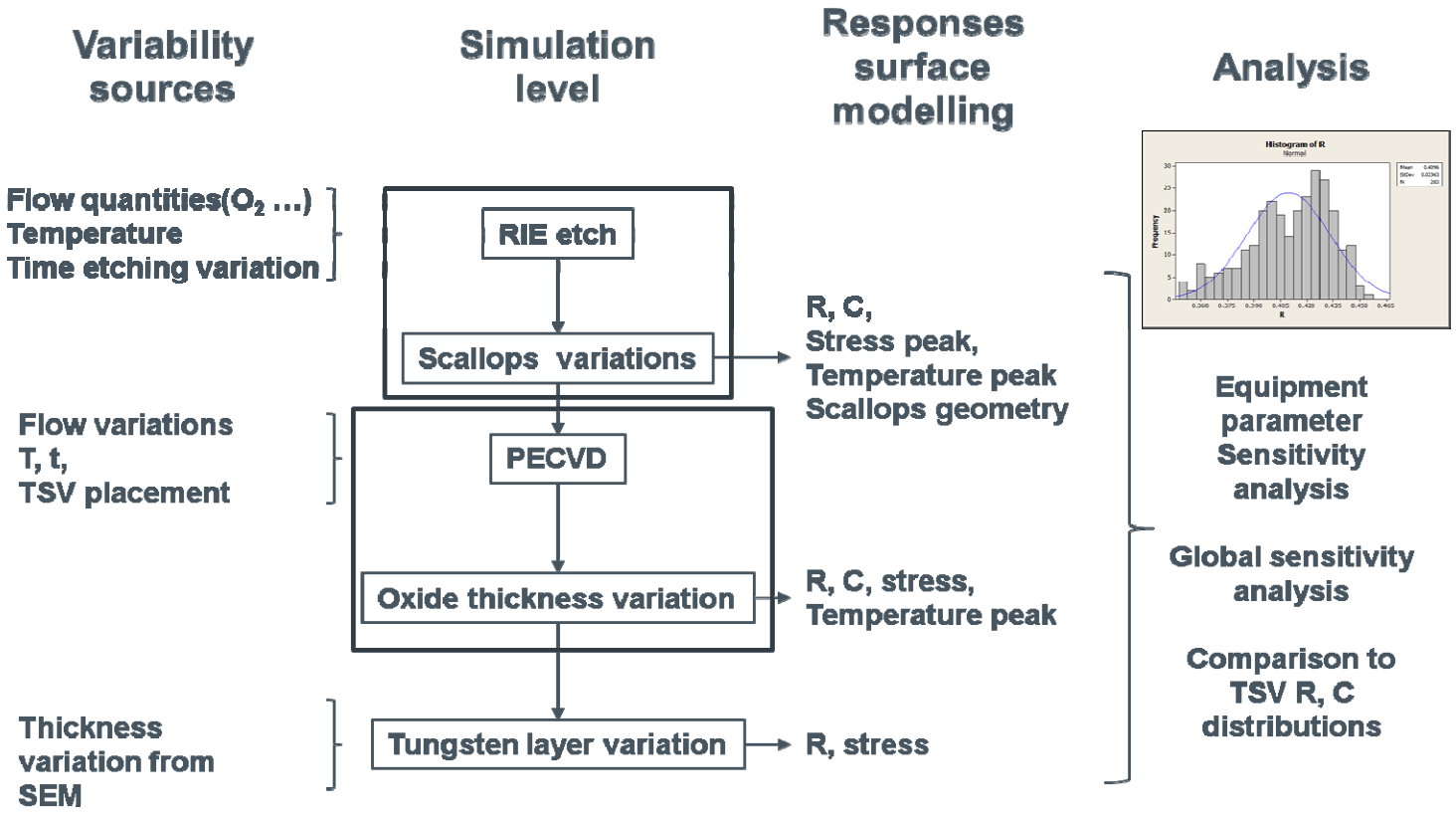
2.4

VARIABILITY ON PROCESS LEVEL

VARIABILITY GENERAL APPROACH

- Relation between variability sources and physical parameters of interest



Final result will provide R, C, stress function of equipment/process parameters

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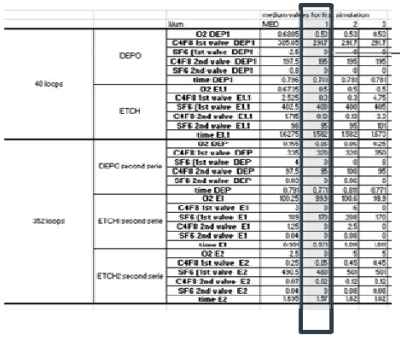
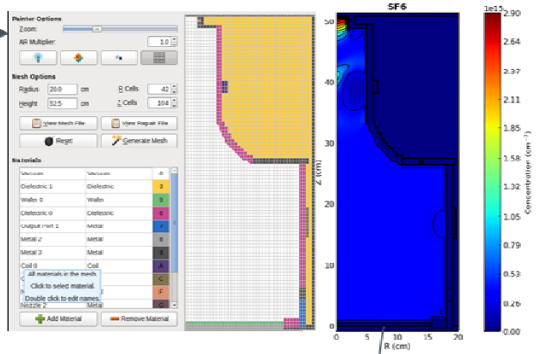
VARIABILITY GENERAL APPROACH

Simulation loop up to scallops

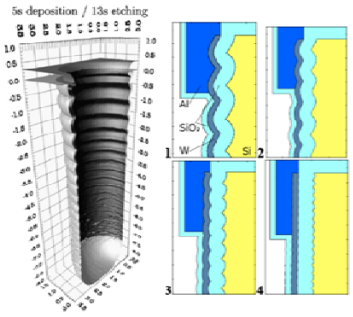
Parameters extraction from ams measurement

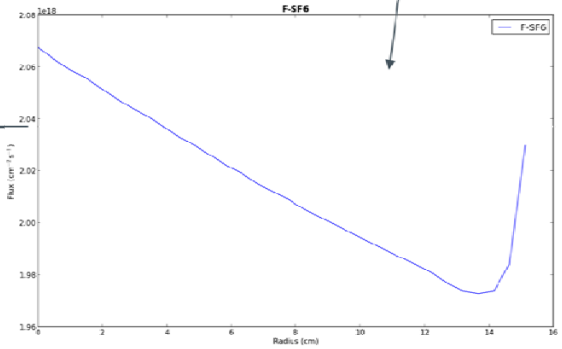




Species distribution in chamber during one sequence of DRIE process

Etching simulation at a wafer position 2D, 3D analytical/MonteCarlo





SF6 distribution on wafer surface at one sequence loop

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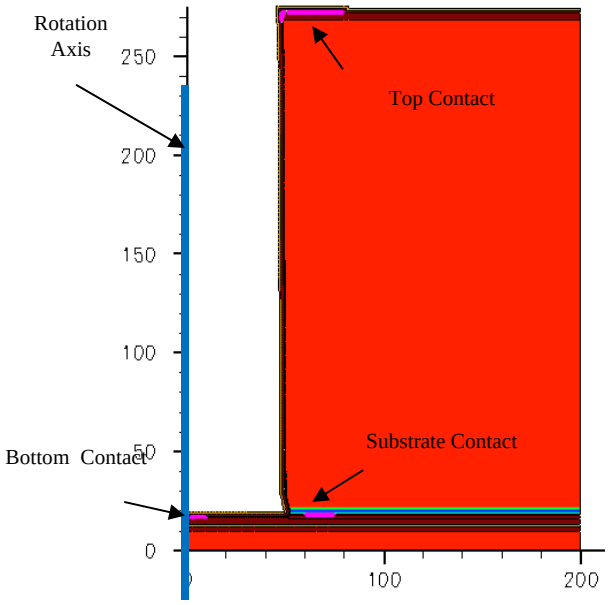
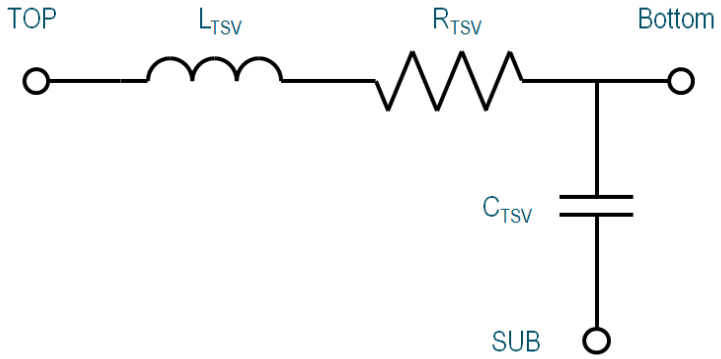
TSV ELECTRICAL CIRCUIT

- TSV can be described as a RCL circuit (including S-parameters in a quadripole model)
- Typical values in the GHz frequency range: LTSV=12pH, RTSV=0.35Ohm, CTSV=3.4pF
- Resistance and Capacitance can be measured but inductance is impossible





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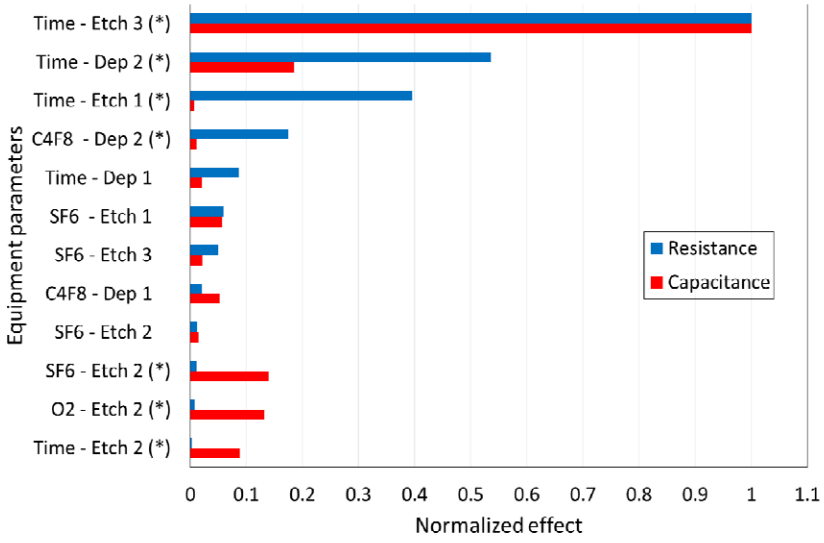
Page 28

RESULTS

- **Pareto graph** of relevant equipment parameters on **resistance and capacitance response**
- Resistance and capacitance are very sensitive to the second stage etch-dep cycle (Large scallops cycle)
- Morphological variations (scallops width and height) **do not generate** large R,C, L and stress variations. Therefore, variations on TSV electrical and mechanical properties must have another source. (e.g. oxide and tungsten deposition)



	% Variation		% Variation
Large scallops width	9.64%	**R (mOhm)**	1.08%
Large scallops depth	10.34%	**C (pF)**	0.70%
Small scallops width	28.89%	**L (pH)**	1.20%
Small scallops depth	32.58%	**Average stress (MPa)**	3.04%

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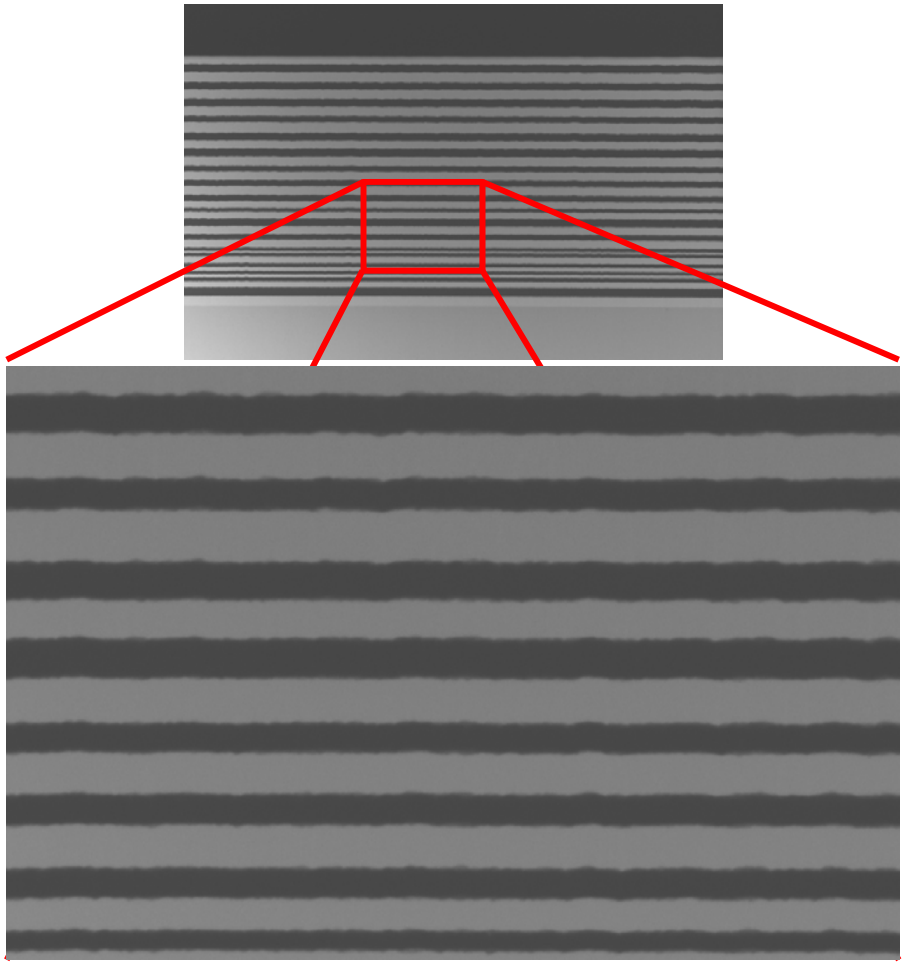
BENCHMARK B4



- Variability of interference filters and dielectric stacks
  - Overall system to model transmittivity by TMM method available.
  - MC based multivariate thickness variation of layer stack to model variability of transmission through stack has been implemented.
  - Furthermore the effect of layer roughness on transmittivity variation has been included into the benchmark

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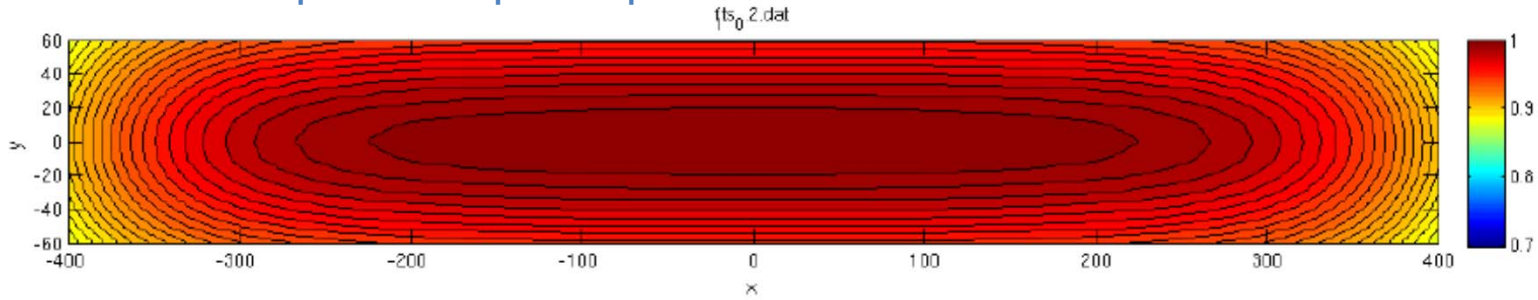
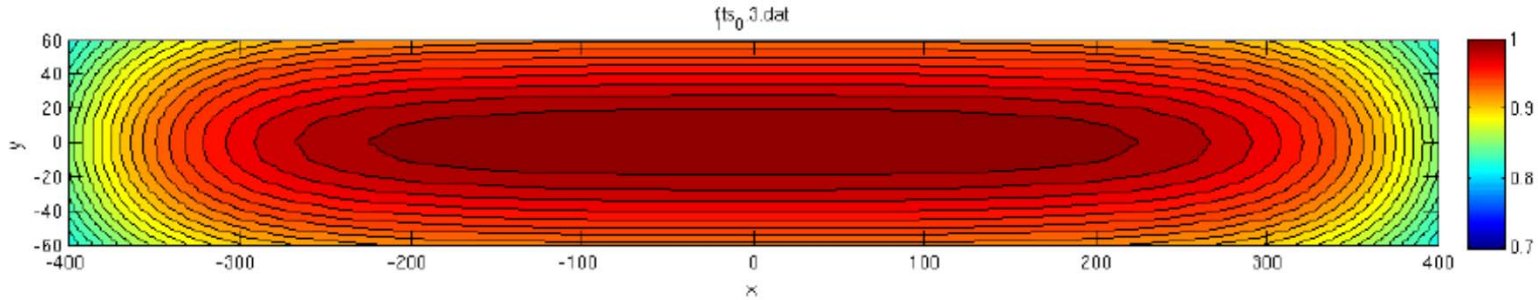
BENCHMARK B4

Dielectric Filter Sputter Dep.: Maps of relative thickness on substrate

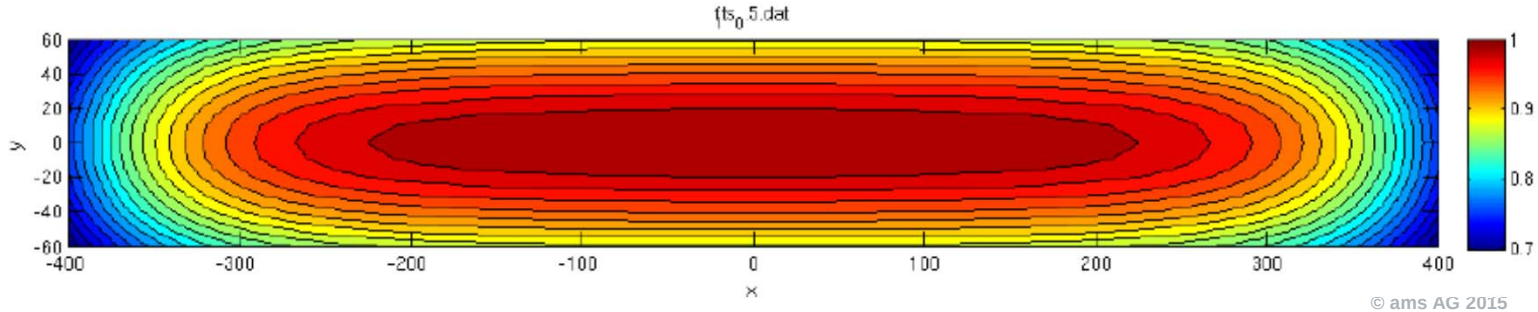
f_lts = 0.2



f_lts = 0.3



f_lts = 0.5



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3

CONCLUSIONS AND OUTLOOK

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CONCLUSIONS & OUTLOOK

- A multi-hierarchical simulation system to model the variability behavior of high-performance analog circuits has been shown
- The vertical integration of multiple levels (process, device, circuit, system) enables optimization of key sources of variability
- The established causalities between system behavior and underlying processing variability will enable new much higher optimized integrated systems in future.

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Campbell Millar, Gold Standard Simulations Limited.

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VARIABILITY-AWARE SPICE MODELLING AND CIRCUIT SIMULATION IN SUPERTHEME

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OUTLINE

1. Introduction
2. SPICE Model Extraction
3. Combined Global and Local Simulation
4. Process Variation and Local Variation
5. Conclusion

INTRODUCTION

- Design at advanced technology nodes REQUIRES accurate SPICE Models.
  - Reduces design cost and time to market
  - Design Right first time
- Systematic/Global variability and local mismatch can no longer be treated in isolation.
  - Complex and correlated
- Need a holistic approach to modelling Global and Local variability and reliability effects
- Design Technology Co-Optimisation (DTCO)
- Software and modelling methdologies which accurately capture the interplay between global and local variability and reliability.

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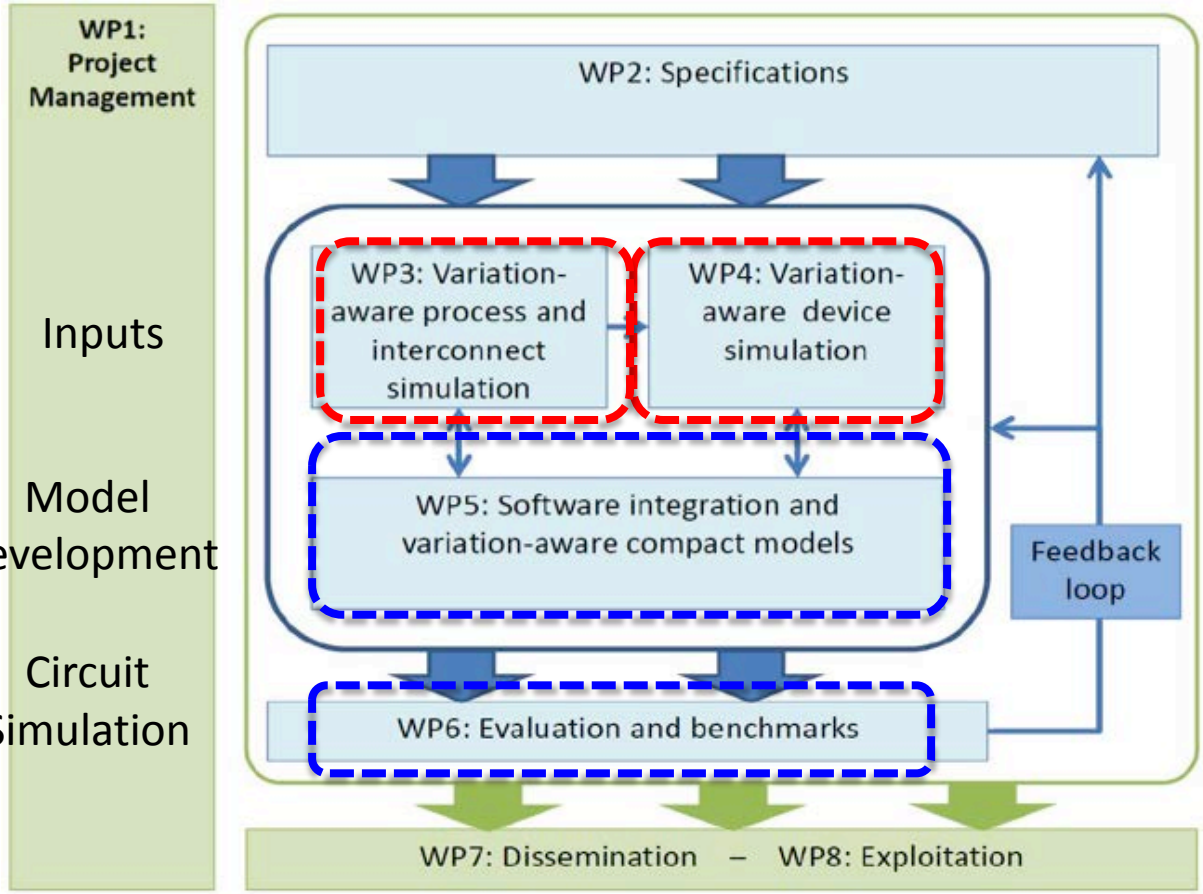
INTRODUCTION - CONTEXT



Collaborators

GSS

amun

Fraunhofer IISB

Fraunhofer IIS

University of Glasgow

INTRODUCTION - TOOLCHAIN

Full simulation tool chain

- Structure Manipulation/Translation
  - Monolith
- Device Simulation GARAND
  - DD, 3D Full Band MC , 1D Multi-sub-band MC
- Statistical SPICE Modelling
  - Mystic –SPICE Model extraction
  - ModelGEN – Advanced process and statistical aware SPICE Model generation technology
- Circuit Simulation
  - RandomSPICE – Statistical Circuit Simulation Engine
- Toolchain integration
  - Enigma – Automation and Integration framework

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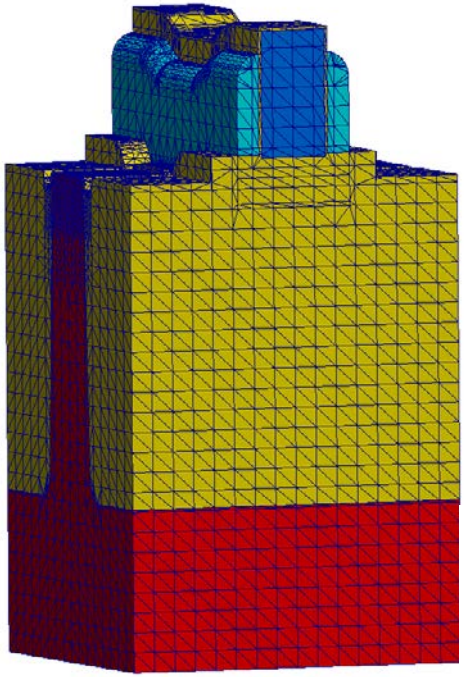
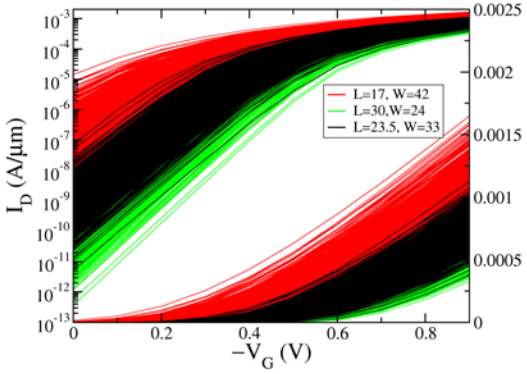
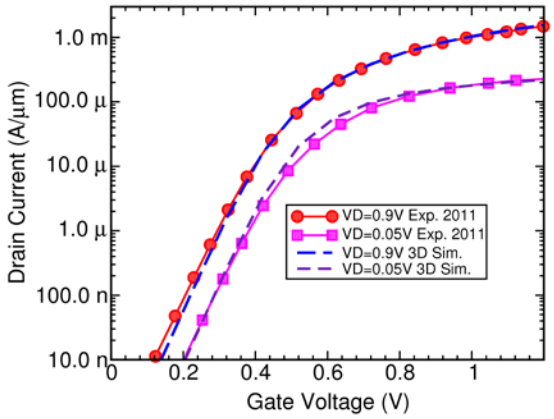
SUPERTHEME 20NM MOSFET







Process simulation (Sentaurus Process/ Dr Litho)

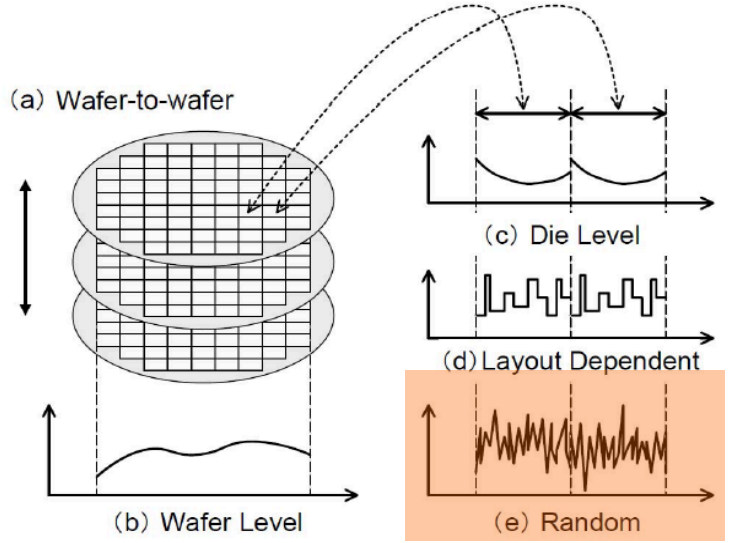
Mesh Conversion/Transfer (GSS Monolith)

Device simulation (GSS Garand)

SUPERTHEME

GSS

VARIABILITY DECOMPOSITION



(Takeuchi, Nishida, Hiramoto, SISPAD 2009)

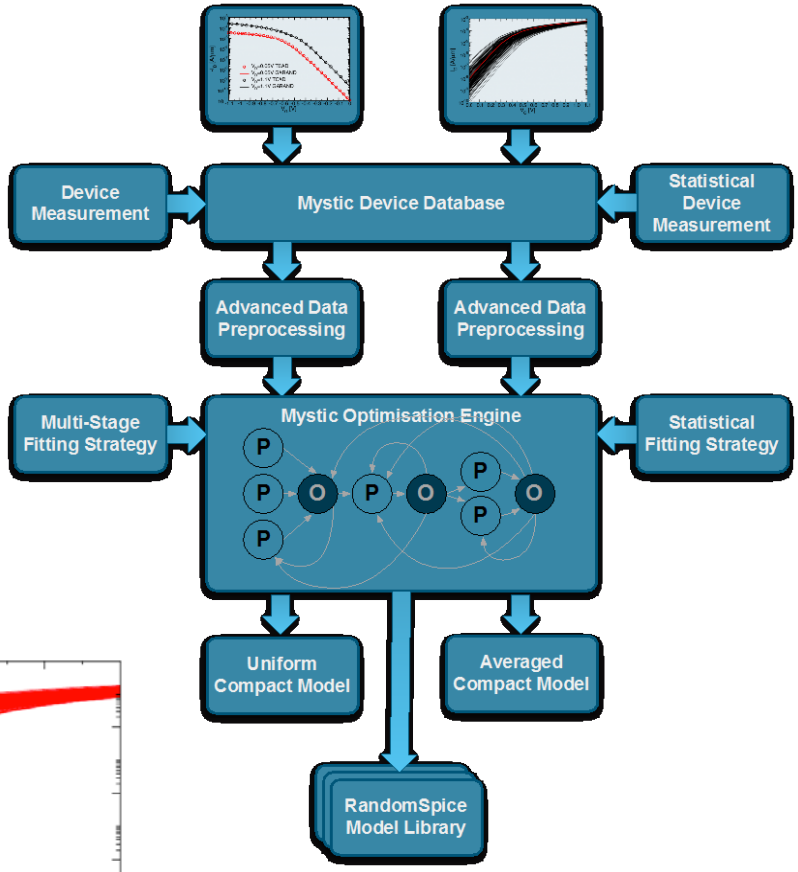
	Process	Environment	Temporal
Global	<L_g> and <W>, <layer thicknesses>, <R>'s, <doping>, <t_{ox}>, <V_{body}>	Operating temperature range, V_{DD} range	<NBTI> and Hot electron shifts
Local	**Line Edge Roughness (LER), Discrete doping, Discrete oxide thickness,** R and V_{body} distributions	Self-heating, IR drops	**Distribution of NBTI,** Voltage noise, SOI V_{body} history effects, Oxide breakdown currents
Across-chip	Line Width, due to pattern density effects	Thermal hot spots due to nonuniform power dissipation	Computational load dependent hot spots

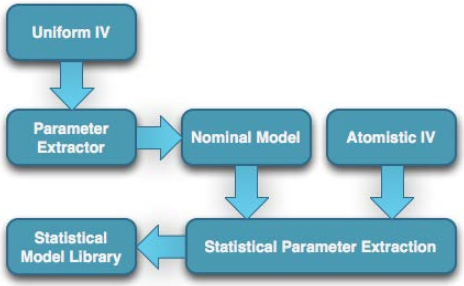
(D. Frank, IBM)

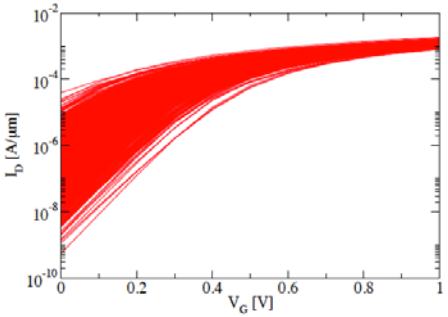
- In general, variability can be decomposed into global process variation and local random variability.
- Global Variability: systematic, spatially correlated, long-range.
- Local Variability: random, no (weak) correlation, short-range.

COMPACT MODEL EXTRACTION WITH MYSTIC

- Extraction of nominal and statistical compact models
- Flexible extraction based on state machine workflow.
- Supports PCA and ModelGEN
- ModelGEN preserves correlations between non-normal parameter distributions
- Unprecedented statistical accuracy

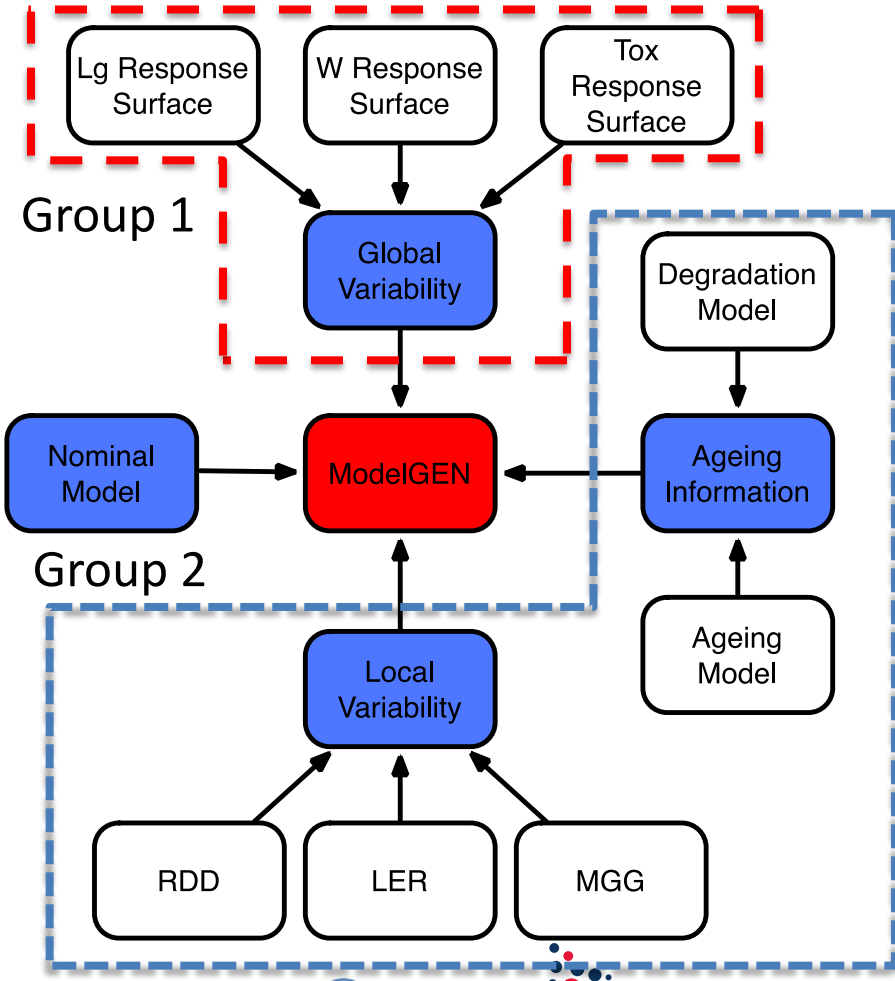






HIERARCHICAL MODELLING METHODOLOGY

- Multi-stage extraction process
- Nominal Base Model
  - Standard SPICE Model Extraction
- GV Process Aware Model
  - Identify Group 1 Model Parameters
  - Define DoE Space
  - Fit to TCAD process splits or Si
- LV Statistical SPICE Model
  - Identify Group 2 Model parameters
  - Simulate variability under appropriate GV conditions



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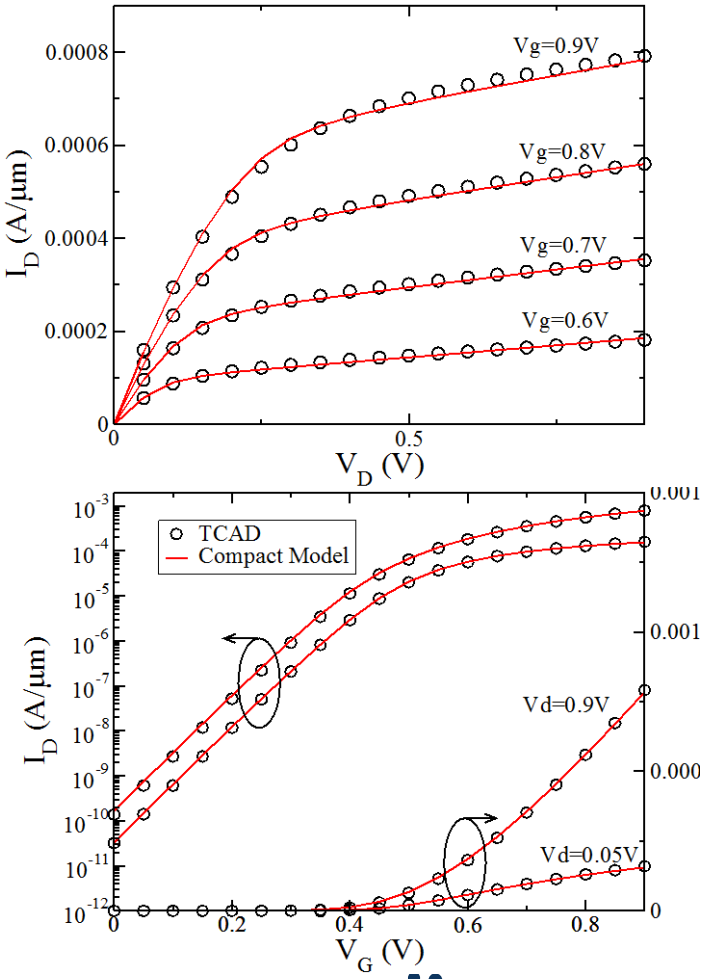
NOMINAL MODEL EXTRACTION

- Extract Base Model from TCAD using Mystic
- Full model extraction
- Uniform Doping
- Basis for variability model extraction
- Typically Target <2-3% error
  - Needs to cover range of W and L
  - Range of Temperatures

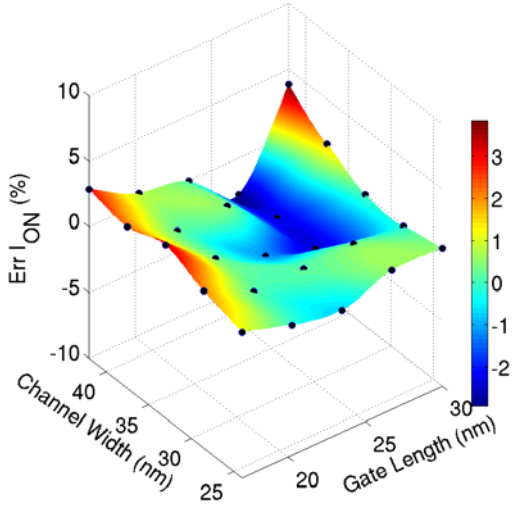


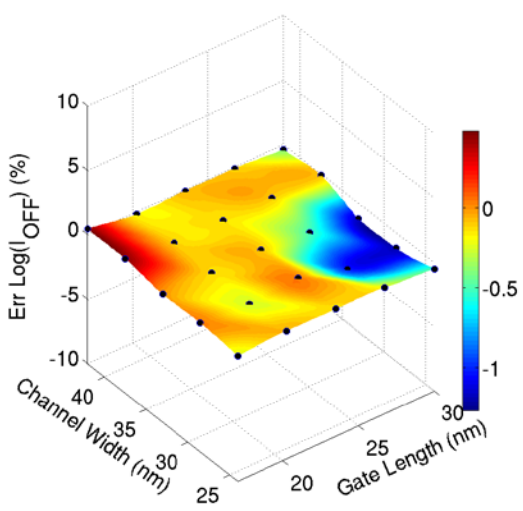
EXTENDED UNIFORM MODEL – GROUP 1

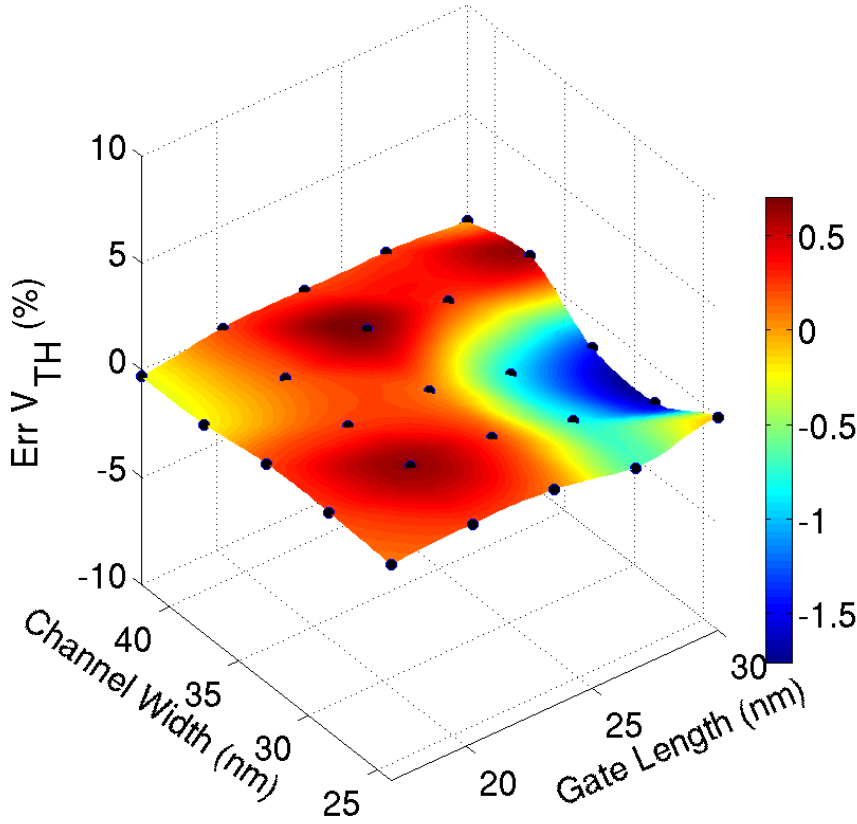
Group 1 Parameters - Subset of model parameters capture process/geometry variation

- 5 × 5 DoE space
- L_G=17, 20.25, 23.5, 26.75, 30
- W=24, 28.5, 33, 37.5, 42

Typical extraction <3% Fitting Error



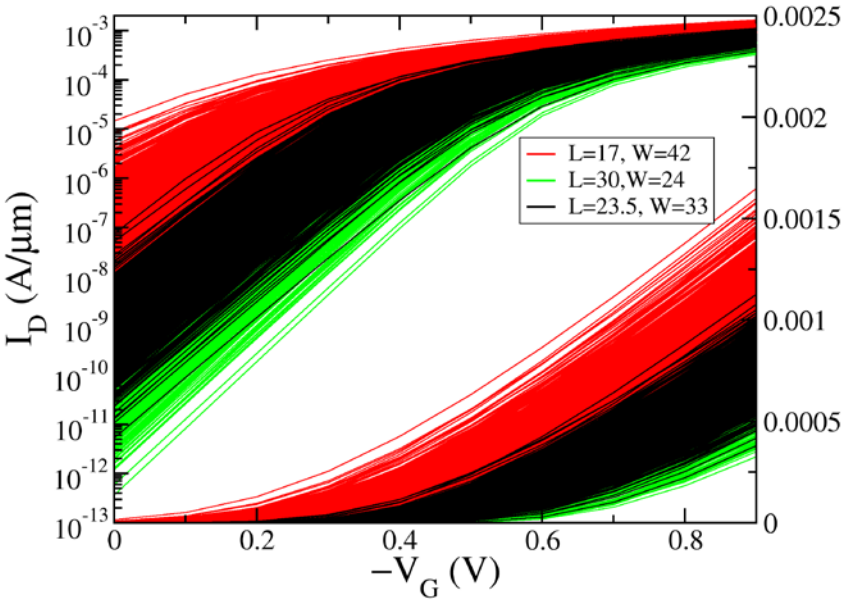


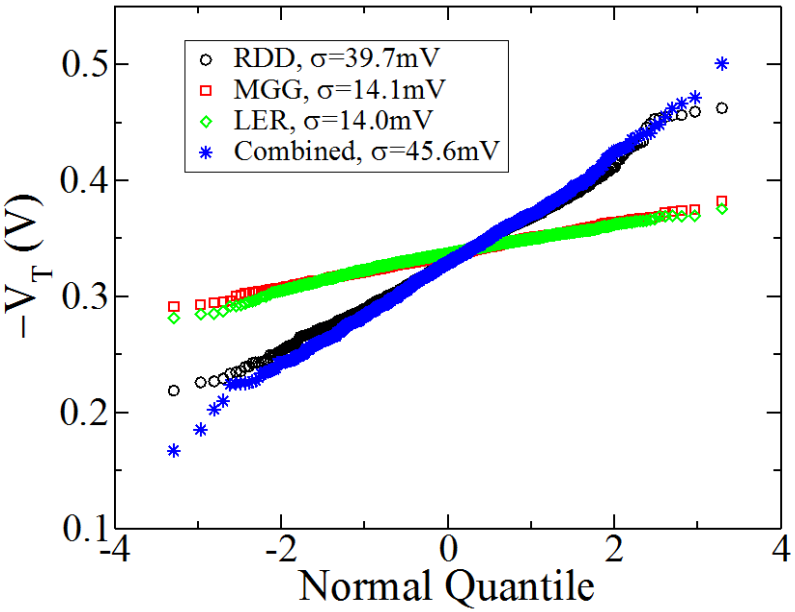


STATISTICAL MODELS - GROUP 2

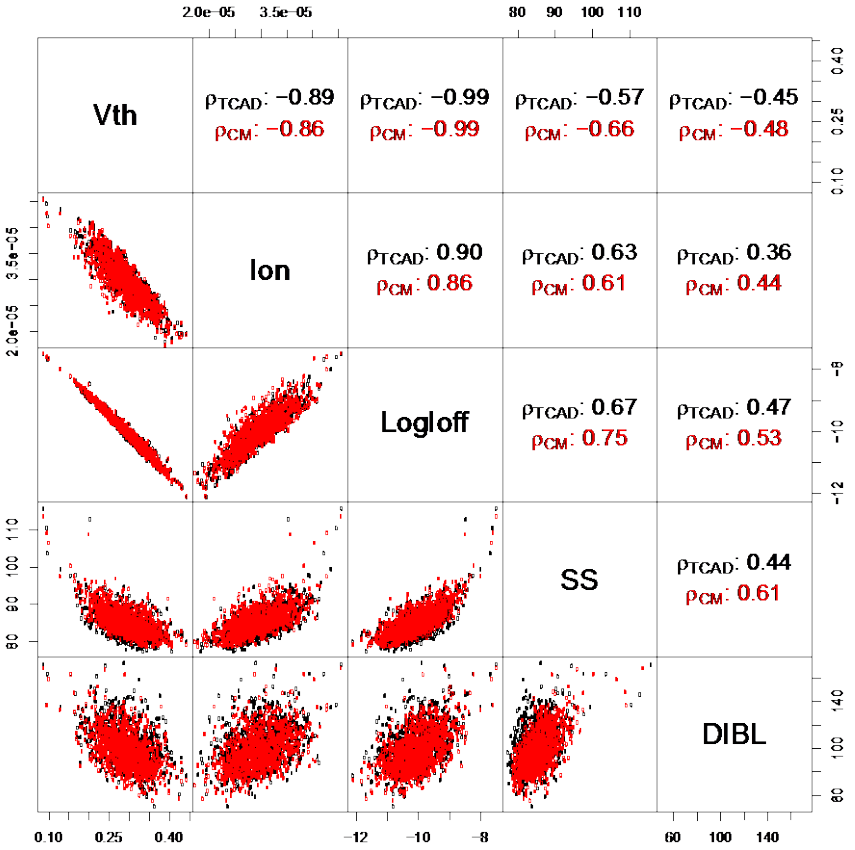
Group 2 Parameters - Subset of model parameters capture local variations and reliability

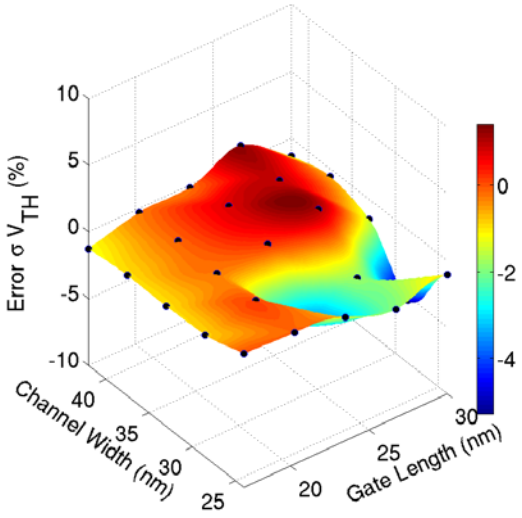
- 5 × 5 DoE space
- RDD, LER, MGG
- L_G=17, 20.25, 23.5, 26.75, 30
- W=24, 28.5, 33, 37.5, 42

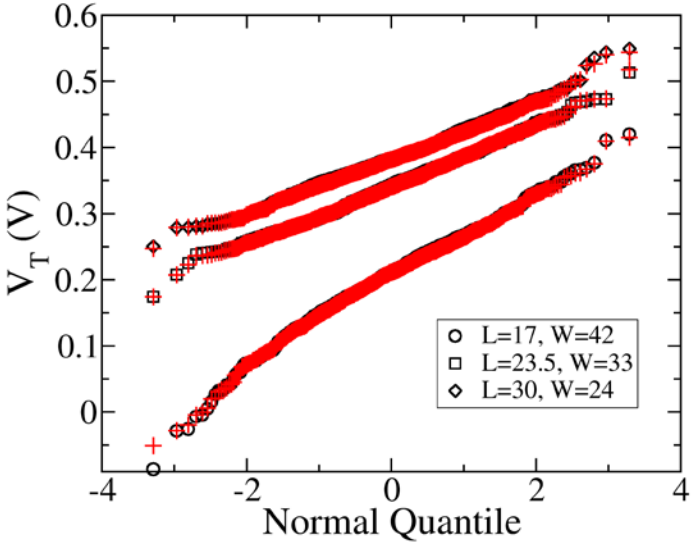




STATISTICAL MODELS



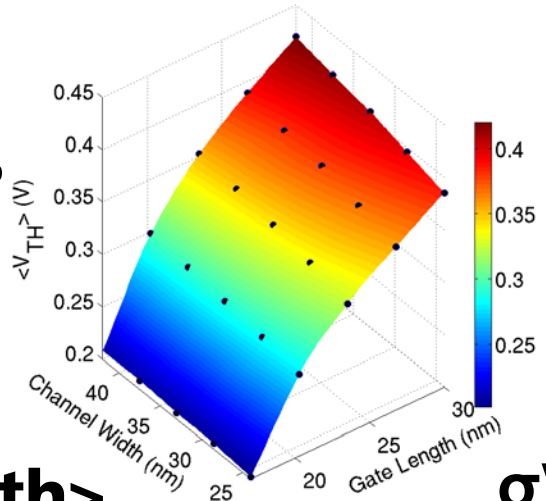




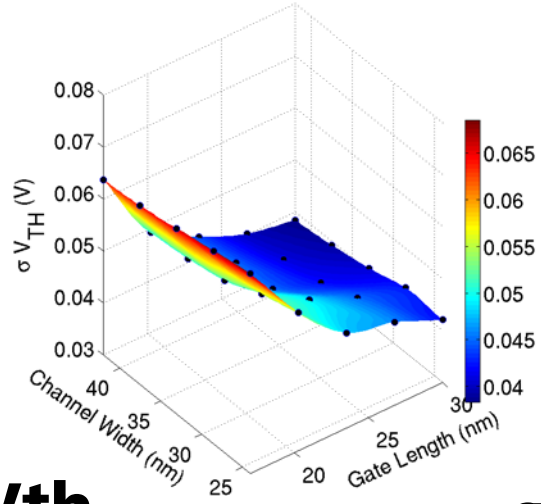
Accurately capture device variation including variations in SS and DIBL

LOCAL VARIATION RESPONSE SURFACES

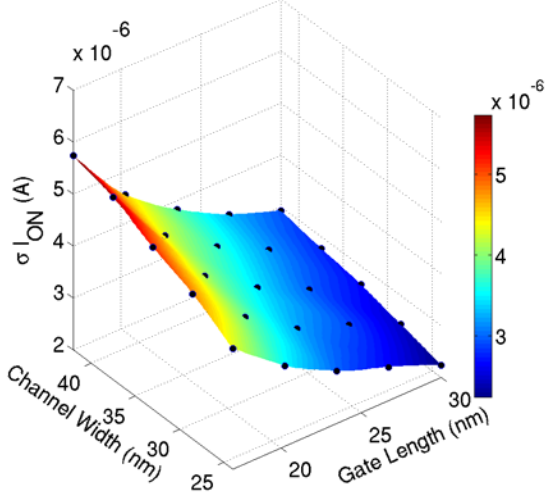
NMOS



<Vth>

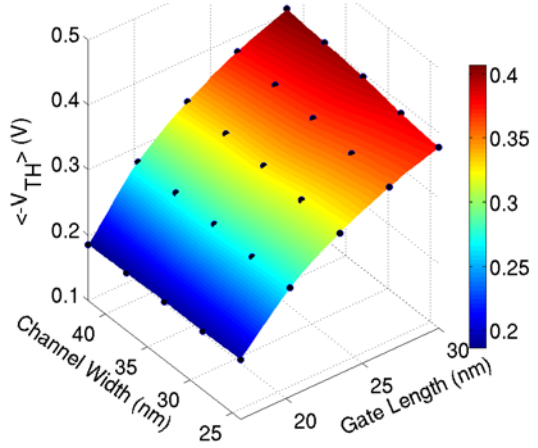


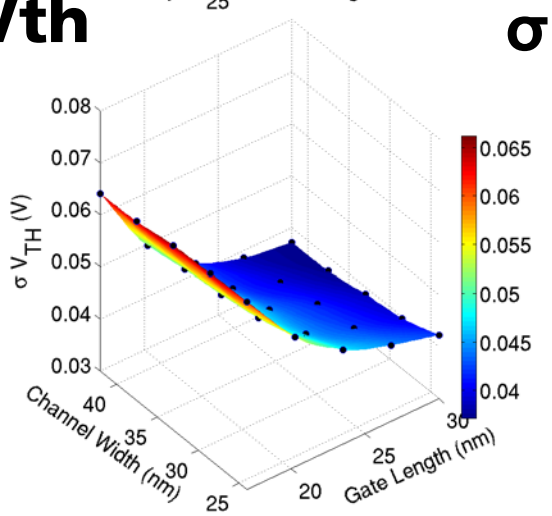
σVth

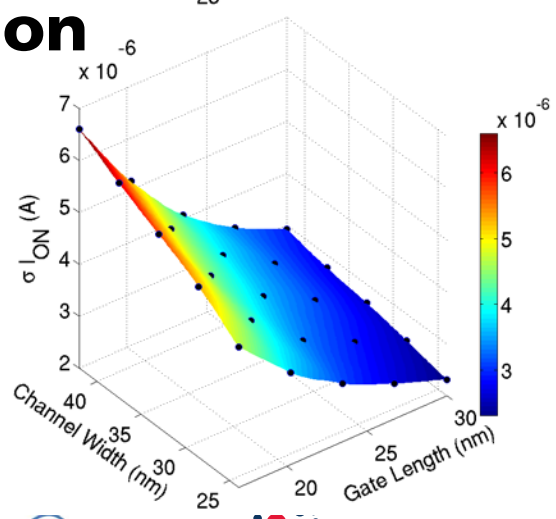


σIon

PMOS







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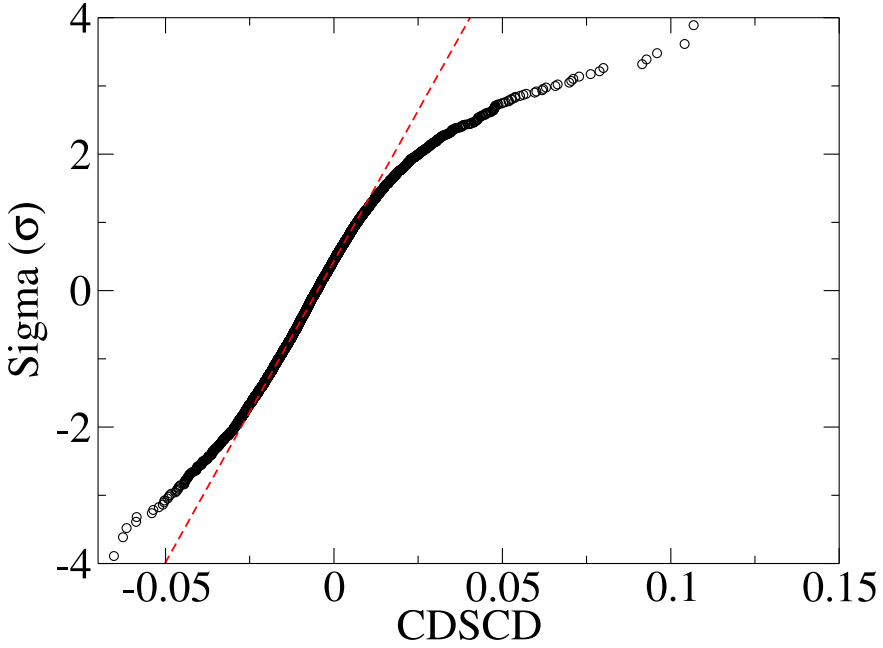
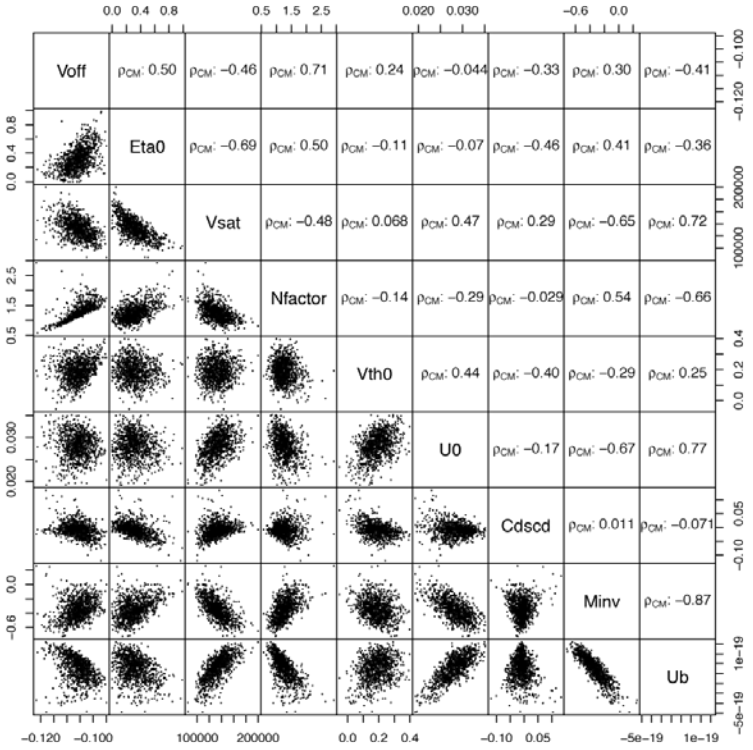
GROUP 2 PARAMETER DISTRIBUTIONS



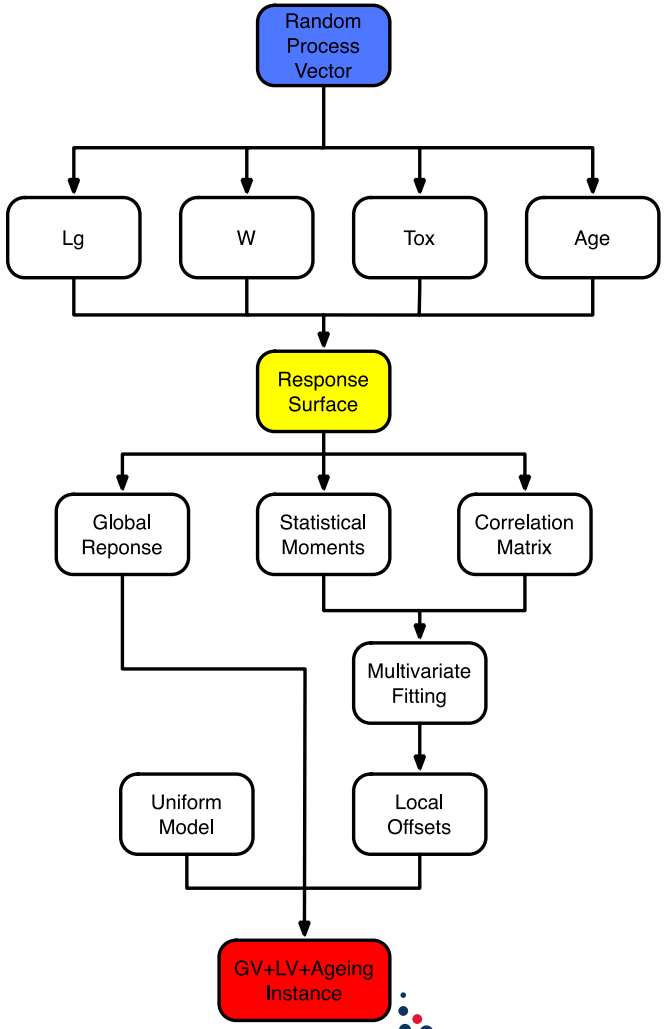


Distributions of SPICE model parameters for Group 2 are non-Gaussian and have complex correlations.

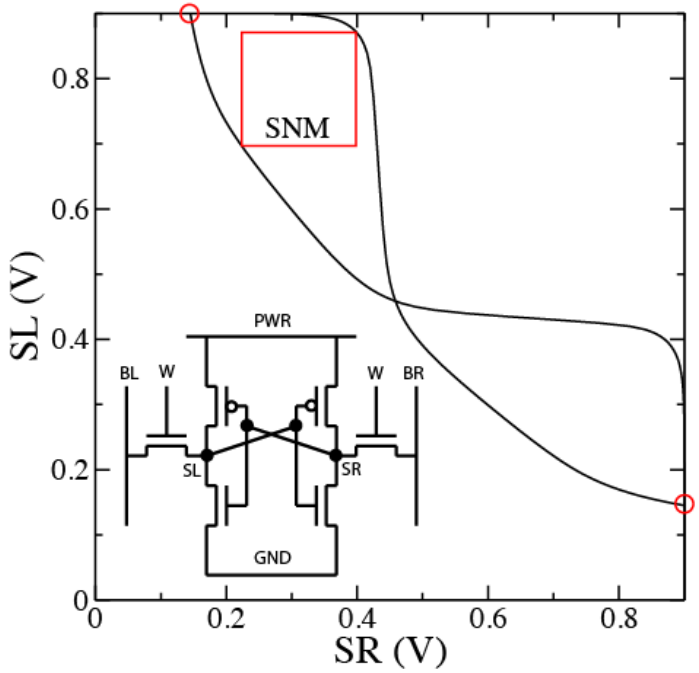
SUPERTHEME GSS

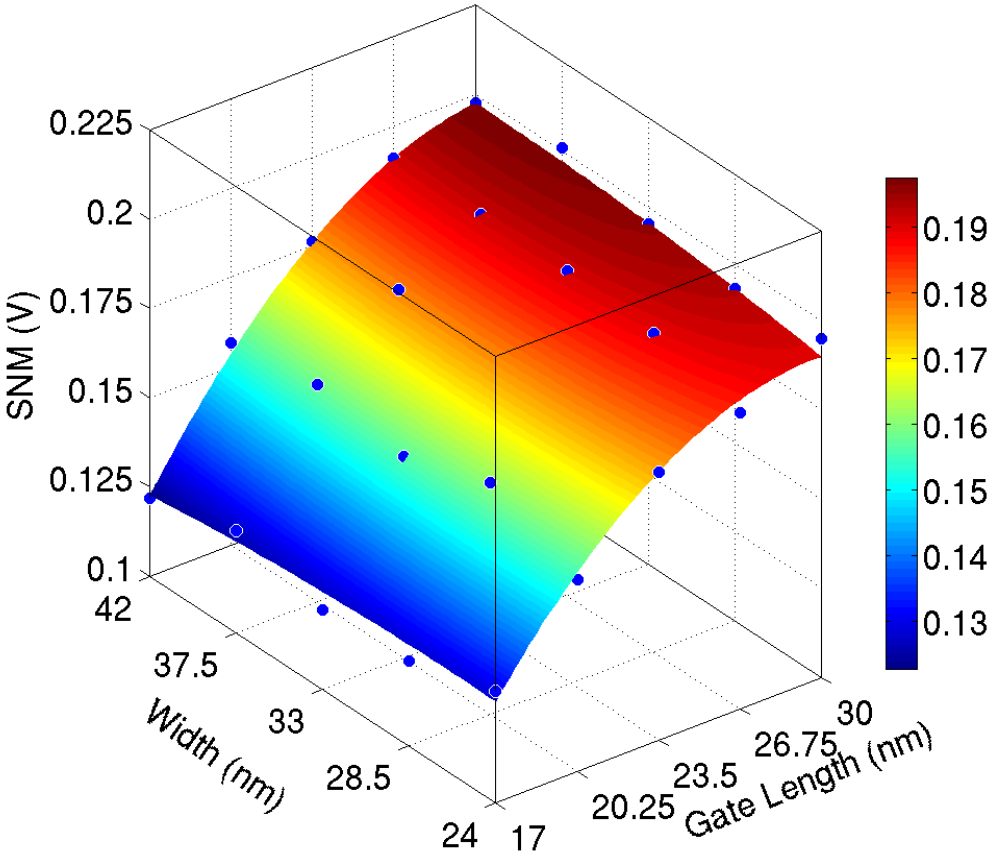
MODELGEN

- Highly accurate Compact Model Generation
  - Captures non-Gaussian distributions
  - Parameter correlations
- Models combined impact of
  - Global Variation
  - Local variation
  - Reliability and ageing
- Uses response surface models for GV
- Model interpolators used for
  - BTI-induced ageing response.
  - Local statistical variability information.
- GSS RandomSPICE Statistical Circuit Simulation Engine



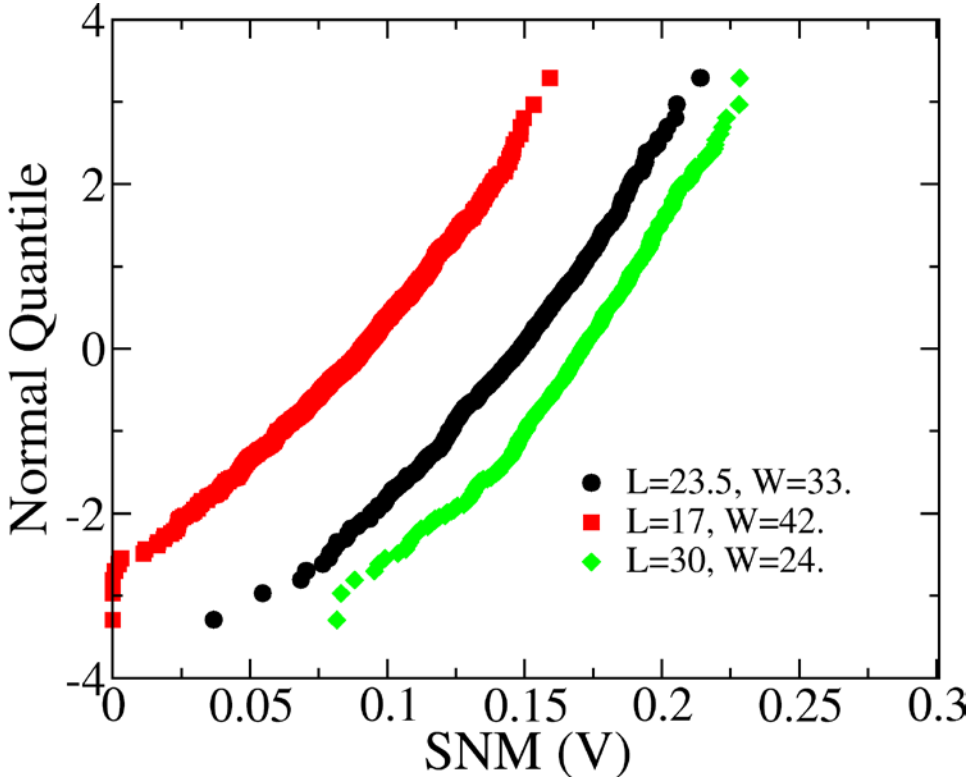
EXAMPLE: SRAM

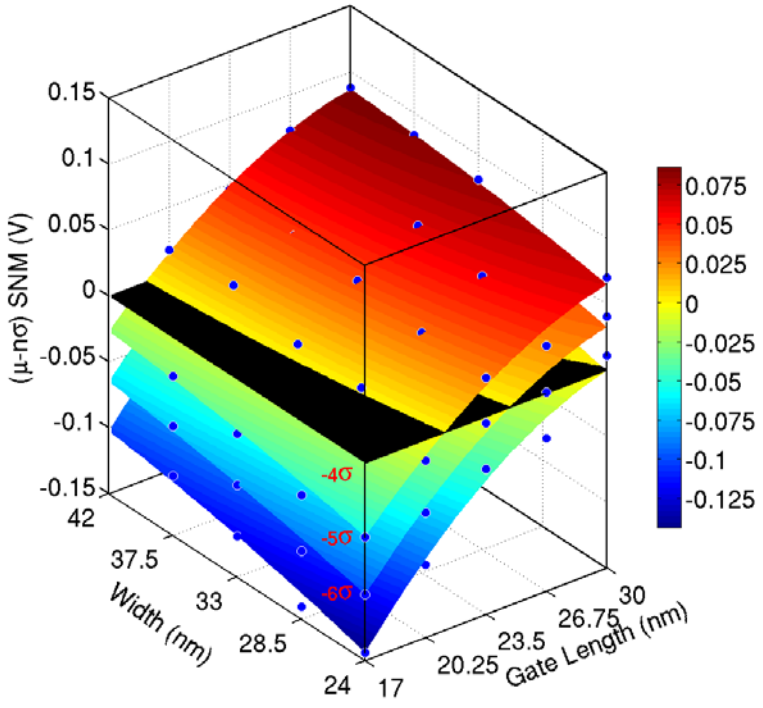




- 6T SRAM cell simulations
- ModelGEN response surface models
- Global PV has significant impact on SNM.

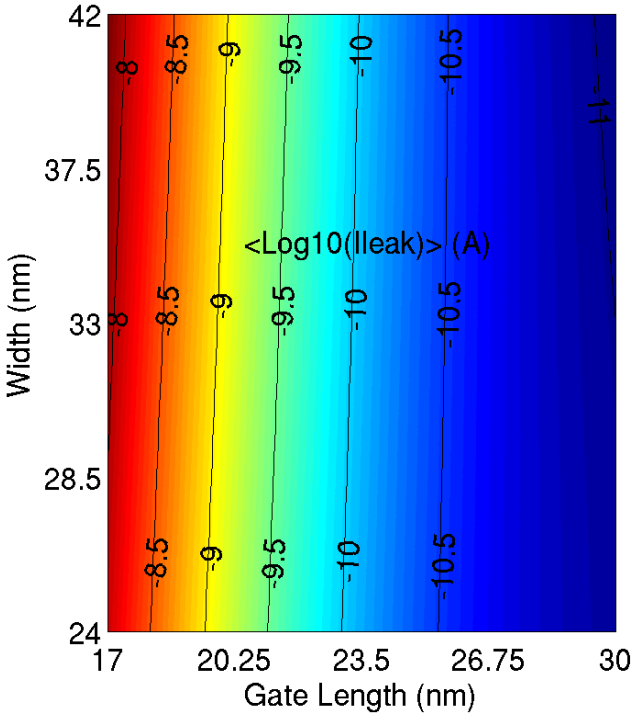
SRAM: SNM

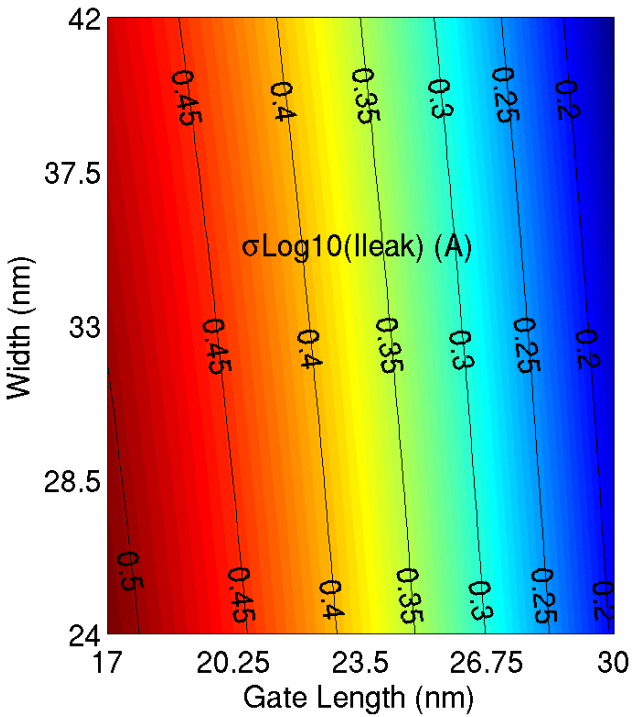




- Simulated SNM using RandomSPICE and ModelGEN Library
- Good control of PV is essential for yield.

SRAM: CELL LEAKAGE





- SRAM Cell leakage critical for IOT applications
- In this case Lg variation dominates due to strong short channel effects
- σIoff changes due to Vt shift as well as L dependent σVt
- Variation span 3 orders of magnitude.

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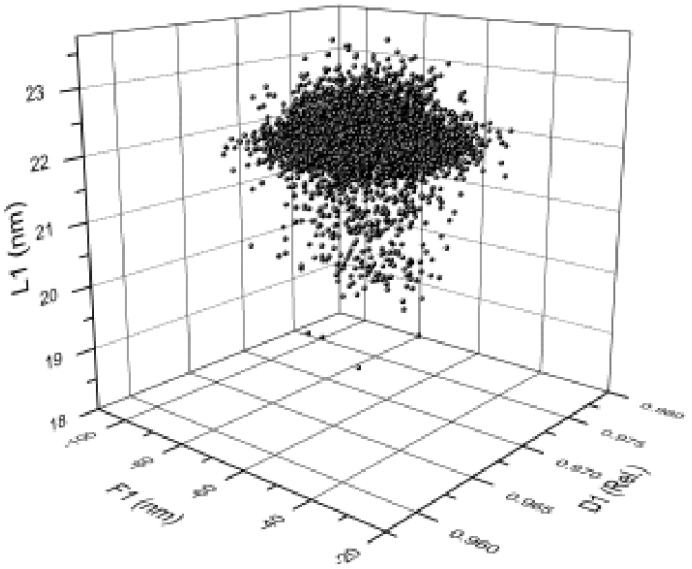
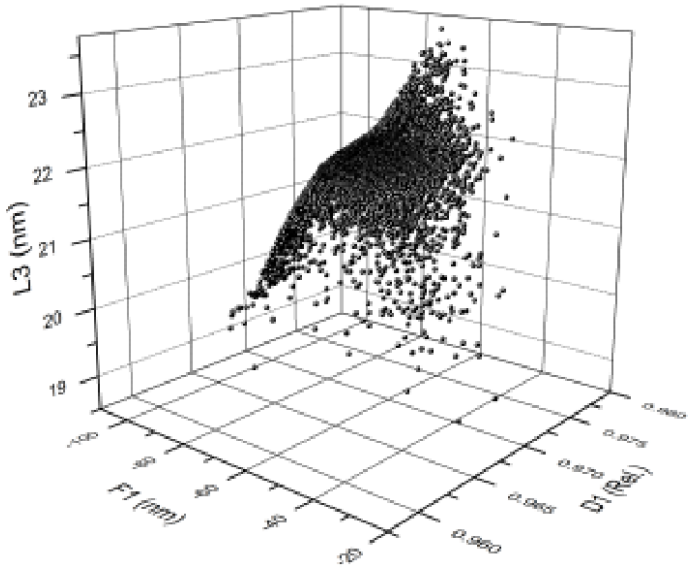
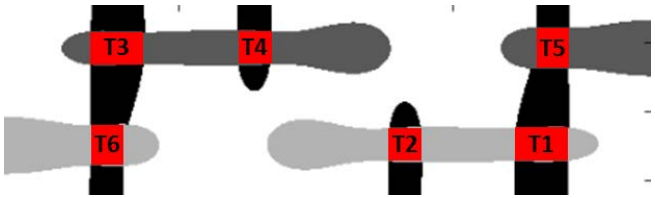
SUPERTHEME DEMONSTRATOR







- Variation in SRAM cell DC variation due to Litho random variation in Focus (F1) and Dose (D1)
- Horizontal lines need to be structured with LFLE double patterning. Simulated with Dr Litho.

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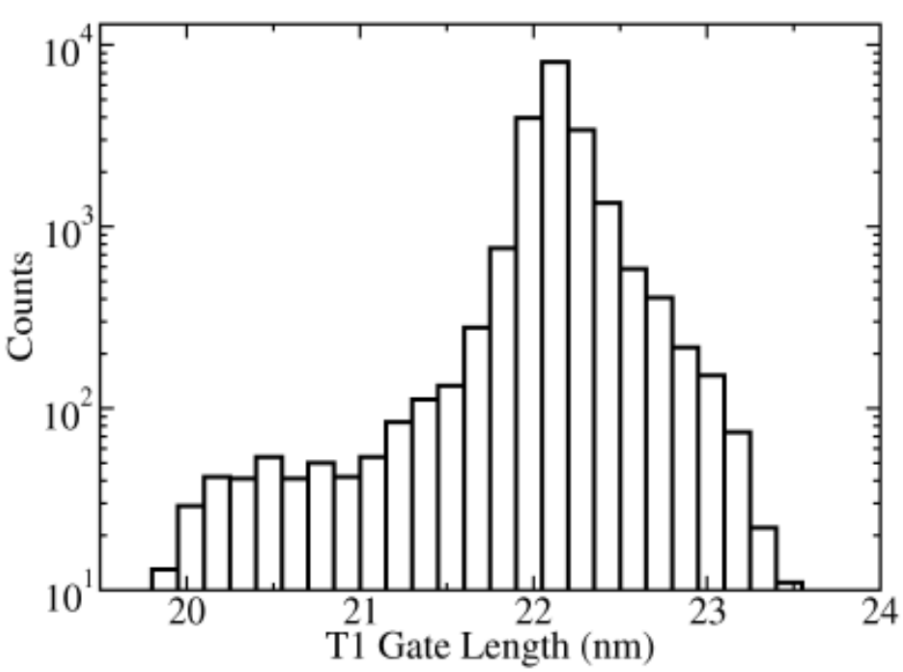
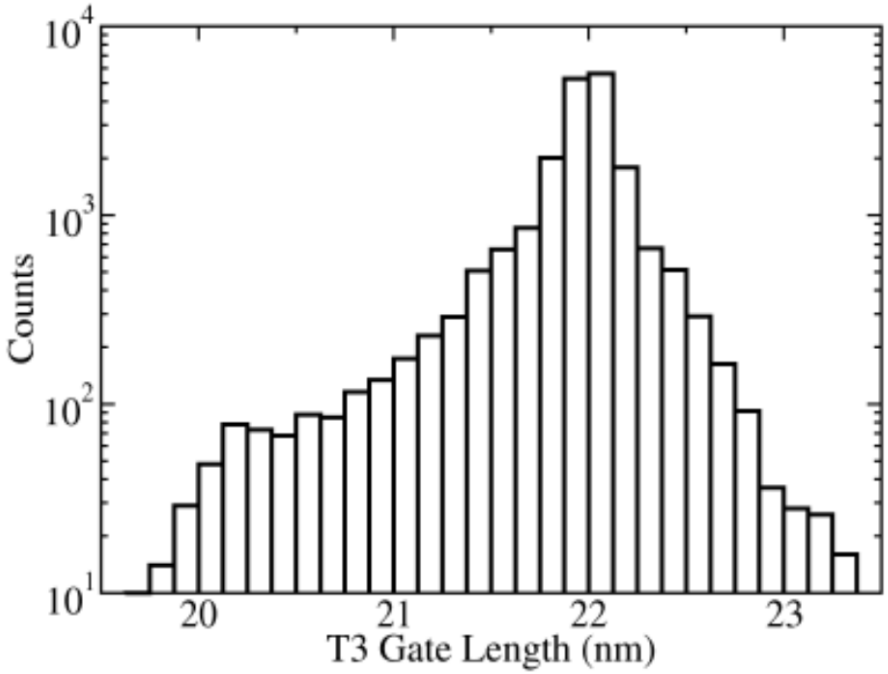
RANDOM CD VARIATION



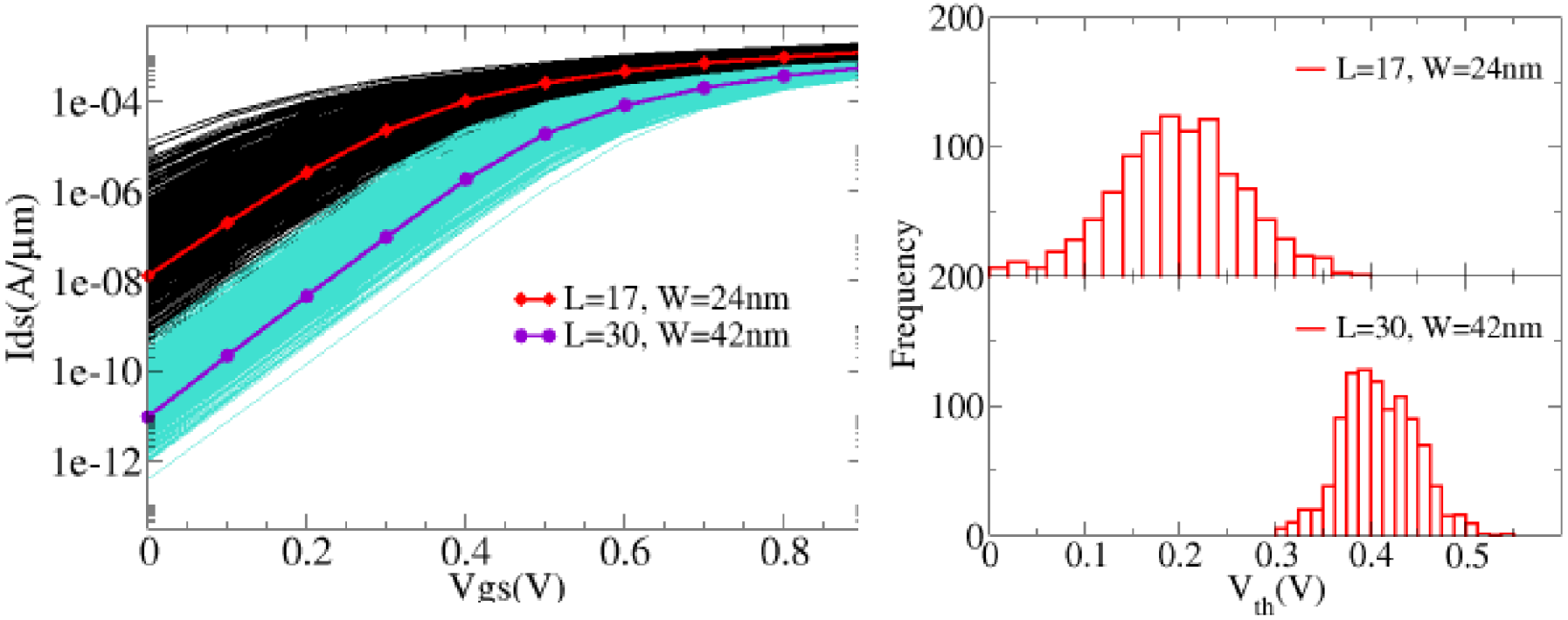


- Probability distribution of lengths of transistor T1 and T3
- Provided as input distribution to ModelGEN
- Simulated using Dr Litho from Fraunhofer IISB

SUPERTHEME

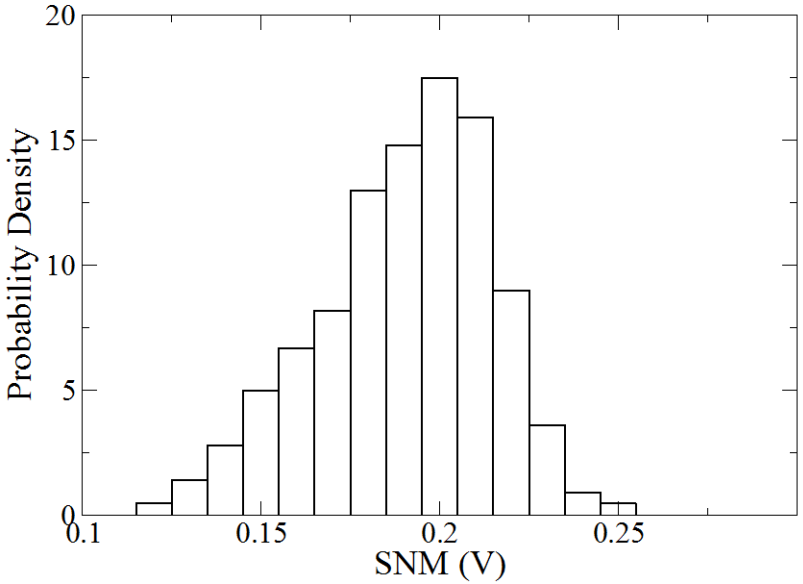
GSS

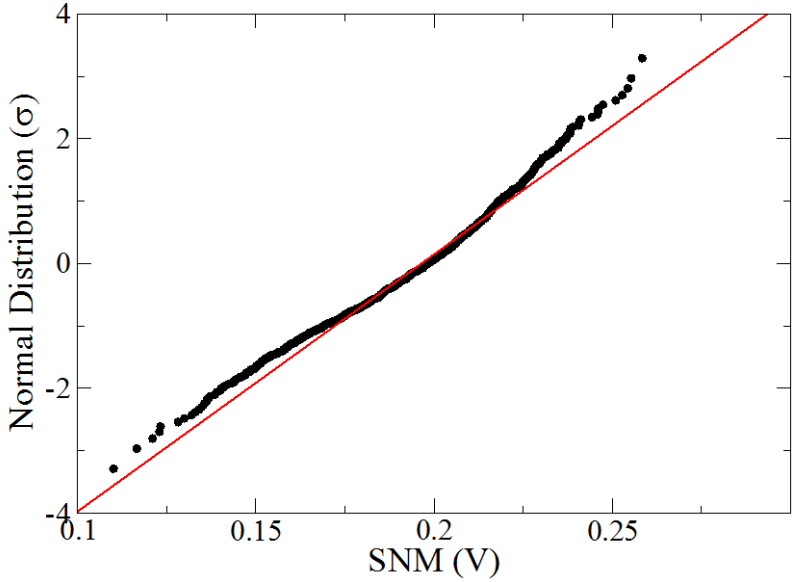
DEVICE CHARACTERISTICS



SPICE simulated IV-characteristics of 2 corner transistors due to GV in L and W resulting from combined lithography step and statistical variability due to RDD, LER and MGG.

SRAM SNM: COMBINED GV AND LV





- Example – SRAM SNM simulation in the presence of Combined Random GV and LV
- Produces multi-modal output distribution

CONCLUSIONS

- Performed comprehensive simulation of 20nm Planar Bulk MOSFETs
- At advanced technology nodes correlations between Global and Local variability require careful consideration
- Developed process and statistical variability aware compact modelling methodology and ModelGEN SPICE model generator to enable true TCAD DTCO flow.