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SUPERTHEME

ICT Project no. 318458

SUPERTHEME

Circuit Stability Under Process Variability and Electro-Thermal-Mechanical Coupling

D1.14: Final Project Report

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PROJECT FINAL REPORT

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4.1 Final publishable summary report

Executive summary

Among the physical limitations which challenge progress in nanoelectronics for aggressively scaled *More Moore*, *Beyond CMOS* and advanced *More-than-Moore* applications, process variability and the interactions between and with electrical, thermal and mechanical effects have got more and more critical. Effects from various sources of process variations, both systematic and stochastic, influence each other and lead to variations of the electrical, thermal and mechanical behavior of devices, interconnects and circuits. Correlations are of key importance because they drastically affect the percentage of products which meet the specifications. Whereas the comprehensive experimental investigation of these effects is largely impossible, modelling and simulation (TCAD) offers the unique possibility to predefine process variations and trace their effects on subsequent process steps and on devices and circuits fabricated, just by changing the corresponding input data. This important requirement for and capability of simulation is among others highlighted in the International Technology Roadmap for Semiconductors ITRS.

However, before the beginning of the SUPERTHEME project several critical gaps and weaknesses strongly limited the usability of simulation to study the impact of variations. First and most important, available software systems did not allow for the simultaneous treatment of equipment-induced systematic variations and stochastic variations caused by the granularity of matter. This limitation was removed in SUPERTHEME by various software development and integration results, based on own and third-party software ranging from third-party equipment simulation tools via proprietary topography simulation and third-party doping simulation programs to proprietary statistical device simulation tools. A key requirement for this hierarchical variability simulation was the generalization of the statistical device simulator GARAND of the SUPERTHEME partner GSS for arbitrary device geometries, and the development and implementation of additional physical models as far as strictly needed. The second critical gap was the lack of variability and/or correlation aware compact models. In turn, a key activity and achievement of SUPERTHEME was the development of hierarchical compact models which include both variability and correlations. Third, electrical, thermal and mechanical effects must be included and partly be simulated in parallel. IN SUPERTHEME this was enabled by the extension of required physical device models by the corresponding extension of the hierarchical compact models. Finally but also important, the lack of data for equipment-induced process variations was removed by an inventory of the sources of variations and the quantification of the sources of equipment-induced variability in some exemplary cases.

Whereas due to the Call for Proposals addressed by SUPERTHEME benchmarks conducted in the project focused on advanced *More-than-Moore* applications, the software development and integration results obtained are both important for advanced analog applications, where especially matching plays a key role, and for aggressively scaled digital applications. Concerning these latter *More Moore* applications, the variability of state-of-the-art planar and FinFET transistors was addressed, especially focusing on variation-aware compact models.

The project has fully met the technical objectives defined in its workplan and widely disseminated its results to the scientific community at conferences, workshops, via journal papers and via the SUPERTHEME WWW page. Internal exploitation of project results at partners' site and commercialization of software results via the SUPERTHEME partner GSS have already achieved very good results.

Project context and objectives

In order to cope with the challenge of the variability of process steps in the fabrication of semiconductor devices, it is imperative to trace variability from its source. Variability is generated by nonidealities of process equipment (e.g. focus shifts or lens aberrations in lithography, etch rates varying between different wafers, across a wafer or between neighboring structures due to plasma effects, varying angles of attack or pattern effects, insufficient reproducibility of temperature profiles or pattern-dependent effects in millisecond annealing steps, ….) or statistical effects like dopant fluctuations (important especially for short and narrow, lowly doped channels) and then propagated through subsequent process steps until the devices are final. Pattern-induced changes of device properties (e.g. iso-dense bias, pattern-depending effects of mechanical stress, …) need not be considered here because they do not change from wafer to wafer and can be compensated by appropriate changes in the technology used (e.g. the standard optical proximity correction in lithography).

The variability of the device performance and its reliability needs to be extracted, and this information must be passed up to the design level. This would allow to quantify the impact of variations and fluctuations on devices and circuits. Then it would be possible to investigate whether these variations or fluctuations push a too large percentage of the final product out of specifications, thereby reducing yield or even hampering manufacturability. Simulation can then also help to find the remedy for these yield losses and manufacturability problems, by assessing whether a modified device architecture or process flow may improve the situation, or whether the source of variability must be attacked by changing the process in question or perform some modification or improvement at the equipment.

This holistic approach has of course huge industrial benefits. However, to enable this, **two main problems needed to be and were solved in SUPERTHEME**:

- First, all simulation tools used in this sequence of combined process/device/circuit simulation must simulate not only the nominal process and device but also their variations with sufficient accuracy. Besides the quality of the physical models used this also requires that the results are not invalidated by numerical errors e.g. due to discretization according to the meshes used, or interfacing between different tools and simulation levels.
- Various simulation tools dealing with the different simulation levels, from the individual process steps through device up to circuits and systems must be suitably interfaced. A key problem here is that at process and device level a single device is discretized with about hundred thousand mesh points in a (three-dimensional) numerical process/device simulation, whereas at circuit level a large number of devices must be described. This requests data reduction and necessitates the use of suitable compact models, which are also the interface for transfer of results to the system and design level.

The SUPERTHEME project focused on the missing links for the simulation of process variations and their impacts on device performance and reliability. Therefore, it was based on the usage, extension and integration of existing own and third party simulation tools, and **addressed the improvement of the individual physical models and simulation tools just as far as these improvements were needed for the simulation of variability:**

- Lithography simulation: Within SUPERTHEME the proprietary lithography simulator Dr.LiTHO [1] of Fraunhofer IISB has been used, which has been proven outside the project to be at least comparable and in several cases superior to external commercial tools in terms of generality of the structures to be simulated, and minimization of the computation times needed.
- Simulation of deposition and etching: The topography simulation modules of IISB in the field of etching and deposition, used in SUPERTHEME, are representative for the state-of-the-art. However, still several drawbacks existed in this field. The geometrical evolution was still not

satisfactory in many cases, even for purely solid modeling operations. An important aspect for improving the predictability of topography simulation has been the coupling of feature scale modeling with equipment scale modeling. **Both issues have been addressed in SUPERTHEME.**

- Simulation of ion implantation, diffusion and oxidation: For the simulation of these process steps, the simulator Sentaurus Process [2] from Synopsys is something of an industrial standard and has also been used in SUPERTHEME, and other tools have been interfaced to this software via the well documented DF-ISE file format. Concerning variability, so far the most critical processes within this domain are various very short-time annealing processes. Within the earlier FP7 project ATEMOX [3] among others models for melting laser annealing processes were developed and implemented within Sentaurus Process.
- Device simulation: The main sources of statistical variability in decananometer transistors are the random distribution of discrete dopants and charged defects, and the line edge roughness and the granularity of the materials forming the gate material. Various approaches to deal with these effects, such as the impedance field method used in Sentaurus Device [2] and the handling of individual charges by charge smearing, face severe limitations and problems. The GSS 3D statistical TCAD simulator GARAND [4] handles physically correctly the impact of discrete charges in drift diffusion simulations by introducing simultaneously quantum corrections for both electrons and holes [5]. It also handles native and seamlessly all known sources of statistical variability including random dopants, trapped charges, line edge roughness, interface roughness and material granularity in contemporary bulk transistors and new transistor architectures. However the superposition of systematic and statistical variability was a challenge for GARAND and was therefore addressed in SUPERTHEME.

  Problems related to statistical aspects of reliability are of great importance to analogue circuits. In combination with random discrete dopants, the statistical nature of discrete trapped charges on defect states at the interface or in the gate oxide associated with hot electron degradation and negative/positive bias temperature instability (NBTI/PBTI) and hot carrier injection (HCI) result in relatively rare but anomalously large transistor parameter changes, leading to loss of performance or circuit failure. Although present simulation tools like GARAND can handle the electrostatic impact of such trapped charges in the simulations there are no suitable mobility models that can handle their impact on mobility and transport. The progressive BTI degradation results in increasing noise which is of great importance for analogue applications but currently cannot be predictively simulated in TCAD tools.

  In view of this background, within SUPERTHEME two key limitations in the area of device simulation were addressed and removed:

  - **The simultaneous treatment of systematic variations** which are largely caused by non-ideal equipment **and of statistical variations** resulting from the discreteness of charge and the granularity of matter **was not available before the project, and was enabled in SUPERTHEME.**
  - The physical models utilized in statistical device simulation e.g. using GARAND, were not satisfactory to cover interface or thermal effects, or noise. **Also this limitation of physical device models required for variability simulation was removed in the project.**

- Simulation of interconnect reliability: Three-dimensional (3D) integration technology using Through-Silicon-Vias (TSVs) is a critical building component to enable the fabrication of 3D systems which connect various technologies and allow high density packing, lower power consumption, and multi-functionality. However, there are still many concerns regarding TSV reliability. Process induced variations of TSVs can lead to large differences in interconnect

performance. The bottom of a TSV is considered to be a critical reliability site. Geometry and layout variations in this region can cause a large variation in interconnect lifetime and generally make the prediction of failure behavior difficult. **Therefore, in SUPERTHEME the impact of geometry feature variations on interconnect reliability was studied.**

- Compact modeling: The standard approach of using three sets of SPICE models with low, normal and high performance among others suffers from its missing capability to trace correlations between the sources of variability and the figures of merit for device performance. The corner analysis which uses different combinations of the best and the worst performance devices can only evaluate limiting cases. In the Monte Carlo method which is implemented in the state-of-the-art circuit simulators such as SPECTRE of Cadence [6] and HSPICE [2] of Synopsys, a chosen set of the SPICE model parameters is varied randomly according to the distributions of these parameters. However, for typical circuit sizes this approach soon becomes prohibitively expensive. **Within SUPERTHEME, fully process and variation aware compact models were developed and demonstrated. This has enabled the study of the simultaneous impacts of systematic and stochastic process variations on circuit behavior, and also established the interface to use results from SUPERTHEME in the design community.**
- Electro-thermo-mechanical simulations: The electrical performance and stability of electronic circuits, especially of analog circuits, is impacted by temperature and mechanical stress. Temperature variations appear due to self-heating of integrated circuits. Under certain conditions (different materials, high voltage and current) mechanical stress is induced in the chips when temperature increases due to self-heating. This mechanical stress may change the electrical performance of the devices in the circuit leading to some additional performance variability. Such kind of variability was so far neglected in simulations of electronic circuits, but was addressed in the SUPERTHEME project. Although the simulation of the electro-thermo-mechanical effects in integrated circuit is in principle possible by the application of the TCAD simulation systems such as Sentaurus TCAD of Synopsys or software package ANSYS [7], a prohibitive simulation time would needed for a direct simulation of even small integrated circuits. Therefore, **in SUPERTHEME the results of the numerical simulations of electro-thermo-mechanical effects for separate devices were transferred to compact models so that they can be used in evaluation of the variability of the electrical behavior of integrated circuits.**

The SUPERTHEME project addressed the most critical gaps in the simulation of process variations and their impact on devices and circuits. These gaps consisted of four topics which were hardly considered in earlier projects:

- First in the simulation sequence, the link between the sources of variations within the semiconductor fabrication processes and the device and interconnect geometries, and the dopant distributions in the devices. These geometries and dopant distributions after the whole process flow are referred to here as *device defining data.* The systematic variability occurring especially in lithography, deposition and etching processes must be treated together with the statistical variability caused by the granularity of matter and manifesting itself e.g. via dopant fluctuations in doped areas or line edge/line width roughness resulting from photon statistics and molecular structure in photoresist illumination and development.
  Correlations between the various sources of variability must be traced in the simulation, because corner models are in many cases over-pessimistic. This requirement was not met by tools available before the start of the project.

  Within SUPERTHEME, this gap was closed: An integrated simulation sequence was implemented spanning from equipment through process and device simuation to compact model extraction. This software system enables the hierarchical simulation of the

impact of variability, including correlations between device data which are influenced by the same process variation.

- Second in the simulation sequence, process-aware compact models must be made available which take into account the possible correlations between some of the *device defining data.* For example, the frequently used approach to treat transistor gate length and threshold voltage as separate input parameters which vary independently is in many cases wrong, because for short-channel devices the threshold voltage critically depends on gate length.

  Within SUPERTHEME a hierarchical compact model extraction method was developed, implemented and demonstrated, which enables the simultaneous treatment of systematic and stochastic variations. It was presented in various publications and has already found large interest at end-users in industry.

- Third, the interplay of devices, interconnects and other parasitic elements in a circuit must as well be included as the interaction between electrical, thermal and potentially also mechanical effects. The latter influence each other especially for advanced high-voltage but also for aggressively scaled logic devices.

  Within SUPERTHEME this gap was closed by the development and application of required device models eps. for carrier scattering, and by the development of compact and behavioral models.

- Fourth, an appropriate quantification of process variations at their source is mandatory to take real benefit from the software to be developed: With process steps, device architectures and circuits acting as filters and (de)amplifiers of the initial variations, such characterization of the input data is key for industrial application.

  Within SUPERTHEME a broad and exemplary inventory and quantification of process variations was conducted, based on data from literature, equipment manuals, and newly collected experimental characterization data,

The novel advanced capabilities of the software system developed were demonstrated on advanced *More-than-Moore* and *More Moore* benchmarks. The project has fully met the technical objectives defined in its workplan and widely disseminated its results to the scientific community at conferences, workshops, via journal papers and via the SUPERTHEME WWW page. Internal exploitation of project results at partners' site and commercialization of software results via the SUPERTHEME partner GSS have already achieved very good results.

Strategy beyond the project

As pointed out below in the section on the dissemination and exploitation of results, various results from SUPERTHEME are already now being used to support product development at ams and the equipment companies involved in SUPERTHEME. The partners plan to further push these exploitations via internal work and bilateral cooperations, and look for opportunities to further enhance the simulation system for *More than Moore* applications.The software is and will also be applied in third-party funded technology projects. Most important, SUPERTHEME has already strongly enhanced the market position of the software house GSS. Prospects are excellent to keep this development sustainable.

The results obtained in SUPERTHEME have also provided an excellent starting point for further extension of the successfully demonstrated approach of variability simulation to leading-edge More Moore devices and interconnects, which were not in the focus of SUPERTHEME: Within the new project SUPERAID7 ("Stability Under process Variability for Advanced Interconnects and Devices beyond 7 nm Node") funded by the EC from January 2016 to December 2018 within the HORIZON 2020 Programme new and improved simulation modules and models will be developed and integrated which are needed for aggressively scaled interconnects, FinFET and nanowire transistors, and al-

ternative channel materials. In addition the capabilities and methodologies developed during SUPERTHEME have helped project partners in successfully securing additional EC project funding in the shape of the CONNECT and REMINDER projects recently funded under HORIZON 2020. The CONNECT project is utilising simulation and compact modelling methodologies developed during SUPERTHEME and extending them for use in the investigation of Carbon Nanotubes for advanced interconnects from both a technological and modelling perspective. The REMINDER project will also build upon tools and methodologies developer during SUPERTHEME and will expand their capabilities for memory technology modelling, specifically targeting ultra-low power memories for IOT applications.

Description of the main S&T results / foregrounds

The key objective of the SUPERTHEME project was to close these critical gaps, by focusing on the simulation of process variations and their impact on device and circuits, including device reliability. To this end, a hierarchical simulation approach was implemented which allows for the holistic simulation of the impact of process variations from their source (largely at equipment level) through the sequence of process steps needed for device and circuit manufacturing up to the performance and reliability of the device and circuits.

An immanent problem was that equipment-induced variability had hardly been characterized at its source. Although it had e.g. been demonstrated how a change in the focus position ("defocus") in lithography results in changes of the gate length of a transistor, this information is of very limited use if the distribution of the defocus values is not known for the equipment used. Generally, one needs to know the distribution of all relevant equipment parameters which cannot be fixed to a desired value during manufacturing, e.g. due to inaccuracies of equipment settings or due to inhomogeneities across wafers or non-stationary processes. In SUPERTHEME project this problem of missing equipment data was tackled by the involvement of four semiconductor equipment companies which collected representative data on the amount and distribution of equipment-induced variability. The four equipment companies active in SUPERTHEME and the semiconductor company ams extracted related variability data available from literature and equipment documentation available. This data collection was complemented by dedicated work to characterize equipment-induced process variations for one exemplary piece of equipment at each of the four equipment companies. Additionally, own equipment documentation and partly also process statistics recorded at ams have been used. **As one important result of SUPERTHEME the quantification of process variations has been worked out for the process steps lithography, etching, layer deposition, ion implantation, annealing, and oxidation**.

Equipment-induced variability was in SUPERTHEME traced up to device level by a combination of proprietary tools from Fraunhofer IISB for topography simulation and commercial tools (Sentaurus Process) for dopant simulation. A special methodology developed by Fraunhofer IISB has enabled to trace correlations which result e.g. from the use of the same mask level for patterning of different critical dimensions in the circuit. **In turn, the second key result of SUPERTHEME was to enable the simulation of the impact of equipment-induced variations on devices.**

In order to make the new information on the resulting variations of geometries and dopant distributions of the fabricated devices usable for application, variability must be traced at the device and circuit simulation level. To this end in the SUPERTHEME project the proven expertise of GSS and Glasgow University in the device simulation of the impact of statistical variability (dopant fluctuations, line edge roughness) was used. **In turn, the third key result of SUPERTHEME was the integration of Glasgow tools with the variation aware process simulation mentioned above, and thus enables to simulate not only the impact of statistical variations, but also of systematic variations caused by the equipment. In order to link to design as the forth key result of SUPER-**

THEME process and variation-aware compact models were developed which enable the efficient simulation of circuits, including also effects of electro-thermo-mechanical coupling.

The approach described above is generic in the way that it is applicable to all devices which are affected by variability from the fabrication with a top-down technology, which means by patterning and modifying bulk material (including SOI and other thin layers). Within SUPERTHEME, it was especially developed and applied for advanced *More than Moore* devices and systems, in line with the focus of the ICT8 call of FP7 to which SUPERTHEME was submitted. However, also the use for aggressively scaled CMOS devices was demonstrated. In this way SUPERTHEME addressed both advanced *More than Moore* and advance *More Moore*. So in fact **the bridge built by SUPERTHEME started from the equipment side and extended to a large area of applications**. It is obvious that the ambitious goals of the project could only be achieved if – and was only achieved because - best usage was made of the results of prior and current projects as well as of existing software.

In the following some examples of software development and application results obtained within SUPERTHEME are presented.

Coupled equipment and process simulation, incl. process compact models

Within WP 3, among others work has been carried out to couple equipment simulation tools with process simulation on feature scale. This coupling has been mainly applied to modeling of topography steps (lithography, etching, deposition). Whereas for lithography simulation, the treatment of the equipment is an inherent part of the simulator, coupling to external equipment simulation tools is required for the simulation of etching and deposition. For the modeling of plasma implantation and plasma oxidation, equipment simulation using the commercial tool Q-VT has been carried out with the final goal of feeding the output to the feature scale process simulation. The complete workflow for coupling has been established and demonstrated for etching and deposition. For the reactor simulation for plasma oxidation and plasma implantation, the corresponding equipment simulation setups can be considered beyond current state-of-the art: For plasma oxidation, the power supply via microwave sticks requires a sophisticated setup of the reactor model. For plasma implantation, modeling of the reactor with non-constant pressure in the chamber has been successfully realized.

As an example, in the following, the simulation chain from equipment to interconnect simulation is demonstrated for the modeling of etching and deposition processes which are part of the TSV (through-silicon via) benchmark sequence studied within SUPERTHEME. Furthermore, a compact model for lithography simulation extracted from full process simulations is shown.

Etching simulation

TSVs are generally fabricated using the so-called Bosch process. In one cycle of the Bosch process, first a thin chemically inert polymer layer is deposited, followed by ion-enhanced plasma etching. Whereas the polymer protects the sidewall the ions remove the protection at the trench bottom and enable chemical etching there. Many of these cycles are performed to achieve deep trenches and finally TSVs. This sequence of deposition and etching cycles created the scallops which are typical for TSVs.

Using the plasma equipment simulator Q-VT [8], which is based on the plasma process simulator HPEM [9], the neutral and ion fluxes on the wafer surface are found for each deposition and etch step. This way, the variation between the gas flow through the individual valves of the etching reac-

tor and the flux of relevant species is correlated. Using the simulated fluxes, the vertical and lateral deposition and etch rates on feature scale are simulated using the Level Set process simulator at TU Wien. As an example, in **Figure 1** the simulated dependence of the isotropic and vertical rates on the different fluxes is shown for plasma etching in SF_6. The rates are then used in the same simulation environment to generate desired TSV geometries using process compact models which are based on a linear relationship between the fluxes and the rates (see **Figure 1**). During deposition (C_4F_8) and etching (SF_6), neutral species influence the isotropic chemical deposition/etch rate, while the ions are mainly responsible for the deposition/etch rate on flat horizontal surfaces, leaving the sidewalls relatively intact.

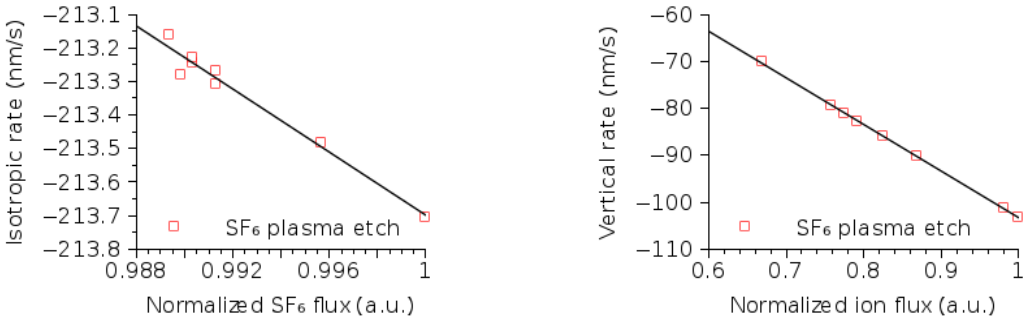


Fig. 1: SF_6 and ion flux influence on the surface rates during etching in an SF_6 plasma.

Deposition simulation

Part of the TSV processing sequence studied is the plasma-enhanced chemical vapor deposition (PECVD) of a SiO_2 layer in a capacitively coupled plasma (CCP) reactor. It is of interest to simulate the profile of the deposited SiO_2 layer in a feature such as a contact hole and to investigate its variation across the wafer. To model the deposition process it is assumed that the adsorbed fragments of the TEOS (tetraethyl orthosilicate) precursor are saturated on the surface and that the process is therefore governed by the local fluxes of oxygen ions and radicals [3]. The equipment modeling of a PECVD reactor containing argon and oxygen has been carried out using the equipment simulator Q-VT [1]. The reactor studied is a CCP reactor with the gas showerhead as one electrode at the top and the wafer carrier platen as the other electrode. This configuration leads to a maximum ion concentration in the approximate middle between the two electrodes. As an example, **Figure 2** shows the simulated reactor along with the concentration of the O_2^+ ions. **Figure 3** shows the fluxes of oxygen radicals and O_2^+ ions at the substrate versus

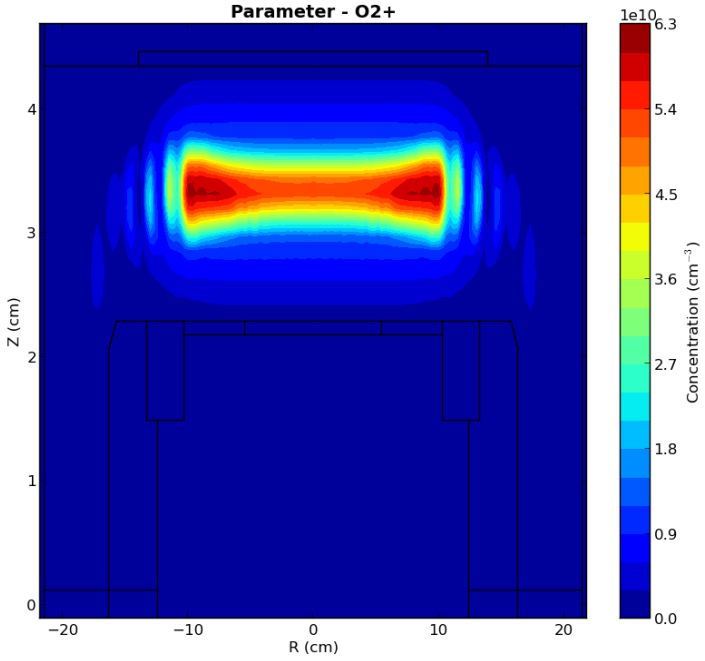


Fig. 2: Equipment simulation result (O_2^+ ions) for a PECVD reactor. The black lines in the figure denote the geometry of the reactor, showing the showerhead electrode at the top and the wafer carrier platen in the middle. For the simulation, a rotationally symmetric geometry has been assumed, a cross section of which is shown in the figure.

the distance from the reactor center axis. These fluxes are provided as a boundary condition for feature-scale modeling.

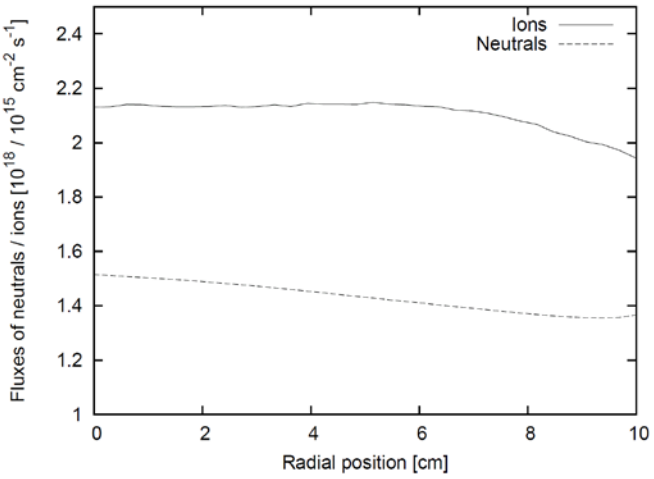


Fig. 3: Fluxes of oxygen neutrals (radicals) and O_2^+ ions at the substrate versus distance from the center axis for the equipment simulation shown in Figure pe.2.

As an example, the simulated profiles of a layer deposited by oxide PECVD in a contact hole are shown in **Figure 4**. For the example studied here, the profile change is due to the change of the growing thickness rather than due to the change of the layer conformality.

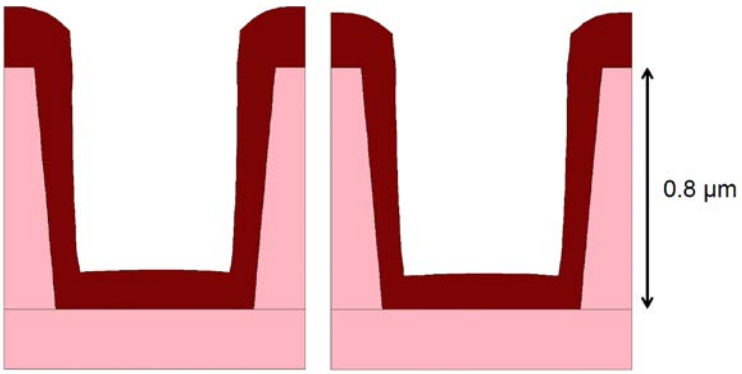


Fig. 4: Simulated profiles (cross sections) of PECVD oxide layers deposited into rotationally symmetric contact holes at different positions on the wafer. The dark red region corresponds to the deposited oxide layer. The left side and the right side show the profiles at the wafer center and at the wafer rim (radial position of 10 cm), respectively. The difference of the growing thickness on top is 10 % with respect to the value for the position at the wafer center.

Compact model for lithography variation simulations

Illumination dose and focus position are two important lithography parameters that are subject to variations. The process window describes the possible variation range of the two parameters for which the resulting feature CDs on the wafer are still inside the specifications. Typically +/- 10% of the nominal CD is allowed. In order to investigate the impact of those variations, a statistical distribution of the illumination dose and focus position inside the process window can be assumed and the resulting CD variations, e.g. serving as input for further electrical simulations, have to be computed. This would typically require thousands of lithography simulations for all the individual dose and focus values. Therefore, a compact model describing the relation between dose, focus and CD can significantly speedup and simplify such investigations. **Figure 5** shows exemplarily one of the response

surfaces of a compact model calibrated for the active and poly layer of a specific 6T SRAM cell layout with nominal feature sizes between 25 nm and 40 nm and a double patterning lithography process.

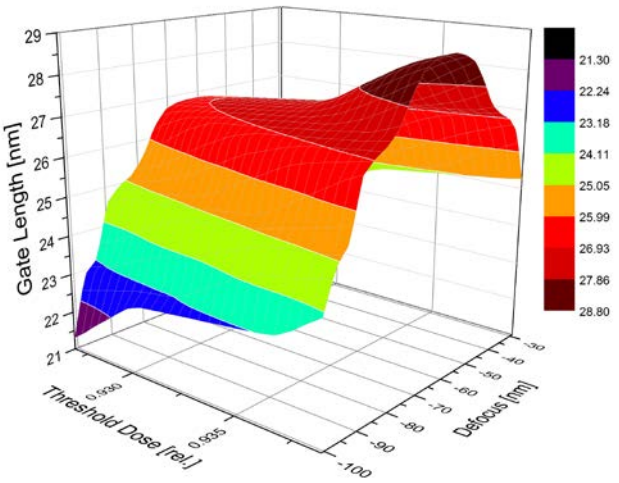


Fig. 5: Response surface of the calibrated compact model.

The gate length of transistor T1 (the SRAM cell consists of 6 transistors with individual gate lengths and widths) depending on dose and defocus is shown in the figure. In the same way the compact model describes the response surfaces for the gate lengths and widths of all the 6 transistors. Using this model the computation time of any individual number is negligibly small. Therefore, the model enables very efficient and fast lithography variation investigations and their coupling with further simulations and process steps.

Improved physical models for variation- aware device simulation

The hierarchy of classical electron transport models, based on the Boltzmann equation, are increasingly challenged in the development of nanoelectronic technologies by the novel phenomena which arise and influence the evolution of the electron system in modern devices and thereby their operation. Furthermore, these phenomena are interdependent and cannot be switched on and off independently without influencing their counterparts, which compose the physical system. This requires a comprehension of the existing physical models and/or the development of novel counterparts and their implementation.

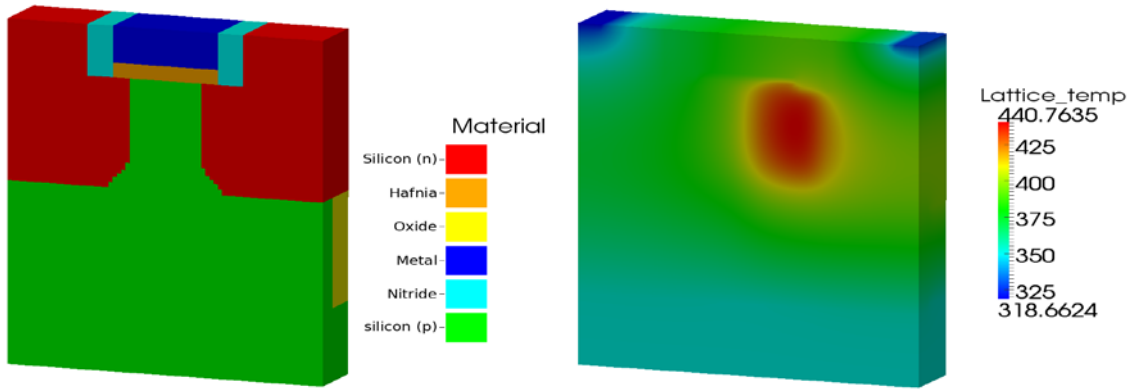
The development of simulation models involves activities to establish the set of relevant phenomena which must be taken into account, to integrate them into a relevant theory presented by a set of equations and to develop algorithms for their solution. Often these models must be refined (improved), which has a twofold meaning: It could be related to improvement of the theory by e.g. adding novel phenomena and, accordingly, novel elements in the equations set and by optimizing the corresponding numerical algorithm. Refinement may also mean appropriate approximations that ensure the numerical feasibility of the implemented computer model. In this case a theoretically superior model is usually refined by certain approximations providing a good balance between physical comprehension and numerical efficiency. Thus, the efforts are devoted to physical analysis and formulation of comprehensive models, which are to be further refined for the needs of GU/GSS and finally industrial application.

Especially important for the behaviour of advanced *More-Than-Moore* and *More Moore* devices are processes of thermal diffusion between active regions and device boundaries, noise due to trapping/scattering from single and multiple dopants and quantum effects due to the existence of nanoscale (confined) domains. These phenomena must be taken into account in the analysis of the systematic variability caused by the process equipment and the statistical variability caused by the granularity of matter. Indeed, the former give rise to non-ideal device geometries and variations in the shape of the interface, which form the boundary conditions for the electro-thermal transport. They determine the distribution of the temperature, which affects all types of electron scattering and, thus, relaxation times and mobilities. Statistical variability caused by the random distribution of dopants depends not only on their position in the channel, but also on the interaction with the electron system comprised of trapping, tunnelling and scattering processes. It is concluded that a relevant device simulator must account not only for the direct sources of process and statistical variability but must simultaneously account for the comprehensive physics of thermal, trapping/scattering and quantum processes. The challenges arise from the large class of physical phenomena which must be taken into account: quantum effects caused by confinement and tunnelling, thermal coupling giving rise to a non-equilibrium lattice environment, noise caused by the discrete charges/traps and variability effects due to real device geometries. Accordingly, the range of utilized approaches varies from well-established classical-macroscopic (Drift-Diffusion (DD)) and microscopic (particle Monte Carlo (MC)) models to quantum models. The numerical issues are related to the conjunction of deterministic and stochastic approaches, the multi-dimensional character of the relevant description and the computational time requirements of the involved statistical simulations. All these peculiarities are addressed in the three categories of models related to: (i) heat transfer; (ii) instabilities and noise caused by discrete charges/traps; (iii) quantum effects in the nanoscale limit.

Electro-thermal transport: A hierarchy of electro-thermal models have been developed and implemented during the project. Initially, a thermal simulation module was developed based on the current state in the field, but simplified to yield numerically efficient models. The modules couples the current continuity equation (CCE) for electrons, a heat flow equation linking the Fourier law with energy conservation law for phonons and the Poisson equation, which ensures the module is self-consistent. Based on these equations, we have developed a thermal simulation module implemented within the framework of the GSS statistical-variability-aware device simulator GARAND. Several steps towards comprehension of the involved physics are realized. The temperature-dependence has been considered in both mobility and the thermal conductivity models.

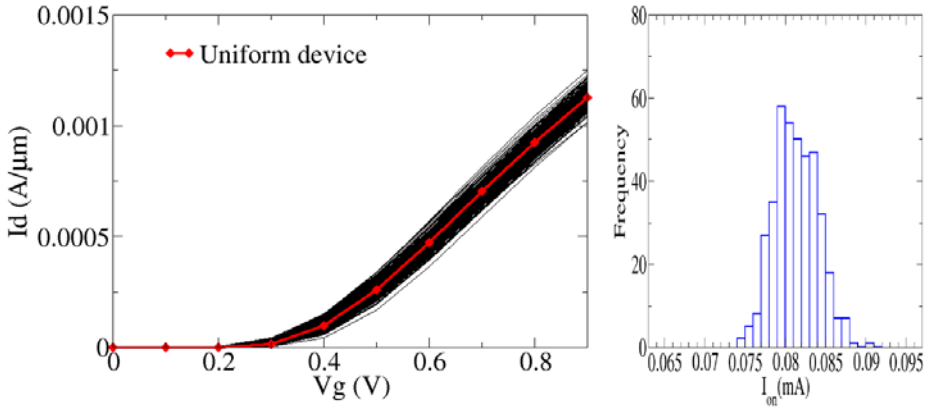
A further refinement is provided by a more relevant physical description of the heat flow process, which accounts for the fact that heat is dissipated in a much larger domain than just the active region of the device. In actual FinFET devices, where the thickness and width of the fin is much less than 100 nm, the thermal conductivity can be significantly reduced when compared to bulk Si, due to phonon-boundary scattering. We employ a new model for the calculation of the fin's thermal conductivity in the fin region, which refines a previous 1D paradigm to 2D confined structures. The suggested formula considers both the fin height and the fin width and depends on both position and temperature. Using this new calculation method, the thermal conductivity is predicted to be 1~2 orders of magnitude lower than the values for bulk Si.

The research on electro-thermal transport culminated in a novel two phonon temperature model, which accounts for the individual temperatures of optical and acoustic phonons. The new heat flow equation was developed by starting with the current-state model in the literature consisting of energy transfer equations involving the temperatures of electrons, acoustic and optical phonons (*Te, Ta* and *To*, respectively) under the assumption of stationary transport; the new heat flow equation extends on this and comprises *Te, Ta,* the electron density, drift velocity and the heat capacity. *Te* can be precalculated by MC simulations and a look-up table of the temperature (as a function of the local field)



(a) Cross section of the nominal device showing materials and structures included in the simulation domain

(b) Lattice temperature distribution (in Kelvin)



(c) Statistical transfer characteristic

(d) Distribution of on-current

Fig. 6: 3D coupled electro-thermal simulation for bulk FinFET

can be constructed. Then, the coupled Poisson, CCE (accounting for the temperature gradient) and energy transfer equations are solved iteratively.

These models have been implemented and demonstrated on some examples of FinFETs. **Figure 6** demonstrates statistical variations in a bulk FinFET example under the combined impact of statistical sources of gate line edge roughness, fin line edge roughness and metal gate granularity. A statistical ensemble of 400 transistors is simulated for both high and low drain voltage conditions. Based on the 3D coupled electro-thermal simulation, we are able to perform comprehensive investigations of self-heating in both SOI and bulk FinFETs with statistical variations, which will be detailed in a later section.

Noise: Random telegraph noise (RTN) and bias temperature instabilities (BTI) are different manifestations of charge trapping in oxide or channel. A reliability-aware CMOS design relies on an understanding of the effects of variability induced by the atomistic nature of dopants. Standard DD approaches only take the electrostatic impact of the charges trapped by the dopants into account. Monte Carlo (MC) simulations correctly take into account also the scattering aspects of the interaction with the charge centers, however they are very slow for stochastic applications with varying positions of individual dopants. High productivity drift-diffusion (DD) simulations are needed, which, however,

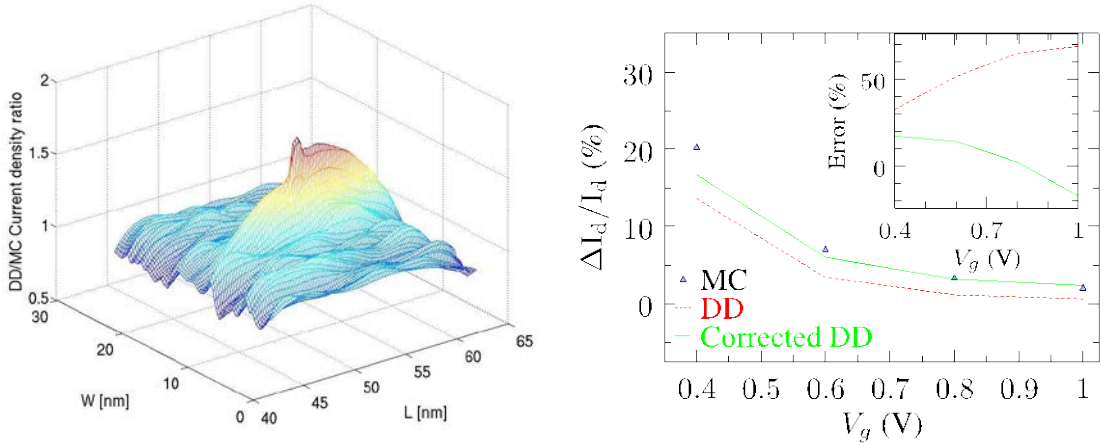


Fig. 7: Left: DD/MC current density ratio at VG = 0.8V on a 2D plane 1nm below the channel/oxide interface for a W, L= 25 nm MOSFET template. Right: Drain Current degradation due to a single trapped charge at the center of the channel as a function of Vg. Simulations with DD, MC and corrected-DD are reported. The relative error between DD and MC and between corrected-DD and MC are shown in the inset.

rely on effective mobility and saturation velocity models correctly accounting for the scattering aspects of the interaction. By comparing DD and MC results, we pursue a methodology to derive a 'quasi-local' mobility model that accounts for the scattering effects associated to single trapped charges in DD simulations. In DD simulations the current flow surrounds the defect – the influence of the trapped charge is very local and confined. Instead, in MC simulations the current flow is split in two main streams and the influence of the trapped charge is non-local and extends toward the drain region. Indeed, the ratio between the DD/MC current densities on a 2D plane, 1nm below the channel/oxide interface (shown in **Figure 7**), is practically unity (1) over the entire channel far from the defect position (note that the fluctuations are due to the stochastic nature of the MC simulation). Immediately before the defect position, the DD simulation overestimates the current value. This is even more pronounced after the defect position, with the DD simulation overestimating the current by a factor close to 2 for more than 10 nm after the trapped charge in the middle of the channel.

An empirical mobility model has been developed, based on a mobility correction factor which takes into account the DD/MC velocity ratio and extends to 3D case by means of triangular functions. A comparative study of device MC and DD simulations, using the implemented empirical model, has been performed. It is shown that the DD approach maintains computational efficiency and accuracy at low drain biases, (Vd=0.05V), as shown in **Figure 7**. The relative error in underestimating the scattering effects increases from 30% to 70% with an increasing gate bias from 0.4 V to 1.0 V. At high biases more complex corrections, which go beyond the empirical mobility modification, are necessary. A mobility correction for multi-dopant induced mobility reduction in the source and drain regions has also been developed, by considering that these dopants act as attractive centres and trap charges, which reduce the mobility in the extensions in atomistic simulations.

Quantum transport: Advanced devices, such as FinFETs and nanowire transistors, are characterized by active regions that consist of spatially confined domains. The Bloch electron – the basis for the Boltzmann picture – with well-defined momentum components and a continuous energy spectrum ceases to correctly describe the electron state in such strongly confined domains. Accordingly, the Boltzmann transport model and all macroscopic models derived from it, like the drift-diffusion and hydrodynamic equations, used for simulation of classical devices must be revised. Novel phenomena arise as a result of the confinement, such as quantization of the energy spectrum (multi-subbands)

and a lack of a well-defined momentum. The latter is a direct consequence of the uncertainty relations: the electron is spatially localized in the direction of confinement, so that the corresponding momentum component cannot be exactly determined. This is of special concern for electron scattering models, since the fundamental property of momentum conservation is lost in the confined directions. A major result is the systematic derivation of multi-subband scattering models where the theoretical aspects reflect the physical features of the GU/GSS simulation tools. Models of multi-subband scattering for acoustic phonons, deformation potential optical phonons, surface roughness and polar optical phonons have been derived. They can account for anisotropic non-parabolic multivalley band structures characteristic for Si and Ge. **Figure 8** shows the total acoustic out-scattering rate from the first sub-band to the first ten sub-bands of a 3 nm round wire. The phonon models have been used to calculate the electron mobility with the help of the Kubo-Greenwood formula. The formula is obtained within a linear response theory, assuming small displacements from equilibrium and expresses the mobility via the momentum relaxation rate.

Under certain simplifying assumptions the latter may be expressed explicitly via the total out-scattering scattering rates. **Figure 8** presents the Kubo-Greenwood mobilities calculated for acoustic and optical *f*- and *g*-type scattering, in a square gate-all-around quantum wire for 10 sub-bands as a function of the wire width and orientation. Monte Carlo results of *Ramayaya et al, J. of Appl. Phys. 104, 063711 (2008))* for similar conditions (SOI square wire, in the presence of phonon and surface roughness scattering) are in a good agreement, which may be regarded as a validation for the developed approach and its implementation. The mobility approaches bulk values for wires with widths above 10 nm.

Processes of electro-thermal transport, scattering caused by discrete charges and quantum effects of the scattering mechanisms determine the operation of aggressively scaled devices and thus their response to sources of variability. **Models of such processes, derived within SUPERTHEME provide the relevant physical environment for simulation of the systematic and statistical variability and thus significantly advance the state of art in the field.** A hierarchy of electro-thermal models has been developed to predict the distribution of the electron and lattice temperatures, which affects all types of electron scattering and, thus, relaxation times and mobilities. Unique mobility models have been obtained to account for scattering from single and multiple

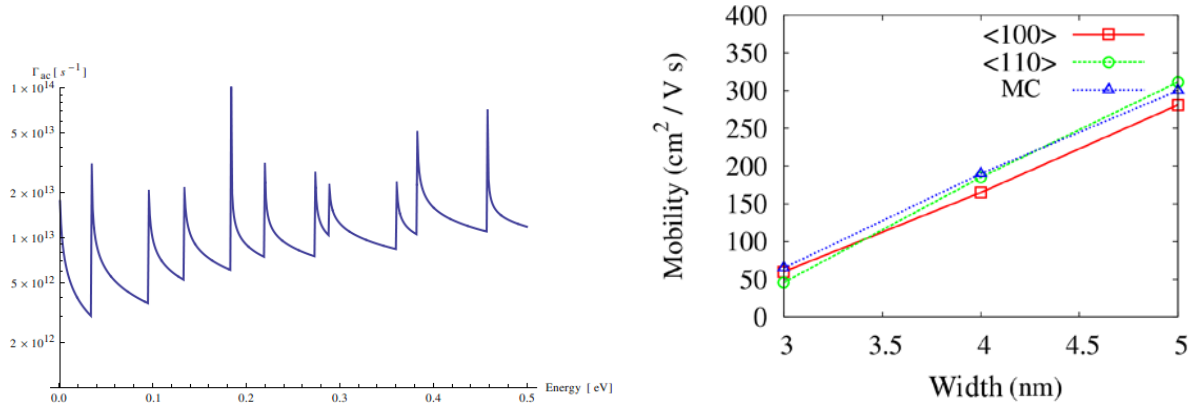


Fig. 8: Left: Total acoustic phonon out-scattering rate for 1_to_ X sub-bands in the case of the elastic, parabolic equipartition approximation. Peaks correspond to the energies of the X=1,2,.10 sub-bands. Right: Kubo-Greenwood mobilities of a gate-all-around square wire for two different orientations. Monte Carlo results calculated for a SOI square wire are given for a qualitative comparison.

discrete charges, allowing for computationally efficient noise simulations. The derived models accounting for the quantum confinement on a variety of scattering mechanisms allow not only to improve the GU/GSS simulation engines, but also provide tools for a deep analysis of the operation of confined devices to the semiconductor community.

Software integration and extension

Prior to SUPERTHEME project, there were missing links between the simulation of statistical variability and the systematic variability which occurs at the equipment and process level. Consequently, it was impossible to do full simulation flow from process level to device level to circuit level and investigate the impact of variability sources at all levels including their correlations.

In order to enable the simultaneous simulation of systematic and stochastic variations, we have worked on the integration of the lithography/topography simulation tools of Fraunhofer IISB and other commercial TCAD tools with the statistical-variability-aware device simulator GARAND of GSS. We have developed a structure translation tool, MONOLITH, which allows device structures to be transferred via a common transfer file format. Considerable attention has been paid to the transfer of simulation geometries between the different meshes used in the different simulators. The 3D 'atomistic' TCAD device simulator GARAND uses finite difference simulation meshes, in order to implement seamlessly the different statistical variability sources and to ensure simulation efficiency and small memory footprint and to allow Monte Carlo transport simulations in the same simulation domain avoiding intolerable self forces associated with finite element discretisation. The lithography, deposition and etching simulators Dr.LiTHO, DEP3D and ANETCH, developed by Fraunhofer IISB, and the commercial process simulation tool SENTAURUS Process are based upon various kinds of meshes. It has been necessary to develop a set of tools and interfaces to facilitate their interoperation. The tool MONOLITH developed in SUPERTHEME is capable of interpreting input device structures in a commonly supported file format (DF-ISE) and resampling and interpolating material, doping and electrical parameters from finite element to finite difference simulation meshes (**Figure 9**).

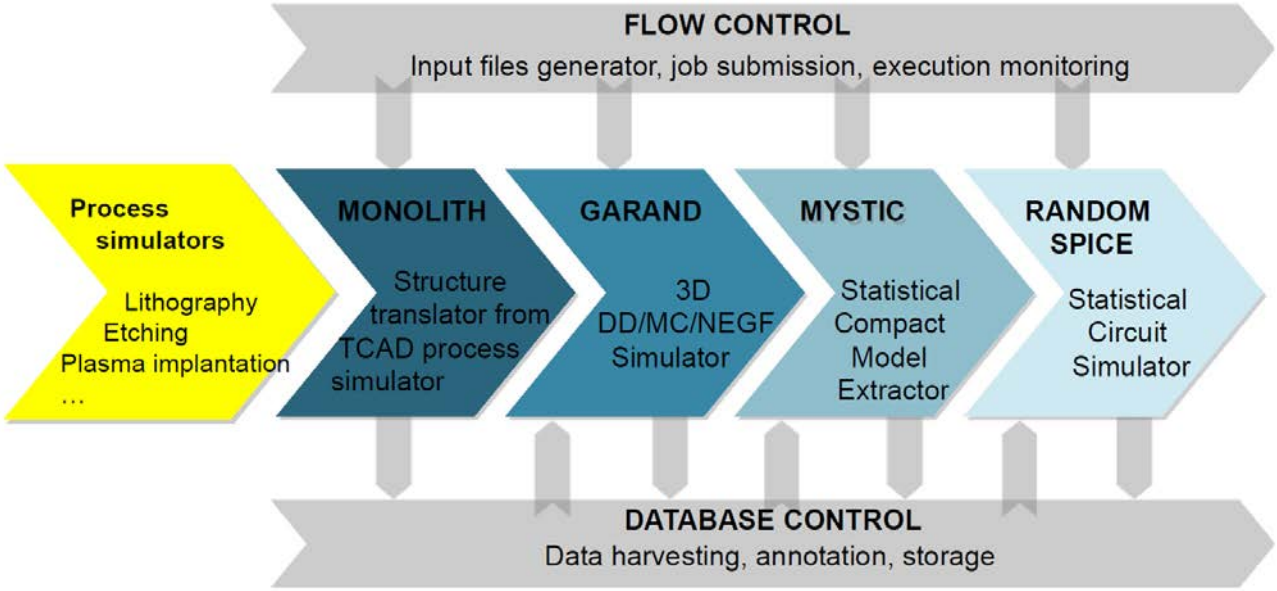


Fig. 9: Schematic description of GSS tool chain.

An optimised import process has been worked out for the DF-ISE structures produced by Sentaurus and the Fraunhofer tools. Our developed tools can convert tetrahedral finite element tensor meshes produced by commercial tools such as Sentaurus to the hexahedral finite difference meshes required

by the GSS Garand simulations tools. By using Sentaurus' *snmesh* tool to perform the re-meshing required to produce a tensor mesh either prior to, or post, implantation and annealing simulation, and directly transferring this simulation mesh to Garand, any errors due to inconsistencies in mesh or interpolation are almost completely eliminated. This process is illustrated schematically in **Figure 10**.

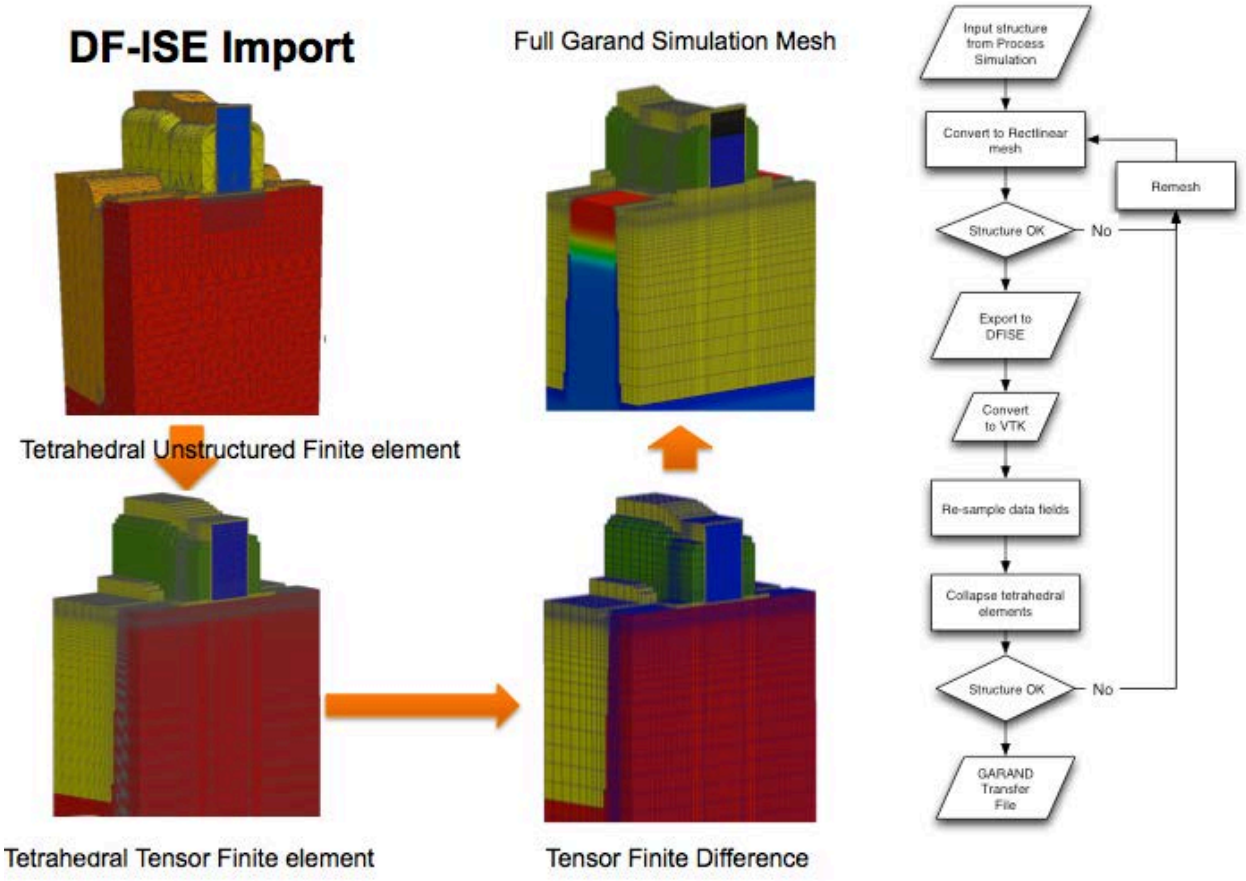
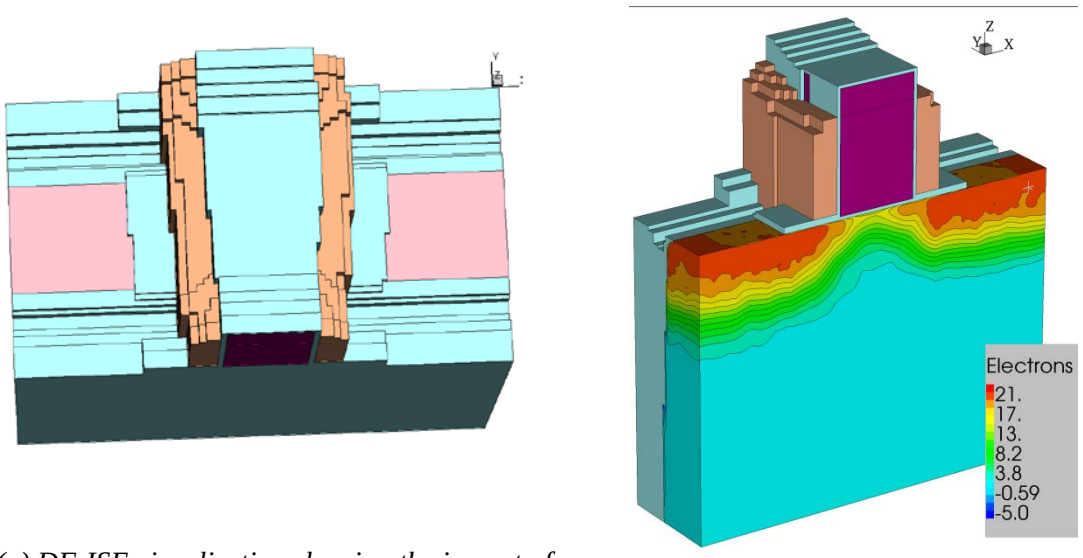


Fig. 10: Schematic description of the process of mesh conversion from Sentaurus process to Garand.

To facilitate the tighter integration between commercial tools such as Synopsys we have developed a set of utilities, for conversion of exported finite element DF-ISE mesh to VTK with material and data re-sampling, for conversion of tetrahedral elements to hexahedral, and for conversion of Garand VTK output to DF-ISE. Due to the complex nature of the workflows employed in commercial TCAD operations it is necessary to adopt standardised procedures for the creation and running of simulations. The de-facto standard in the semiconductor industry is to use the Sentaurus workbench (SWB) software from Synopsys for workflow management. DFISE output capabilities that have been added provide best fit within the current industry standard practices. We have introduced other features to the Garand tool chain to aid integration with SWB, to allow users of SWB to make full use of the GSS data management framework from within SWB. The developed specific tool allows the user to interact with the GSS Data Management system via a configurable module in SWB. The GSS tool chain heavily uses the open source VTK file format for data transfer and particularly for visualisation of simulation results. However, the standard visualisation tool that is used by SWB is a proprietary piece of software called "Sentaurus Visual" (SV) with very limited file format support. The export of Garand simulation data in a supported form provides the essential tool for the many users who utilise SV along with the native scripting capabilities of SWB for simulation analysis as well as visualisation (**Figure 11**).



(a) DF-ISE visualisation showing the impact of LER

(b) Electron concentration from Garand variability simulation

Fig. 11: A demonstration of Garand variability simulation visualised using Sentaurus Visual

The integrated simulation is demonstrated on a bulk silicon MOSFET designed to meet the requirements of the 20nm CMOS technology generation, and based on a set of data covering a 5x5 experiment design obtained from simulation of variability introduced by double-patterning lithography of a test SRAM cell circuit at Fraunhofer IISB, see Figure 12. For the simulation of the patterning processes the Fraunhofer tool Dr.LiTHO was used. Other process simulations of the example 20 nm bulk planar CMOS transistors are carried out using Sentaurus process, and then converted and transferred to GSS device simulator Garand. The transistors have a 23.5nm physical gate length and 33 nm channel width. The realistic transistor structure includes shallow trench isolation (STI), incorporated into the simulation domain, which is critical in order to accurately capture narrow width effects. Simulations of NMOS and PMOS transistors are benchmarked against industrial 20 nm bulk CMOS MOSFET technology. A total of 25 transistors with different dimensions are simulated to cover the design-of-experiments (DoE) space. Based on each uniform transistor in the DoE space, 1000 “atomistic” microscopically different transistors are simulated using GARAND. The dominant statistical variability sources including Random Discrete Dopants (RDD), Line Edge Roughness (LER), and Metal Gate Granularity (MGG) are simulated in combination. From the simulated IV characteristics, the figures of merit including on-current (I_{on}), threshold voltage (V_{th}), the subthreshold slope (SS) and the off-current (I_{off}) are extracted and their statistical distributions are investigated.

The software integration and the extension of GARAND capability to simulate the generic structures coming from process simulations have become the essential base for variability-aware compact modelling to capture both systematic and stochastic variations, and correlation-aware circuit simulations. The work on streamlined structure transfer, simplified workflow interface and flexible data management, has further lead to the development of Enigma - the GSS workflow, automation and productivity framework - which is designed to deliver a powerful and flexible environment for rapid design-technology co-optimisation (DTCO). Dur-

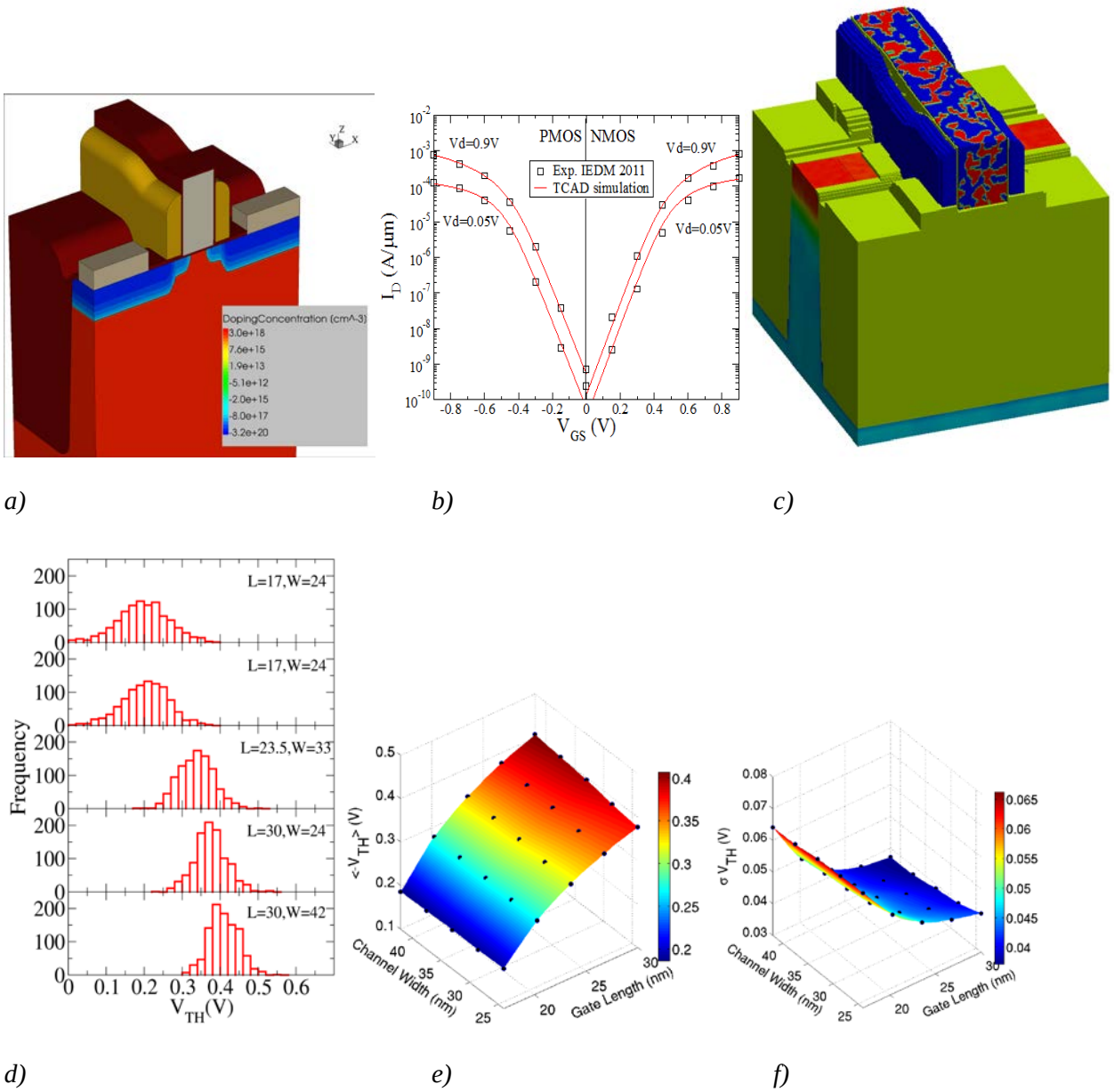


Fig. 12: Integrated simulations on a bulk silicon MOSFET. (a) An examples of the geometrical shape and the doping distributions in p-channel MOSFET devices simulated at Fraunhofer IISB using Dr.LiTHO and Sentaurus TCAD; (b) The uniform simulation of nominal n/p MOS transistors benchmarked to the 22 nm bulk CMOS experimental data, using GARAND; (c) The atomistic simulations of the n-channel bulk MOSFETs, which includes random dopants, gate line edge roughness, and metal gate granularity; (d) the threshold voltage distributions at four corners of DoE and nominal design for NMOS; (e) and (f) The average and standard deviation of the threshold voltage over (L, W) for PMOS.

ing SUPERTHEME, the statistical-variability-aware device simulator GARAND has also been enhanced in other respects, including the capability of electro-thermal simulation, the mobility correction related to trapped charges, and quantum confinement, which will be described in other parts of the document.

Hierarchical compact modelling

Based on the assessment of the sources and types of variation and their potential correlations, in SUPERTHEME a methodology to extract process and correlation-aware compact models was developed as follows:

- The statistical device simulator GARAND has been extended to enable the treatment of general non-planar device geometries.
- The GSS compact model extraction tool Mystic is integrated in the GSS tool chain and links to GARAND through a database that contains the results of statistical device simulations carried out with GARAND.
- This database is filled with results of GARAND simulations of both the nominal and variation-affected devices.
- Using this extended version of GARAND, Mystic can be used to extract parameters for relevant compact models, especially BSIM4.

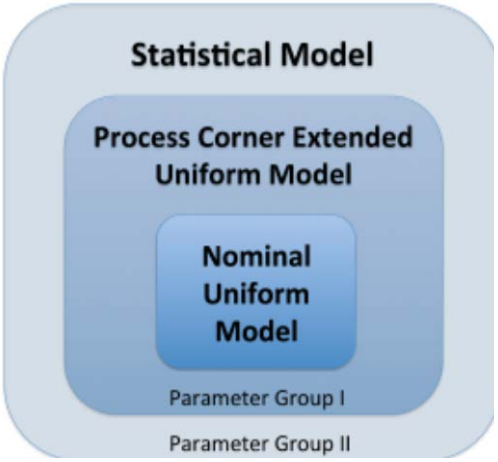


Fig. 13: Schematic view of unified compact modelling strategy. It features nominal uniform model and two groups of parameters, and enhanced statistical models.

Two distinct groups of parameters are used to capture the effects of process and statistical variations respectively, and a unified compact modeling strategy is applied:

- Firstly, a comprehensive compact model is extracted for nominal design device. This is the first and inner step in the sequence illustrated in **Figure 13**.
- Secondly, the extraction strategy is employed for devices which result from fabrication steps with different variations. A simple example, discussed below, assumes that due to variations in the fabrication sequence channel length L and width W vary in some way. These variations are studied by process simulation. Using GARAND and MYSTIC, the dependency of a first set of compact model parameters on L and W is extracted. This leads to the extraction of the so-called “Group 1” parameters.
- Then, the extraction strategy is employed for devices which are subject to statistical variations, such as Random Dopant Fluctuations RDF. This dependency is expressed by the so-called “Group 2” parameters shown in **Figure 13.**

Based on this compact model extraction strategy the statistical GSS circuit simulation engine RandomSpice [11] can generate correlated process-aware and statistical compact models using GSS proprietary statistical compact model generation technology.

The compact models extracted in this way are process-aware and correlation-aware:

- Variations of selected process results are included, such as gate length and width in the example discussed below.
- Correlations are included insofar as different equipment variations (e.g. of lithography focus and dose) and statistical variations partly influence different electrical properties (e.g. I_{on}, V_{th}) in parallel. These correlations must be and are included in the compact models extracted. A good example is that focus variations in optical lithography may affect the channel length of some transistor in an SRAM cell, while not influencing the channel length of other transistors in the same cell [12].

A first example for the impact of correlations was presented at SISPAD 2013 [12]. Here, an SRAM circuit consisting of bulk transistors with nominal gate lengths and widths of 20 nm for the inner flip-flop and 25 nm for the access transistors was considered. Due to limitations of optical lithography

such small features must be fabricated with Double Patterning. For the example studied we assumed the Litho-Etch-Litho-Etch (LELE) variant of Double Patterning. Unlike usual lithography, which uses a single mask, Double Patterning splits a critical mask level into two incremental masks, which are exposed separately in two incremental lithography steps. **Figure 14** shows the SRAM cell after simulation of double patterning for fixed values of dose and focus. The black features are the active silicon areas, the dark gray features are the polysilicon areas generated with the first lithography step of the Double Patterning process and the light gray features are the polysilicon areas generated with the second lithography step of the double patterning process. Due to periodic boundary conditions four 6T SRAM cells have to be simulated. T1 / T2 / T3 / T4 are the flip-flop transistors, T5 / T6 are the access transistors. Due to the two lithography steps of the double patterning process the focus / threshold variations inside the two groups T3 / T4 / T5 and T6 / T2 / T1 are the same but between the two groups the variations are independent from each other.

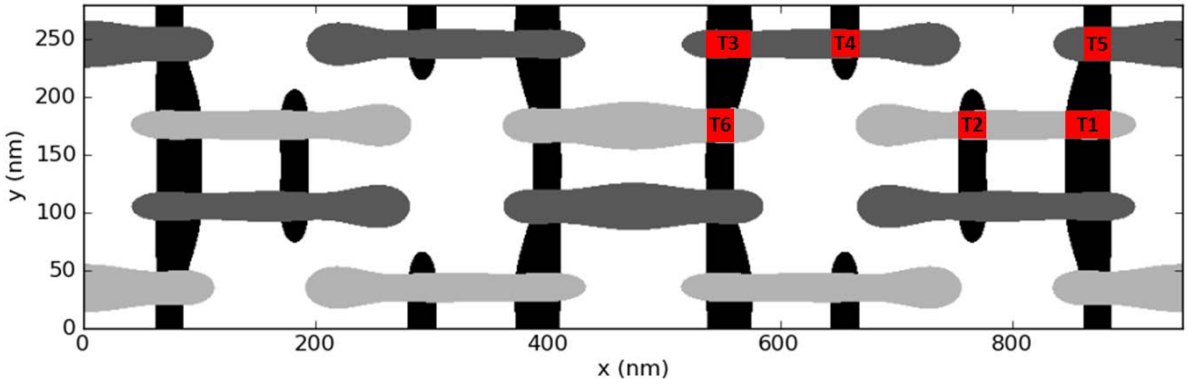


Fig. 14: Final result of the lithography simulation of the 6T SRAM cell exemplarily for one focus / threshold position. The black features are the active silicon areas, the dark gray features are the polysilicon areas generated with the first lithography step of the double patterning process and the light gray features are the polysilicon areas generated with the second lithography step of the double patterning process [12].

Assuming Gaussian distributions for the variations of focus and dose threshold in both incremental lithography steps the gate length distributions of the six transistors have two distinct properties: First, they are different from each other, both due to the two incremental lithography steps used and due to their different positions in the cell layout which due to the proximity effect influence the feature sizes printed in the lithography process. Second and especially important, due to the division of the cell layout into two incremental steps for the patterning of the gate structures, within each of the two transistor triples (T1, T2, T6) and (T3, T4, T5) the variations of the gate lengths correlate, but gate length variations do not correlate between the two triples. Besides this, the layout used also leads to different channel width variations for the six transistors although the channel width is defined by a single exposure lithography step.

In order to study the effect of these correlations on the SRAM cell we first set the defocus and the intensity threshold to their minimum and maximum values and observed the resulting change of the SRAM performance parameters [12]. **Figure 15** shows the results of such sensitivity analysis for two variants of correlated variations. In the first variant shown in **Figure 15** (left), defocus and intensity threshold were set simultaneously in all lithography levels to their minimum and then to their maximum values. In **Figure 15** (right), defocus and intensity threshold were set in anti-phase in the two lithography levels for polysilicon structuring, i. e. in Var F1 defocus was at its minimum in the first illumination but at its maximum in the second illumination; in Var F2 defocus was at its maximum in the first illumination but at its minimum in the second illumination; in Var D1 the intensity threshold

was at its minimum in the first illumination but at its maximum in the second illumination; and in Var D2 the intensity threshold was at its maximum in the first illumination but at its minimum in the second illumination. The results of such sensitivity analysis are shown in **Figure 15**. If defocus is set synchronously to its minimum a lower Read static noise margin than in nominal setting is obtained. On the other hand, if defocus in Var F1 was at its minimum in the first illumination but at its maximum in the second illumination, we have very little difference in Read SNM in comparison to the optimum setting of defocus and intensity threshold in the middle of the process window (Nominal). In contrast, in Var F2, when defocus was at its maximum in the first illumination but at its minimum in the second illumination the value of the Read SNM has a value much lower than nominal SNM or SNM in Var F1. A synchronous variation of the intensity threshold leads to moderate change of Read SNM, while Var D1 variation results in an SNM significantly higher than the nominal and Var D2 leads to SNM significantly lower than the nominal. These correlations are further discussed in the literature [12].

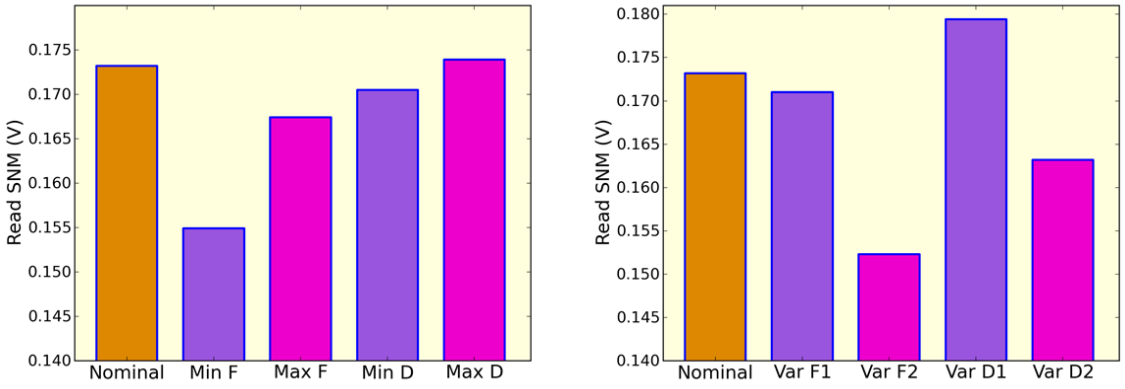


Fig. 15: Read Static Noise Margin variations of the SRAM circuit from minimum/maximum sensitivity analysis [S2].

The combination of this approach with statistical device simulation employing GARAND and statistical circuit simulation using RandomSpice allows for the study of the combined impacts of systematic process variations caused by the equipment used, stochastic variations caused by the granularity of matter, and correlations which occur because different device features (e.g. the channel length of one group of transistors and the channel width of another group of transistors) **are subject to the same process variations**. In the example shown here, Gaussian distributions of focus and illumination dose threshold were considered independently for the two incremental illumination steps in Litho-Freeze-Litho-Etch Double Patterning Lithography, see **Figure 16**. This leads to correlations of the channel length within each of the two transistor triples (T1, T2, T6) and (T3, T4, T5), but no correlations between transistors which do not belong to the same triple. Beyond this, the channel length distributions for each transistor are also influenced by its neighborhood, due to proximity effects in optical lithography. Figure 17 shows the channel length distributions of transistors T1 and T3

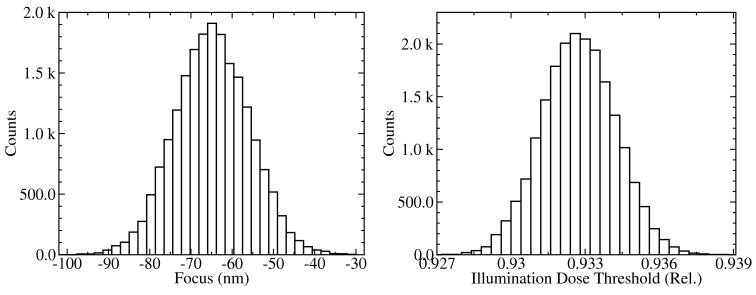


Fig. 16: Assumed probability distributions of the focus and threshold variations used in simulation of lithography steps

which belong to different triples. **Figure 18** shows the IV characteristics and the threshold voltage distributions of two NMOS transistors with fixed different values of transistor channel length and width, subject to the statistical variations Random Dopant Fluctuations (RDF), Line Edge Roughness (LER), and Metal Gate Granularity (MGG). Finally, process-aware compact models were extracted and used in RandomSpice for circuit simulation. **Figure 19** shows the Static Noise (Read) Margin SNM of the SRAM cell from **Figure 14** subject to these lithography and stochastic variations, including correlations in transistor CDs caused by the lithography steps used. The process variations lead to a highly non-Gaussian shape of the SNM distribution.

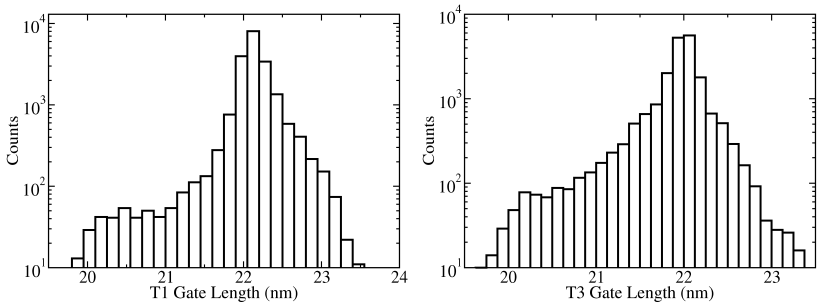


Fig. 17: Probability distribution of lengths of transistor T1 and T3, generated with 2nd and 1st incremental lithography process step in double patterning, respectively. Non- Gaussian shape caused by non-linearities of the lithography process.

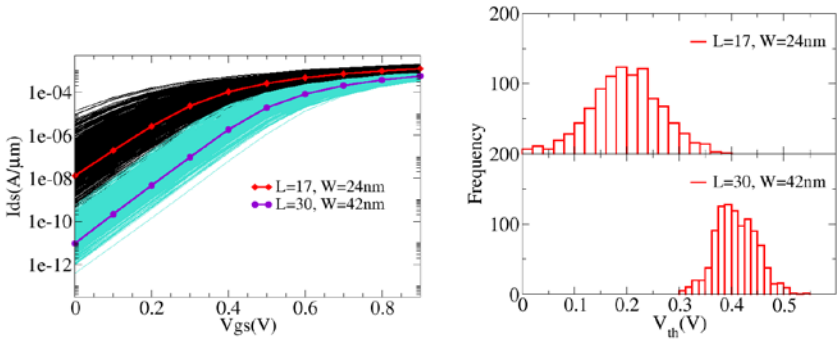


Fig. 18: IV-characteristics and PDF of threshold voltage of 2 NMOS transistors due to variation of L and W resulting from lithography step and statistical variability (RDF, LER and MGG).

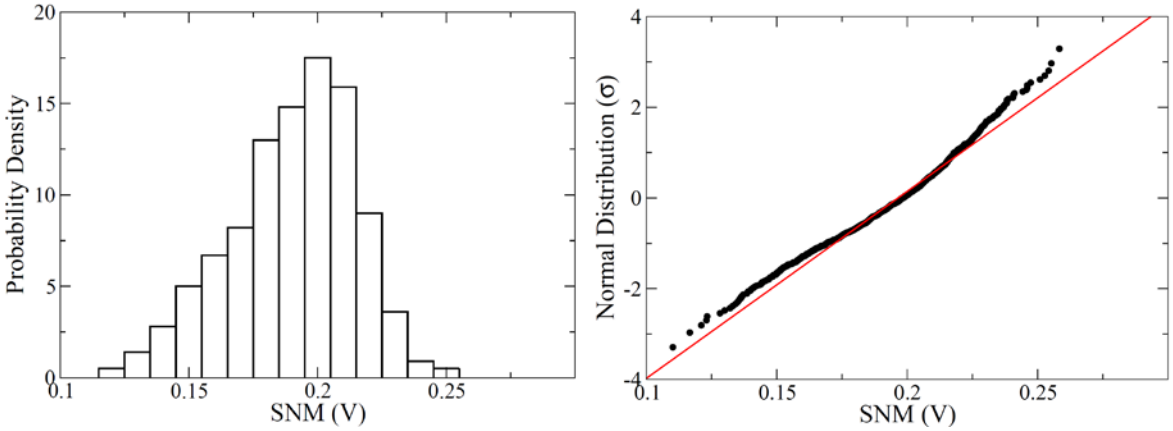


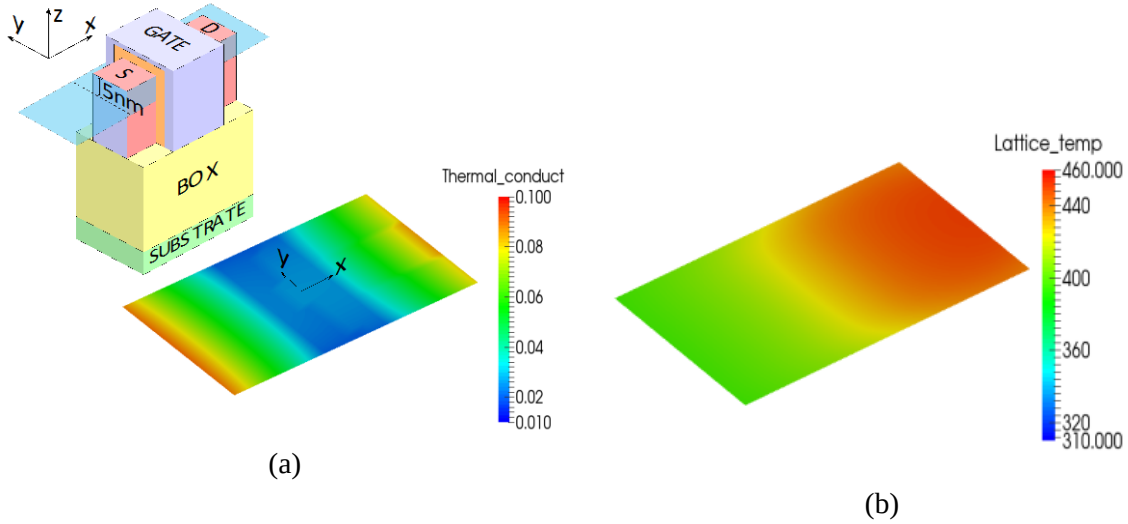
Fig. 19: Histogram and QQ plot for Static Noise Margin of SRAM Cell subject to focus and dose variations in the three incremental lithography steps, together with RDD, LER and MGG. Correlations of electrical transistor parameters resulting from some transistors being patterned with the same lithography step are included.

Electro-thermal simulations

With the continuous scaling of semiconductor devices into the nanometer regime, the thermal density inside transistors is increasing and self-heating effects have become a crucial issue. Now that the traditional planar MOSFET is approaching the end of its useful life, novel architectures such as FinFETs, have been introduced in order to enable technology scaling at the 22nm CMOS technology generation and beyond. The introduction of CMOS FinFETs represents a radical shift in the semiconductor industry. The 3D FinFET architecture excels in the control of short-channel effects and delivers superior scalability, however the FinFETs' thermal properties are significantly degraded and thermal reliability imposes greater challenges. Self-heating effects will be exacerbated in SOI FinFETs due to the low thermal conductivity of the buried oxide layer below the fin. To maximize the benefits of FinFET technology, an enhancement of TCAD tools is required to allow accurate analysis and modelling of self-heating in FinFETs and its influence on device performance.

Within the framework of the GSS statistical-variability-aware device simulator GARAND, we have developed an efficient thermal simulation module to investigate the impact of self-heating on FinFET DC operation and on the corresponding statistical variability. The coupled system of equations describing the heat generation and flow, potential distribution and current density is solved self-consistently.

Furthermore, since the fin thickness (width) is of the order of 10 nm, the thermal conductivity can be significantly reduced compared to bulk Si due to phonon-boundary scattering. We employ a new approximate formula for the calculation of the thermal conductivity in the fin region, which extends the previous 1D formula to 2D, as stated in an earlier section. Using this new calculation method, the thermal conductivity of the fin is predicted to be 1~2 orders of magnitude lower than the conventional value of the thermal conductivity for bulk Si. In our electro-thermal simulation module, the thermal conductivity at each mesh point in the fin is refreshed according to its spatial position and temperature at each iteration cycle, which ensures the self-consistency of the simulation. By using this formula, the thermal conductivity and lattice temperature in a slice of the fin, which is 5 nm below the top gate in the SOI FinFET example, resulting from the self-consistent simulations are obtained and illustrated in **Figure 20** as an example.



(a) (b)

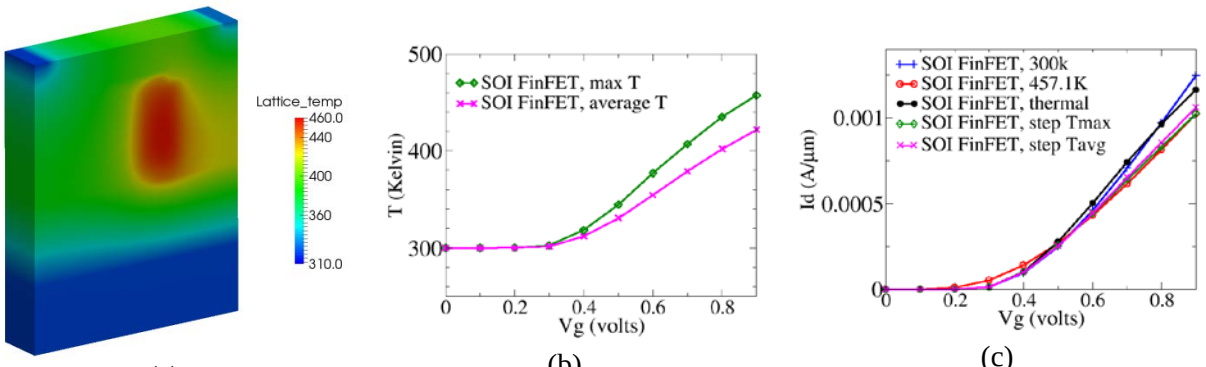
Fig. 20: (a) Thermal conductivity and (b) lattice temperature in a slice of the fin which is 5nm below the top gate in an SOI FinFET example, at Vg=Vd=0.9V, finally obtained from the self-consistent simulation. Inset: schematic showing the cut plane.

Usually the electrical characteristics of the device are calculated in a restricted device simulation domain in order to maximize computational efficiency. However, heat is dissipated in a much larger domain, including the active region of the transistor, its neighbours, the substrate, the interconnect layers, the case, and eventually the heat sink. Therefore, realistic thermal boundary conditions rely on thermal resistances, employed to account for heat dissipation into interconnects, the wafer, the case, etc. By the extended capability of GARAND, external thermal resistances can be included, which is crucial for thermal simulations.

In electro-thermal simulation by GARAND, different mobility models can be used, for example, the Masetti model for doping-dependent low-field mobility, enhanced Lombardi model for perpendicular field dependent mobility and Caughey-Thomas model for lateral field-dependent mobility. We have included the temperature dependency both in the mobility models and saturation velocity.

Overall, GARAND has been integrated and enhanced with this module, enabling to run electro-thermal simulations as a stand-alone tool. Additional commands have been developed for GARAND to activate the capability and specify relevant parameters.

In the SUPERTHEME project, we demonstrate the 3D coupled electro-thermal simulation for both SOI and bulk FinFET. For comparison, simulations without self-heating are performed with geometrically uniform lattice temperature in the device region. Various temperatures were chosen for these simulations: uniform room temperature, the maximum temperature observed within the device during the electro-thermal simulations, a constant temperature defined by the maximum temperature ("step Tmax") and the average temperature in the fin ("step Tavg") at each individual Vd and Vg bias condition, obtained from the electro-thermal simulations. The results show a significant hot spot generated near the drain because of the much lower thermal conductivity of the fin. The coupled electro-thermal simulation clearly shows that the device drive-current is not only affected by the peak lattice temperature, but also by its gradient. The simulations performed assuming a uniform maximum lattice temperature, without solving the Heat Flow Equation, will overestimate the reduction of the on-current. (**Figure 21**)



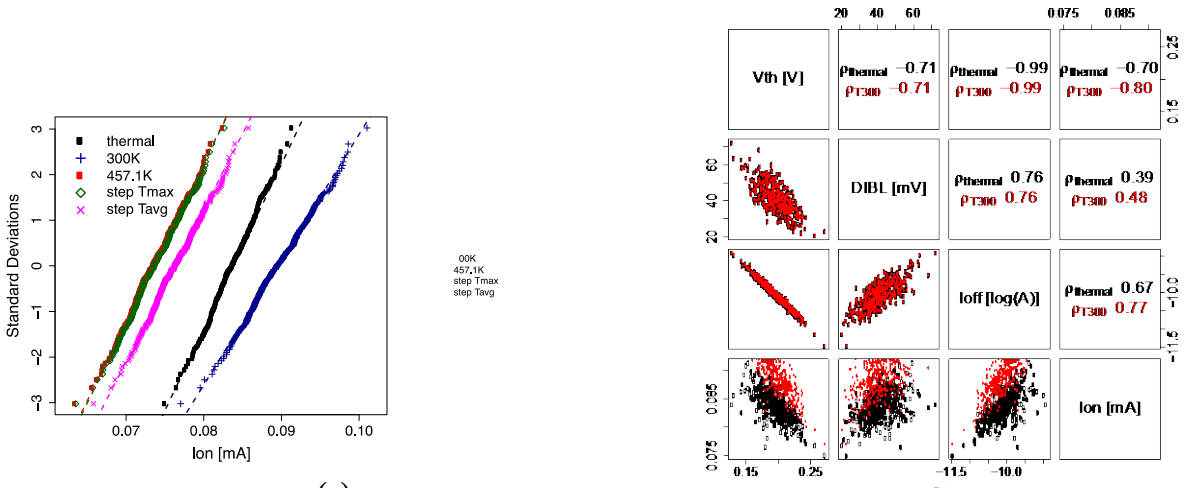
(a) (b) (c)

Fig. 21.: Simulation results for the SOI FinFET. (a) Lattice temperature profile in the middle at Vg=Vd=0.9V; (b) maximum temperature and average temperature in the fin at high drain voltage; (c) simulated Id-Vg characteristics at high drain voltage.

Moreover, using GARAND integrated with the electro-thermal simulation module, we have done more comprehensive investigations on self-heating in both SOI and bulk FinFETs with statistical variations. We have conducted comprehensive analysis on the figures of merit extracted from the statistical simulations. The self-heating has little impact on the figures of merit related to the sub-threshold region in the case of DC operation, however, it affects the distribution of the on-current

(I_{on}) (**Figure 22**). Our electro-thermal simulations indicate an interesting effect in that the self-heating significantly reduces the I_{on} variability. The effect is more pronounced in the SOI FinFET where the self-heating is stronger. The explanation of this effect is related to a negative feedback associated with the statistical distribution of I_{on}. Devices from the higher-current part of the statistical distribution suffer more from the self-heating and their current is more reduced compared to the devices from the lower end of the statistical distribution. Correspondingly, the self-heating strongly affects the correlation between I_{on} and all other figures of merit. These correlations will provide useful information for compact modelling. In conclusion, the temperature variations in the channel need to be included to consider the full picture of self-heating effects, as a uniform increase of the temperature in the whole device region cannot accurately reflect the trends in the variation of on-current.

Our work on electro-thermal simulations has generated publications in SISPAD 2014, ICSICT 2014, IEEE Transactions on Electron Devices 2015, IWCE 2015, SISPAD 2015, EUROSOI-ULIS 2016.



(a) (b)

Fig 22: Simulation results for the SOI FinFET. (a) Comparison of the statistical distribution of on-current for the SOI FinFET obtained from the electro-thermal simulations with uniform temperature simulation results without self-heating. Insets: Threshold voltage and sub-threshold slope. All at high drain bias. Impact of self-heating on the statistical distribution of the on-current is clearly shown, especially the reduction of the I_{on} variability. (b) Correlation between the figures of merit in the electro-thermal statistical simulation (in black), comparing to the results with uniform lattice temperature at 300K (in red). The correlation coefficients can be read diagonally. The self-heating strongly affects the correlation between I_{on} and all other figures of merit.

More than Moore benchmarks

Within the SUPERTHEME project ams AG has defined six benchmarks (B1-4 and D1-2), which were specifically designed to learn about process variability in different technologies of ams's portfolio. Furthermore – as a natural result of SUPERTHEME project – an entire environment of simulation tools and models were developed in order to link process and device simulation, ams explore as well all the development made in this sense.

TSV is a key technology for ams and etch is a critical step on TSV fabrication. It affects directly the final device electrical (resistance, capacitance and inductance) and mechanical (stress) figures, as the via's wall shape is practically defined by the etch parameters (**Figure 23**). In SUPERTHEME work has been carried out to predict which process parameters have more impact on the final electrical and mechanical parameters of the device.

A polyresistor is a rather common structure in semiconductor device, hence a better understanding of its influences a large range of applications. In SUPERTHEME a particular model has been developed which considers the grain in the polysilicon as electrical network of resistive elements (**Figure 24**). The resistivity of each element can be related to the grain size, which depends on thermal conditions during processing. The thermal growth of grains in polyresistor can be obtained by the Potts model (**Figure 25**) and the expected grain size can be readily used for calculation of the resistivity.

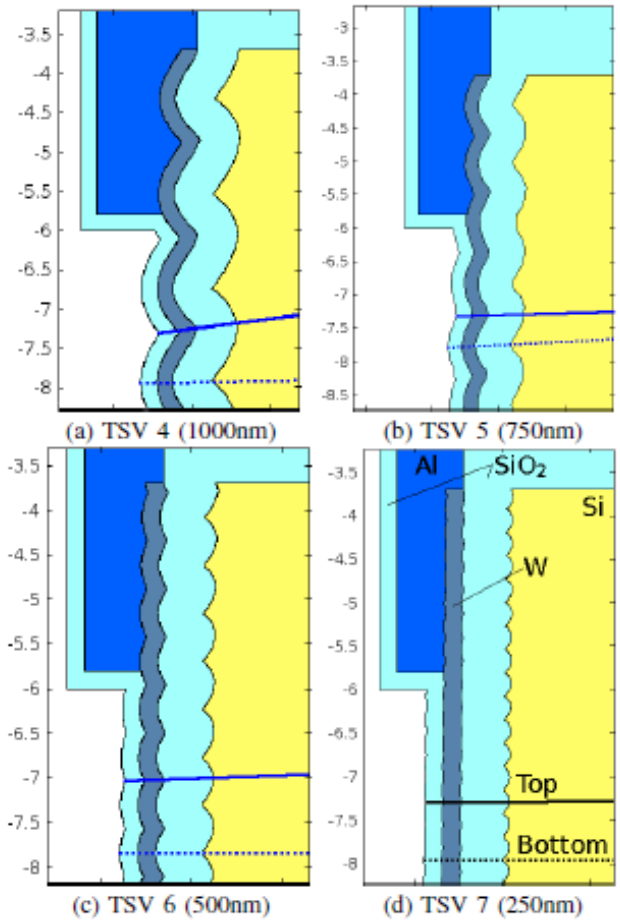


Fig.23: Two dimensional view of the top of the TSV, impact of constant rate on scallops size

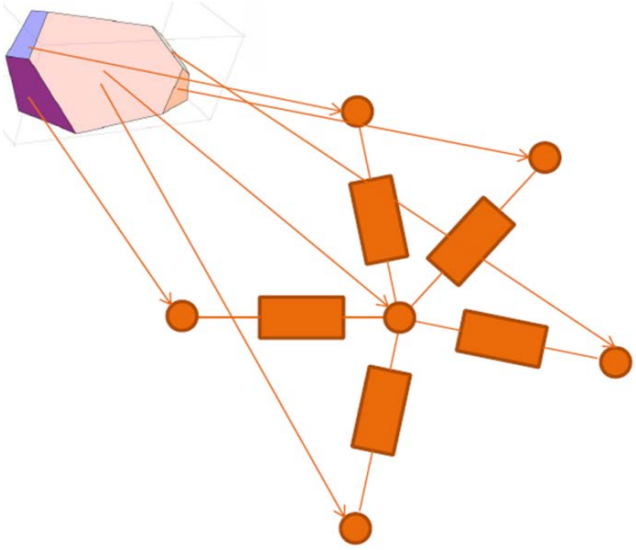


Fig. 24: Network formation for one grain. Each resistor here depicted is the summation of the inner grain resistance and the interface grain-grain resistance.

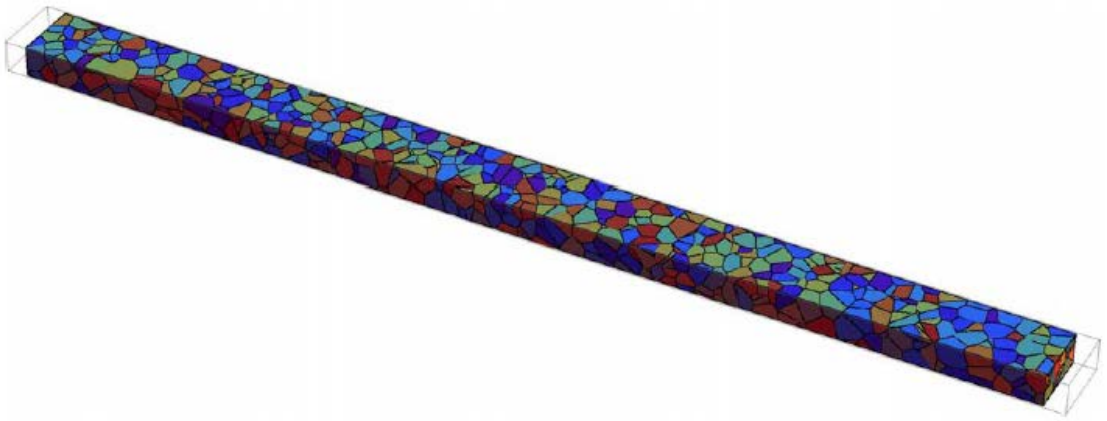


Fig. 25: Grain structure of a poly-silicon resistor. Grain sizes distribution is obtained from the Potts model.

Photodiode and dielectric filter stacks are frequently used for the many optical sensor applications. Depending on the type of photodiodes and dielectric filter stacks, it is possible to introduce various optical sensors in a standard silicon based CMOS technology, which can cover UV, visible light, and near IR regions. Because of the increased complexity and cost issues of a current CMOS technology, it is getting important to know process-induced electrical and optical parameter-shift in advance before fabrication. To investigate the frontend PV effects on the electrical characteristics of photodiodes, critical process variables were chosen from the in-line data analysis for process and device TCAD simulations. This was followed by the equipment-level sputter deposition simulations using DEP3D (developed by Fraunhofer IISB). The main purpose of these simulations is to investigate the reactor geometry process parameter effects on the across-wafer dielectric filter thickness (relative thickness). The information obtained from the sputter deposition simulations will be used for stabilizing across-wafer and wafer-to-wafer dielectric thickness variation.

The motivations and goals of “analog circuit benchmark” are to integrate the results from the SoC benchmarks on a circuit level design mixing a bandgap voltage reference circuit and an operational amplifier circuit. The variability information transferred from the benchmarks studied in the project are in the form of meta-models describing the electrical variation of the related devices (TSV, poly-resistor, diode and interference filter) as a function of the process variations or atomic-level random fluctuations. These models are integrated in the equivalent circuit models representing the devices: RCL equivalent circuit for the TSV (see **Figure 26**), resistor and current source for the photodiode including filter effects.

Based on these models and within the process/equipment parameter ranges studied, we can apply any type of distributions Gaussian or non-Gaussian with any arbitrary correlation. Therefore one can use a random variable into the electric circuit model to account for the variability during process. For illustration purposes, **Figure 27** depicts selected components of the random variable ***A*** for a band gap circuit. Our model well captures parameter correlations as well as Gaussian and non-Gaussian marginal distributions. We implemented this description in Verilog-A to allow faster simulation-based circuit analyses.

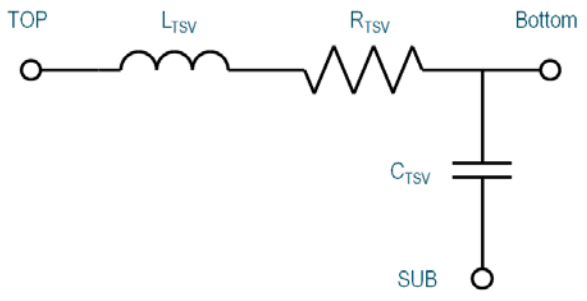


Fig. 26: TSV equivalent circuit.

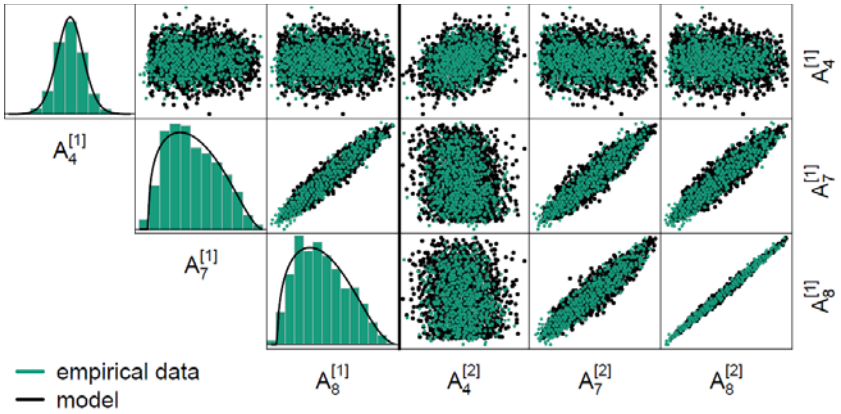


Fig. 27: Selected A coefficients correlation matrix of probabilistic analog behavioral bandgap model.

The same procedure was applied as well for an amplifier circuit. **Figure 28** presents a comparison between the measurements done ams AG and the circuit level simulations done by Fraunhofer EAS/IIS. The model justifies most of the experimental with deviations on the Idd, which are justified by an inadequate setup of the experiment.

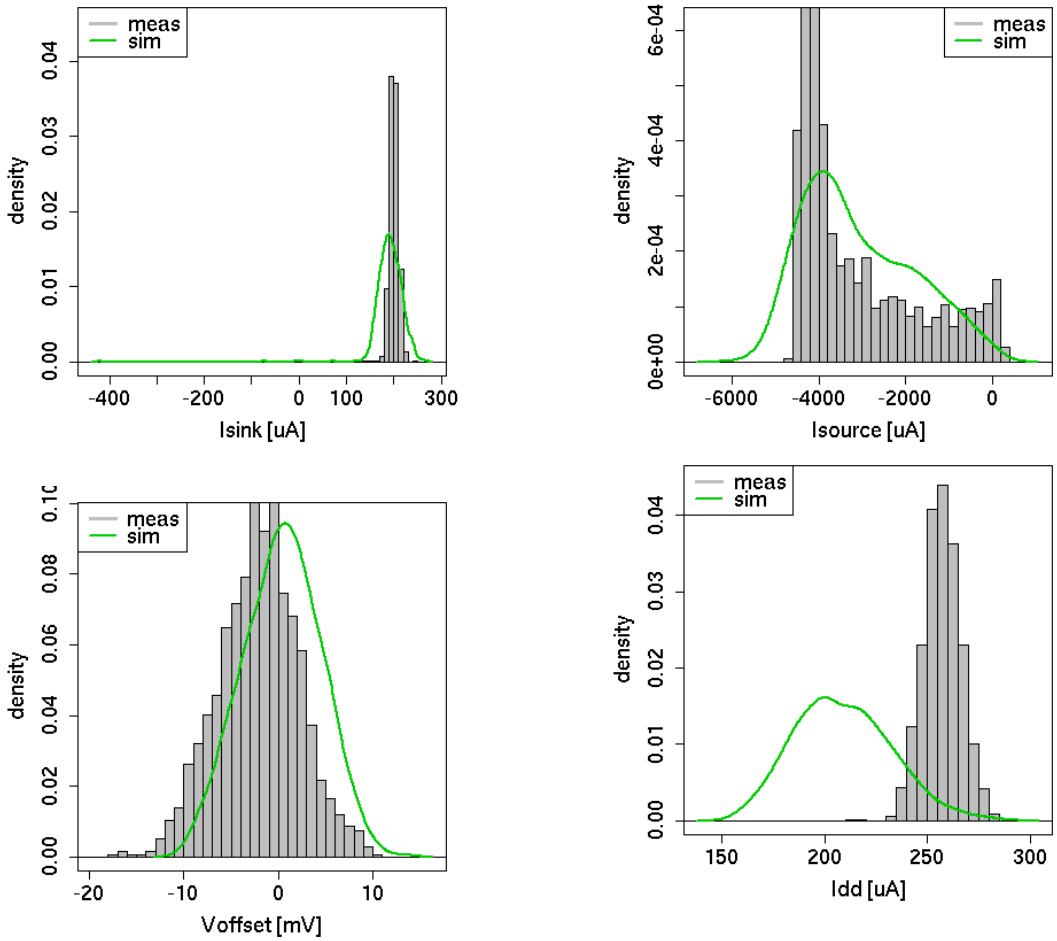


Fig. 28: Comparison of measurements and circuit level simulation on the operational amplifier output.

References for section 4.1

[1] Dr.LiTHO, http://www.drlitho.com
[2] http://www.synopsys.com
[3] ATEMOX
[4] GARAND, http://www.goldstandardsimulations.com
[5] G. Roy, A. R. Brown, F. Adamu-Lema, S. Roy and A. Asenov, IEEE Trans. on Electron Devices, Vol.53, No.12, pp.3063-3070 (2006)
[6] http://www.cadence.com/products/cic/spectre_circuit/pages/default.aspx
[7] http://www.ansys.com
[8] Q-VT plasma processing simulator, 2014, Quantemol Ltd., London. M.J. Kushner, Hybrid modeling of low temperature plasmas for fundamental investigations and equipment design, J. Phys. D: Appl. Phys. 42 (2009) 194013 (20 pp.).
[9] M.J. Kushner, Hybrid modeling of low temperature plasmas for fundamental investigations and equipment design, J. Phys. D: Appl. Phys. 42 (2009) 194013 (20 pp.).
[10] G.B. Raupp, T.S. Cale, H.P.W. Hey, The role of oxygen excitation and loss in plasma enhanced deposition of silicon dioxide from tetraethylorthosilicate, J. Vac. Sci. Technol. B 10 (1992) 37-45.
[11] RandomSpice, http://www.goldstandardsimulations.com
[12] P. Evanschitzky, A. Burenkov, J. Lorenz, Double Patterning: Simulating a Variability Challenge for Advanced Transistors in: Simulation of Semiconductor Processes and Devices (SISPAD) 2013, IEEE, p. 105

Impact and the main dissemination activities and exploitation of results

The potential impact of SUPERTHEME and its dissemination and exploitation activities have been described at the end of the project in the Technology Implementation Plan, which has been provided both in a confidential and a public version. In the following, an excerpt of the public version is given.

Dissemination Actions Carried out in SUPERTHEME

Successful, broad and well targeted dissemination is an essential contribution to the exploitation of the project results. On the other hand it is important to make sure that open dissemination is not negatively affecting commercialization.

In the following the dissemination actions carried out in SUPERTHEME are summarized, referring to the detailed internal plans described in the SUPERTHEME deliverable D1.2. An important additional channel for dissemination, not mentioned in D1.2, has been the SUPERTHEME WWW, www.supertheme.eu: Whereas its public section has been used for broad distribution of selected information to the open public, via a dedicated protected section additionally all documents classified as “restricted” were made available to the members of the Industrial and Scientific Advisory Board of SUPERTHEME. The final content if the SUPERTHEME WWW is summarized in the restricted deliverable D7.3 “Final Version of SUPERTHEME WWW”.

Scientific Publications and Conference Participations

An excerpt from D1.2 is cited in the following in *italics*: “Considerable research activities and high-level scientific results are necessary to achieve the objectives of the SUPERTHEME project. This automatically also includes close interactions with the scientific communities in various fields of TCAD, in order to best consider, use, and compare with developments being made elsewhere.
In consequence, it is vital for the SUPERTHEME project to publish its results at the conferences most important in the field (e.g. SISPAD) and to discuss at these events with the other leading experts in the field. Moreover, publications in leading scientific journals are mandatory to attract attention for the results of the project, in this way also supporting the other dissemination activities outlined below. ….. Partners driving the publication and conference participation actions in SUPERTHEME are primarily the universities and research institutes Fraunhofer IISB, TU Vienna, and Univ. Glasgow.”

Peer-Reviewed Publications

Within SUPERTHEME 8 peer-reviewed papers (including 4 papers from conferences) have been published in renowned journals with a high visibility in the scientific community. The list of the peer-reviewed publications is given in the dissemination table A1 below

Conference Contributions

Due to the topics covered by SUPERTHEME, different scientific areas are relevant in terms of participation in conferences. This includes for instance technology-oriented conferences such as the MAM, device simulation-oriented conferences such as the SISPAD, reliability conferences such as the IRPS, or conferences addressing the circuit level such as the ISCAS. Results of SUPERTHEME have been presented at 21 conferences with a total of 23 conference papers (4 of them as peer-reviewed papers in journals). A complete list of the conferences and the SUPERTHEME papers at these conferences is given in the dissemination table A2 below.

Workshops

An essential part of the SUPERTHEME dissemination strategy has been the organization of or the participation in workshops:

- SUPERTHEME together with the EC FP7 projects TRAMS and MORDRED co-organized the workshop "Variability and Reliability Research in Devices, Circuits, and Systems in Advanced Technologies" linked to ESSCIRC/ESSDERC 2013, on September 20 in Bucharest, Romania. SUPERTHEME contributed with two own presentations plus an invited industrial keynote presentation on variability.
- SUPERTHEME organized the workshop "Variability – from equipment to circuit level" linked to ESSCIRC/ESSDERC 2015, on September 18, 2015, in Graz, Austria. It consisted of six presentations from SUPERTHEME plus three invited presentations from industry and the EC projects MORDRED and MORV, respectively.
- SUPERTHEME presented a poster at the "9th International Nanotechnology Conference on Communication and Cooperation", held on May 14-17, 2013, in Berlin, Germany
- SUPERTHEME presented two posters at the European Nanoelectronics Forum held on November 27-28, 2013, in Barcelona, Spain.
- SUPERTHEME presented a poster at the European Nanoelectronics Forum held on December 1-2, 2015, in Berlin, Germany.

Training of Scientists and Development of Skills in Europe

Another important aspect is the dissemination via development of skills in Europe. SUPERTHEME contributes to this in various respects:

- The research partners in the project (Fraunhofer IISB and EAS, TU Vienna and Univ. Glasgow) employ a considerable share of scientists who join the institutions after their university degrees, gain additional technical and management qualification during their work, under the supervision of senior scientists, and mostly after some years join industry. As far as working on the project, such scientists can in an optimum way transfer knowledge about the application of simulation tools like those developed in SUPERTHEME into the semiconductor industry. In general the regulations in the work contracts with these staff members make sure that although the training and the transfer of application knowledge is beneficial and promoted the IPR of the project partners is protected.
- Whereas Univ. Glasgow and TU Vienna directly educate students, also Fraunhofer IISB (via its close cooperation with the University of Erlangen-Nürnberg) is contributing to the training of graduate and PhD students. This also includes direct participation of these young scientists in the research projects like SUPERTHEME. IPR is protected in a similar way as with other staff members.

Status of SUPERTHEME Exploitation

SUPERTHEME results were exploited in four directions: The integration of software with semiconductor simulation programs, the use of enhanced semiconductor simulation programs for own equipment and process development, the use of enhanced semiconductor simulation programs for research projects, and finally commercialization.

Integration of Software with Semiconductor Simulation Programs

Within the SUPERTHEME Workpackage 5 "Software Integration and variation-Aware Compact Models", relevant background software from the partners and the software modules developed in SUPERTHEME were integrated with each other and with relevant external commercial software like Sentaurus Process[2]. This enabled both the conduction of the benchmark simulations planned in the project and subsequent use for application simulations both by the industrial partners, as outlined below, and by the academic partners Fraunhofer, TU Vienna and Glasgow University in various technology development projects.

Use of the Enhanced Semiconductor Simulation Programs for own Equipment and Process Development

ams

The semiconductor company ams, partner in the project, is one of the key companies for high performance analog semiconductors around the world. Among others this is due to its leading edge products and its efficient and flexible fabrication processes. To support these processes and especially the variety of its products, ams needs advanced process and device simulation tools. Whereas ams primarily uses standard commercial TCAD software, the company has since more than a decade drawn considerable benefit from the active involvement in RTD projects which are dedicated to closing critical gaps in the TCAD software systems available on the market.

Within the SUPERTHEME project ams has defined six benchmarks (B1-4 and D1-2), which were specifically designed to learn about process variability in different technologies of ams's portfolio. The exploitation in each benchmark is proper detailed within the confidential SUPERTHEME deliverable D8.1. Furthermore – as a natural result of SUPERTHEME project – an entire environment of simulation tools and models were developed in order to link process and device simulation.

Equipment companies

The four semiconductor equipment companies ASML, HQ-D, LASSE (formerly Excico) and IBS, partners in the project, derived specifications based both on processes and variations relevant to their equipment, and beyond that derive general specifications for typical equipment for all process steps. The goal for the SUPERTHEME software system is the simulation of the impact of such variations on devices and circuits. As described in the confidential deliverable D8.1, internal exploitation of results from SUPERTHEME at the four equipment companies has been done or enabled as follows:

- ASML: Whereas the primary interest of ASML is in the the impact of the lithography process itself on the feature sizes ("Critical Dimension" CD) and its uniformity (Critical Dimension Uniformity, CDU) across a wafer, the study of the impact of variations in Double Patterning on FinFET based SRAMs led to interesting results that address key performance parameters and its sensitivities to patterning variations. The functionality is interesting for the future development of patterning solutions for logic FEOL, MEOL and BEOL, which are the core business of equipment manufactures.
- HQ-D has primarily benefited from the work on the characterization of its microwave plasma oxidation system and on the extraction of variability data from the equipment. These results significantly contribute to further improvement of the microwave plasma equipment, e.g. in terms of further scaling to smaller dimensions of More Moore devices. Furthermore, the

[2] www.synopsys.com

methodology and toolbox developed and demonstrated will in various respects be useful for preventive maintenance. The simulation results obtained from the cooperation with Fraunhofer IISB helped to far better understand the geometrical plasma distribution below the used array of plasma sources and thus provided helpful inputs in order to improve uniformity of the overall process. HQ-D will use those results to further optimize their systems.

- Work at and with IBS in SUPERTHEME dealt with the IB proprietary plasma doping tool, PULSION®. Within SUPERTHEME a much better understanding of and physical models for plasma doping with Arsenic were developed in cooperation with Fraunhofer IISB. The use of these predictive models is of major interest for IBS. At this date, no commercial solution exists to simulate N type plasma doping, and this can be a barrier for customer to integrate plasma doping in semiconductor process flow. The capability to simulate plasma doping profiles gives to IBS a great technical and commercial advantage, for both internal development and customer demonstration.
- Work at and with LASSE in SUPERTHEME dealt with equipment for sub-µs timeframes. Literature survey and characterization work carried out at LASSE combined with simulation work led to three kinds of exploitation at LASSE:
    - From process integration perspective, the simulation work has been communicated to customers and partners to showcase LASSE simulation capabilities and to answer their request to quantify the impact of key equipment parameters on process integration. Moreover, the experimental data gathered is now used to fine tune designs of experiments and answer customer requests for specific applications.
    - From hardware perspective, the equipment data gathered (energy to pulse duration correlation, stability, etc…) and associated hardware modifications were integrated in an in-house toolbox to be used not only for equipment maintenance and fine-tuning, but also for feasibility experiments for customers (demos) and academic work.

Use of Enhanced Semiconductor Simulation Programs for Research Projects

As foreseen in the Description of Work, background and foreground software developed by Fraunhofer and TU Wien have been interfaced and integrated both with the proprietary software of GU/GSS and with third-party commercial software from the US-based software house SYNOPSYS, which is currently the de-facto industrial standard for Technology Computer Aided Design (TCAD). This has enabled Fraunhofer and TU Wien to utilize in further research those tools which are most suitable, depending on the application problem in question. Selections from the various software tools developed and enhanced as part of this project are among those applied in cooperative projects on sensor development and integration (FP7 project MSP together with ams and others), on modeling of reliability under variability (FP7 project MORV with the SUPERTHEME ISAB members Infineon and IMEC, and others) and on future technologies for lithography with minimum feature sizes (FP7 project CoLiSA.MMP, ECSEL project SeNaTe). The results from SUPERTHEME especially constitute the baseline for the Horizon 2020 project SUPERAID7 (“Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm node”) on the simulation of variability in advanced *More Moore* devices, to be carried out from January 2016 to December 2018 by the SUPERTHEME partners Fraunhofer IISB, GSS, GU and TU Vienna, together with the SUPERTHEME ISAB member CEA/Leti.

Commercialization

Commercialization of the SUPERTHEME results within the field of nanoelectronics is primarily being done via the software house partner GSS. Compatibility with other software is a major selling point for this software house. GSS already works successfully in the TCAD market with device and

compact simulation software specifically tailored to dealing with the impact of statistical variations. This software has been extended in SUPERTHEME both by the work carried out by GSS and GU and by the additional options provided by the project partners Fraunhofer IISB and TU Vienna.

GSS is a UK based software company providing complete solutions for Design Technology Co-Optimisation (DTCO), PDK development and exploration and the screening of future technology options. The GSS tool chain integrates predictive TCAD simulations, statistical compact model extraction and high sigma statistical circuit simulation using 'push button' cluster-based technology.

Over the course of the project, the research and development enabled by SUPERTHEME has significantly enriched the capabilities of the tool chain offered by GSS for commercial customers. The combination of tools enables GSS' customer to accurately model the impact of the combined sources of stochastic and systematic variability from its sources at the atomic level to devices and circuits.

Thanks to the SUPERTHEME project, GSS has benefited from significant R&D, physical model development and the development of automation and productivity tools that has been undertaken in order to fulfil the goals of the project. These have directly impacted on many of the components of the GSS tool chain. In a more general sense GSS has also benefited from the development of interfaces to commercially available external tools such as Sentaurus Process from Synopsys and Dr.LiTHO produced by Fraunhofer IISB as well as from active collaborations with Fraunhofer IISB, The University of Glasgow and TU Vienna.

During the SUPERTHEME project GSS has undertaken significant software development and R&D activities which have directly impacted the commercial software offerings provided by the company, enabling business development activities and delivering unparalleled capabilities to the global semiconductor industry. In particular the capabilities for process and statistically aware compact modelling, integration of the full tool chain and the development of the Enigma automation and productivity framework have helped to advance the position of GSS from a start-up company to globally recognised and trusted software provider. Due, in no small part, to the capabilities developed during the timescale of the SUPERTHEME project GSS has significantly increased its customer base and has grown by nearly 400%, including tool installations with several leading foundry customers worldwide. Participation in SUPERTHEME has enabled GSS to include a unique focus on design-technology co-optimisation (DTCO) in its toolchain. Consequently, this puts GSS in unique position to exploit this market, worth an estimated $25-100 million/year.

During the course of the SUPERTHEME project GSS has been fortunate to benefit from active and fruitful collaborations with the Fraunhofer institutes in both Erlangen and Dresden and with the University partners at both TU Wien and Glasgow University. Specifically, these collaborations have led to jointly developed foreground IP for thermal modelling[3] and advanced quantum transport simulation which are in the process of being integrated into the GSS GARAND simulator (see deliverable D4.5 for more information). From GSS' perspective the principle route for exploitation of project developed foreground IP is via product and feature development in the software produced by the company.

Furthermore, GSS has been able to file three patents relating to the technology developed during the course of SUPERTHEME. The first relates to parameter generation for compact models for transistors subject to BTI-induced ageing. The second relates to parameter generation for compact models

[3] Wang, L.; Brown, A.R.; Nedjalkov, M.; Alexander, C.; Cheng, B.; Millar, C.; Asenov, A., "3D electro-thermal simulations of bulk FinFETs with statistical variations," in Simulation of Semiconductor Processes and Devices (SISPAD), 2015 International Conference on , vol., no., pp.112-115, 9-11 Sept. 2015

for transistors subject to global, local and combined process variations. This technology was developed exclusively as part of SUPERTHEME. The final leverages this technology for application to mobility modelling for TCAD simulation. An additional patent is also currently under preparation.

There will also be continuation of the technology development initiated during SUPERTHEME at GSS through the new European projects CONNECT, SUPERAID7 and REMINDER. These projects aim to take the technology developed here and apply and enhance it to *More Moore* and *More than Moore* areas of research. In particular, the technology will be developed and applied to novel materials and architectures, such as carbon nanotubes; and to other design aspects such as interconnects.

Project web site

www.supertheme.eu

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Use and dissemination of foreground

"A plan for use and dissemination of foreground (including socio-economic impact and target groups for the results of the research) shall be established at the end of the project. It should, where appropriate, be an update of the initial plan in Annex I for use and dissemination of foreground and be consistent with the report on societal implications on the use and dissemination of foreground (section 4.3 – H).

The plan should consist of:

- *Section A*

  This section should describe the dissemination measures, including any scientific publications relating to foreground. ***Its content will be made available in the public domain*** *thus demonstrating the added-value and positive impact of the project on the European Union.*

- *Section B*

  This section should specify the exploitable foreground and provide the plans for exploitation. All these data can be public or confidential; the report must clearly mark non-publishable (confidential) parts that will be treated as such by the Commission. Information under Section B that is not marked as confidential ***will be made available in the public domain*** *thus demonstrating the added-value and positive impact of the project on the European Union."*

Dissemination and exploitation actions have been described in the public section 4.1 above, based on the public deliverable D1.11 "Public version of the Technology Implementation Plan". Peer-reviewed publications and other dissemination actions are listed below in tables A1 and A2, respectively. Some further information on SUPERTHEME dissemination and exploitation actions are given in the confidential deliverable D1.11 "Technology Implementation Plan" and in the restricted deliverable D8.1 "Report on present and expected use of SUPERTHEME results". Further information on IP and patents is given in the confidential tables B1 and B2.

Section A (public)

This section includes two templates

- Template A1: List of all scientific (peer reviewed) publications relating to the foreground of the project.
- Template A2: List of all dissemination activities (publications, conferences, workshops, web sites/applications, press releases, flyers, articles published in the popular press, videos, media briefings, presentations, exhibitions, thesis, interviews, films, TV clips, posters).

These tables are cumulative, which means that they should always show all publications and activities from the beginning until after the end of the project. Updates are possible at any time.

TEMPLATE A1: LIST OF SCIENTIFIC (PEER REVIEWED) PUBLICATIONS, STARTING WITH THE MOST IMPORTANT ONES

NO.	Title	Main author	Title of the periodical or the series	Number, date or frequency	Publisher	Place of publication	Year of publication	Relevant pages	Permanent identifiers[4] (if available)	Is/Will open access[5] provided to this publication?
1	Impact of Self-Heating on the Statistical Variability in Bulk and SOI FinFETs	L. Wang (GU)	IEEE Trans. Electr. Dev.	62	IEEE	Piscataway	2015	pp. 2106-2112	http://dx.doi.org/10.1109/TED.2015.2436351	no
2	The Effects of Etching and Deposition on the Performance and Stress Evolution of Open Through Silicon Vias	L. Filipovic (TUW)	Microelectr. Reliab.	54	Elsevier	Amsterdam	2014	pp. 1953-1958	http://dx.doi.org/10.1016/j.microrel.2014.07.014	no
3	Numerical Evaluation of the	A. Burenkov	J. Comput.	14	Springer	Berlin	2015	pp.	http://dx.doi.org/10.	no

[4] A permanent identifier should be a persistent link to the published version full text if open access or abstract if article is pay per view) or to the final manuscript accepted for publication (link to article in repository).
[5] Open Access is defined as free of charge access for anyone via Internet. Please answer "yes" if the open access to the publication is already established and also if the embargo period for open access is not yet over but you intend to establish open access afterwards.

	ITRS Transistor Scaling	(Fraunhofer)	Electron.					192-202	1007/s10825-014-0638-0	
4	Modeling Carrier Mobility in Nano-MOSFETs in the Presence of Discrete Trapped Charges: Accuracy and Issues	S. Amoroso (GSS)	IEEE Trans. Electr. Dev.	61	IEEE	Piscataway	2014	pp. 1292-1298	http://dx.doi.org/10.1109/TED.2014.2312820	no
5	Simulation of Thermo-mechanical Effect in Bulk-silicon FinFETs	A. Burenkov (Fraunhofer)	Mat. Sci. Semicond. Proc.	42	Elsevier	Amsterdam	2015	pp. 242-246	http://dx.doi.org/10.1016/j.mssp.2015.07.022	no
6	Intrinsic stress analysis of tungsten-lined open TSVs	L. Filipovic (TUW)	Microelectr. Rel.	56	Elsevier	Amsterdam	2015	pp. 1843-1848	http://dx.doi.org/10.1016/j.microrel.2015.06.014	no
7	Coupled Simulation to Determine the Impact of across Wafer Variations in Oxide PECVD on Electrical and Reliability Parameters of Through-silicon Vias	E. Baer (Fraunhofer)	Microelectr. Eng.	137	Elsevier	Amsterdam	2015	pp. 141-145	http://dx.doi.org/10.1016/j.mee.2014.11.014	no
8	Decoherence and time reversibility: The role of randomness at interfaces	M. Nedjalkov (TUW)	J. Appl. Phys.	114	AIP	Melville	2013	174902 (7 pages)	http://dx.doi.org/10.1063/1.4828736	no

TEMPLATE A2: LIST OF DISSEMINATION ACTIVITIES								
NO.	Type of activities[6]	Main leader	Title	Date/Period	Place	Type of audience[7]	Size of audience	Countries addressed
2012 and continuous activities								
1	Web	Fraunhofer	www.supertheme.eu	Released November 6, 2102, continuously updated	N/A	Scientific Community, Industry, Civil Society	N/A	International
2	Other	All	Interaction with the Industrial and Scientific Advisory Board	Project period	N/A	Industry, Scientific Community	8 institutions	European
3	Press release	Fraunhofer	Advanced Simulation Tools to Fight Microchip Variations	November 13, 2012	N/A	Medias	N/A	International
2013								
4	Publication	Fraunhofer	Simulations minimize the effect of process variations (published in: Fraunhofer Microelectronic News)	April 2013	N/A	Scientific Community, Industry, Civil Society	N/A	International
5	Conference	Fraunhofer	9th International Nanotechnology Conference on Communication and Cooperation (INC9) (SUPERTHEME overview posters)	May 14-17, 2013	Berlin	Scientific Community, Policy Makers	300	International

[6] A drop down list allows choosing the dissemination activity: publications, conferences, workshops, web, press releases, flyers, articles published in the popular press, videos, media briefings, presentations, exhibitions, thesis, interviews, films, TV clips, posters, Other.

[7] A drop down list allows choosing the type of public: Scientific Community (higher education, Research), Industry, Civil Society, Policy makers, Medias, Other ('multiple choices' is possible).

6	Conference	Fraunhofer, GSS, GU, TUW	International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) 2013 (2 SUPERTHEME papers)	September 3-5, 2013	Glasgow, UK	Scientific Community	200	International
7	Conference	Fraunhofer	European Nanoelectronics Forum 2013 (SUPERTHEME overview posters)	November 27-28, 2013	Barcelona, Spain	Scientific Community, Policy Makers	300	International
2014								
8	Conference	ams, Fraunhofer, TUW	Materials for Advanced Metallization (MAM) 2014 (1 SUPERTHEME paper)	March 2-5, 2014	Chemnitz, Germany	Scientific Community	100	International
9	Conference	Fraunhofer, GSS, GU	Ultimate Integration on Silicon (ULIS) (1 SUPERTHEME paper)	April 7-9, 2014	Stockholm, Sweden	Scientific Community	100	International
10	Conference	TUW	IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE) 2014 (1 SUPERTHEME paper)	April 7-9, 2014	Ghent, Belgium	Scientific Community	300	International
11	Conference	TUW	International Reliability Physics Symposium (IRPS) 2014 (1 SUPERTHEME paper)	June 1-5, 2014	Hawaii, USA.	Scientific Community	300	International
12	Conference	Fraunhofer, IBS	International Conference on Ion Implantation Technology (IIT) 2014 (1 SUPERTHEME paper)	June 26 – July 4, 2014	Portland, USA	Scientific Community	200	International
13	Conference	TUW	International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA) 2014) (1 SUPERTHEME paper)	June 30 – July 4, 2014	Singapore	Scientific Community	200	International
14	Conference	ams, Fraunhofer, GSS, GU, TUW	International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) 2014 (4 SUPERTHEME papers)	September 9-11, 2014	Yokohama, Japan	Scientific Community	200	International
15	Conference	TUW	European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF) 2014 (1 SUPERTHEME paper)	September 29 – October 2, 2014	Berlin	Scientific Community	200	International
16	Conference	GSS, GU	12th International Conference on Solid-State and Integrated Circuit Technology (ICSICT	October 28-31, 2014	Gunxi	Scientific Community	300	International

			2014) (1 SUPERTHEME paper)					
				2015				
17	Conference	Fraunhofer	E-MRS Spring Meeting 2015 (1 SUPERTHEME paper)	May 11-15, 2015	Lille, France	Scientific Community	750	International
18	Conference	Fraunhofer	IEEE International Symposium on Circuits and Systems (ISCAS) 2015 (1 SUPERTHEME paper)	May 24-27, 2015	Lisbon, Portugal	Scientific Community	1000	International
19	Conference	ams, TUW	VARI 2015, 6th International Workshop on CMOS Variability (1 SUPERTHEME paper)	September 1-4, 2015	Bahia, Brasil	Scientific Community	200	International
20	Conference	GSS, GU	2015 International Workshop on Computational Electronics (IWCE) (1 SUPERTHEME paper)	September 2-4, 2015	West Lafayette, USA	Scientific Community	200	International
21	Conference	Fraunhofer, GSS, GU, IBS, TUW	International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) 2015 (3 SUPERTHEME papers)	September 9-11, 2015	Washington DC, USA	Scientific Community	200	International
22	Conference	Fraunhofer	European Nanoelectronics Forum 2015 (SUPERTHEME overview posters)	December 1-2, 2015	Berlin, Germany	Scientific Community, Policy Makers	300	International
23	Workshop	Fraunhofer, ams, GSS, GU	Public Workshop on Variability (organized by SUPERTHEME)	September 18, 2015	Graz, Austria	Scientific Community, Industry	30	International
24	Conference	TUW	European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF) 2015 (1 SUPERTHEME paper)	October 5-9, 2016	Toulouse	Scientific Community	200	International
				2016				
25	Conference	GSS, GU	Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS) 2016 (1 SUPERTHEME paper)	January 25-27, 2016	Vienna, Austria	Scientific Community	150	International