# Outline and Selected Results of the EC FP7 Project SUPERTHEME

Juergen Lorenz
Fraunhofer IISB, Erlangen, Germany


SISPAD 2016 Workshop “Variability-Aware Design Technology Co-Optimization”
Nuremberg, September 5, 2016



## OUTLINE

- Introduction
- Background pillars: Process and device
- Consortium and project data
- Project structure
- Methodology used
- Example: 23.5 nm transistor
- Some glimpse on further results ….
- Conclusion

# Introduction: Variations

- Many variations have their source at equipment level
  - ⇒ Equipment and process simulation core parts of the project
- Examples for variations at equipment level:
  - Lithography: Defocus; dose variations; (mis-)alignment, …
  - Etching/deposition: Inhomogeneities of gas flow, temperature; drifts, chamber coating; source characteristics, …
  - Ion implantation: Variations of angle(s) and dose; statistics, …
  - Annealing: Temperature variations in space/time, …
- Additional pattern-induced variations



# Introduction: Variations (II)

- Challenge: Insufficient quantitative data on variations in equipment
  - Data can only be gathered by / in cooperation with equipment companies
  - Use data from literature plus experiment on selected tools
- Combination with treatment of statistical variations necessary

⇒ Challenge: Predictive simulation chain equipment/process/ device/circuit for variations needed

# Introduction: SUPERTHEME Objectives

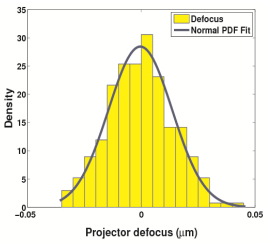
Full project name ”Circuit Stability Under Process Variability and Electro-Thermal-Mechanical Coupling“

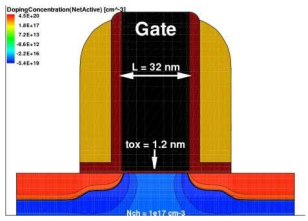
- Development of a software system for the simulation of the impact of systematical and statistical process variations
- Extend / integrate SW of partners + required third-party SW
- Data reduction / hierarchical simulation needed – from discretization of equipment to compact models
- Collect data for variability at process level
- Include thermal and mechanical effects
- Challenge: Correlations of variations must be included
- Exploit background of partners esp. for variabiliy simulation

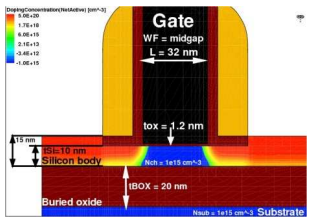


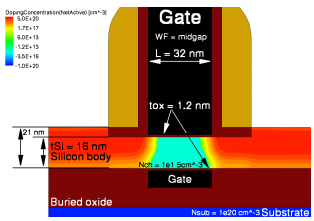
# Background Pillars: Process – IISB

## E.g: Impact of lithography focus variations on transistor performance



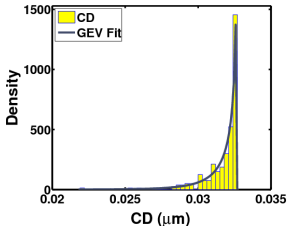



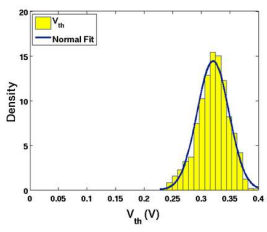

Focus variations
⇩
CD variations

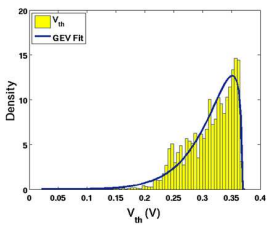
Bulk

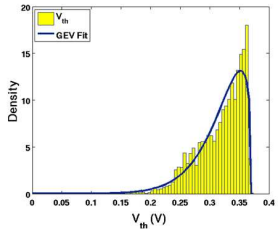
Device architecture
SG FD SOI
DG FD SOI

acts as filter for CD variations and leads to variations e.g. of $V_{th}$



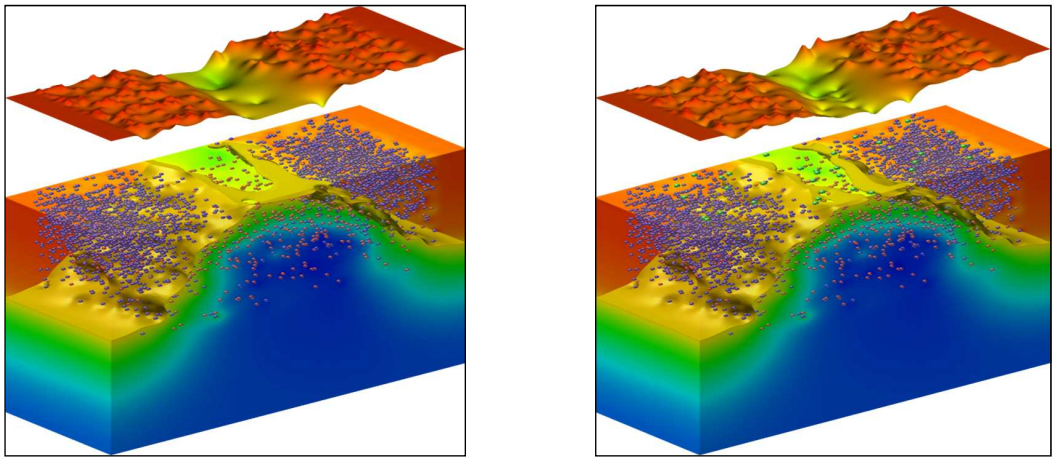




J. Lorenz et al., *Proc. 2009 Intl. Symposium on VLSI Technology, Systems and Applications*, Hsinchu, Taiwan, 2009, pp. 17-18.

# Background Pillars: Device – GU/GSS

## Device simulation SW for the study of the impact of variations caused by the granularity of matter, esp. RDF, LER, MGG



Left: Simulation of a 45 nm technology transistor in the presence of discrete dopant, line edge roughness and polysilicon gate granularity. Right: Simulation of the same transistor subject to degradation. By chance two holes are trapped in the vicinity of the percolation path. From GU / GSS



# Consortium and Project Data

- Project partners
  - Semiconductor industry: ams
  - Equipment companies: ASML, HQD, IBS, Excico/LASSE
  - SW house: GSS
  - Research institutes: Fraunhofer IISB (coord.), IIS/EAS
  - Universities: Univ. Glasgow, TU Wien
- Project period: 10/2012 – 12/2015
- EC funding: 3.3 M€ from FP7 ICT Call 8
- Action line 3.1 “Very advanced nanoelectronic design, engineering, technology and manufacturability“
- See www.supertheme.eu

# SUPERTHEME Project Structure

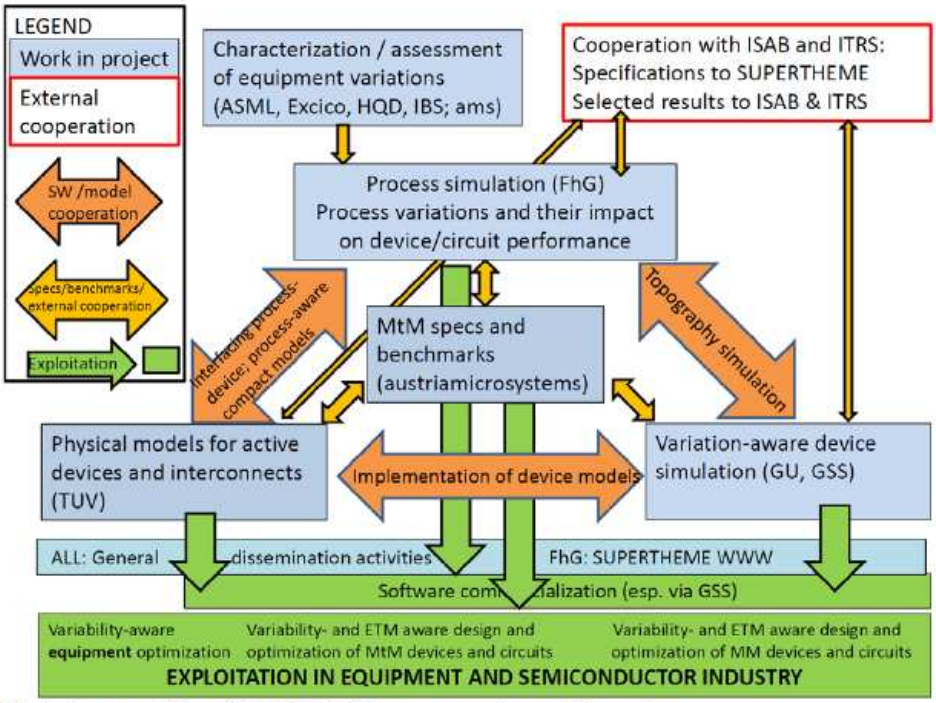
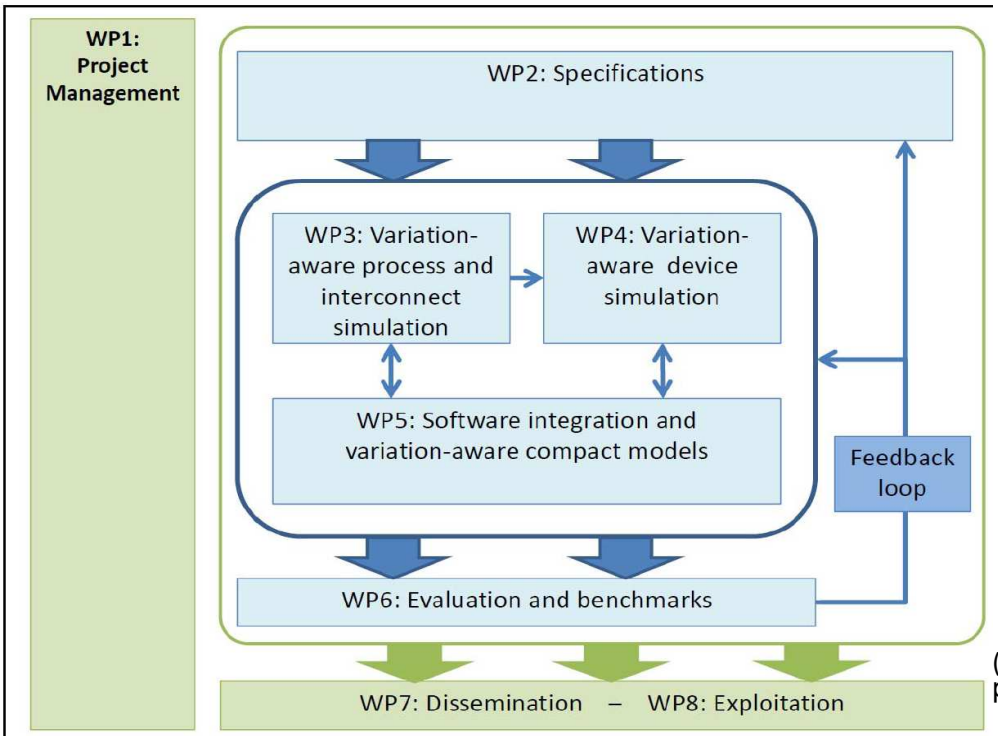


Fig. 2: Focal activities of SUPERTHEME partners and mutual interactions

(From SUPERTHEME proposal and DoW)



# SUPERTHEME Project Structure

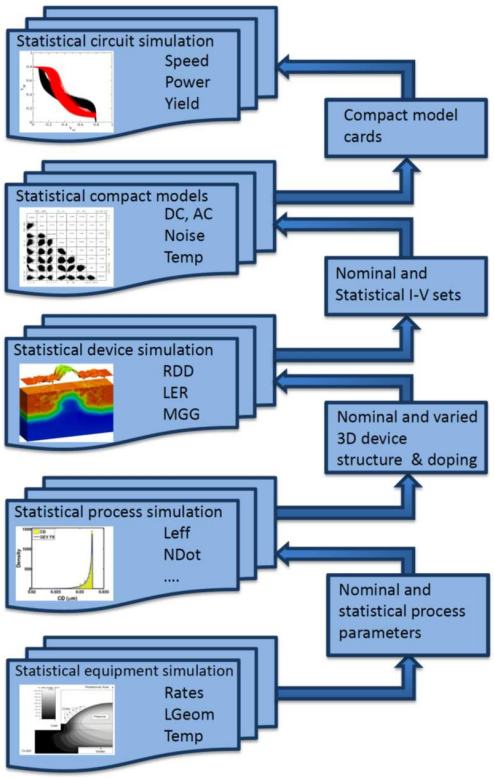



(From SUPERTHEME proposal and DoW)

# Methodology Used

## Simulation levels and tools used

- Equipment simulation: Q-VT (Quantemol), CFD-ACE (ESI Group)
- Process simulation:
  - Lithography: Dr.LiTHO (Fraunhofer)
  - Etching/deposition: ANETCH / DEP3D (Fraunhofer)
  - Implantation/annealing: Sentaurus Process (SNPS)
- Device simulation: GARAND (GSS)
- Statistical compact model extraction: MYSTIC (GSS)
- (Circuit simulation: RandomSpice (GSS))

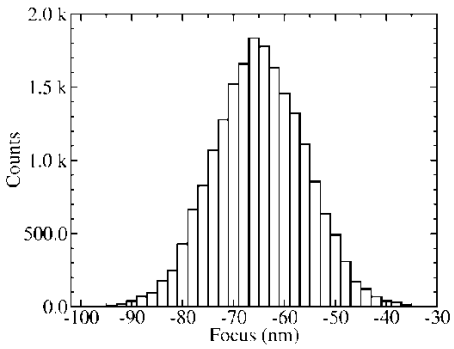


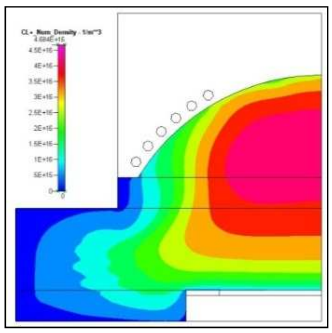

From J. Lorenz et al, SISPAD 2014



# Methodology Used: Source of Variations

- Assumed variations at equipment level – probability density p(P) of some varying parameter P (e.g. litho defocus/dose; position on wafer)



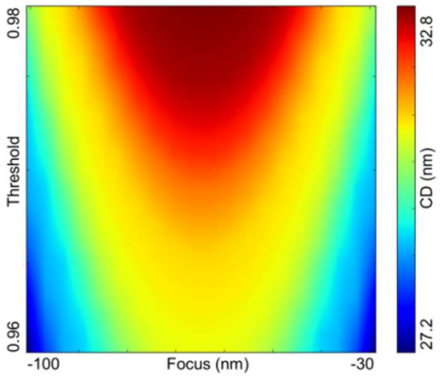
. . . . . .

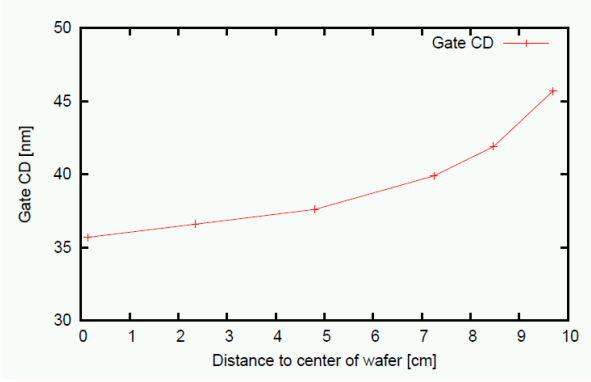
From J. Lorenz et al, SISPAD 2014

# Methodology Used: Tracing Process Variations

- Integrated equipment and process simulation

⇨ Variation of device geometries (and continuum doping) caused by process or equipment variations – e.g. *L(P)* and *W(P)*: ***Device Defining Data D3***



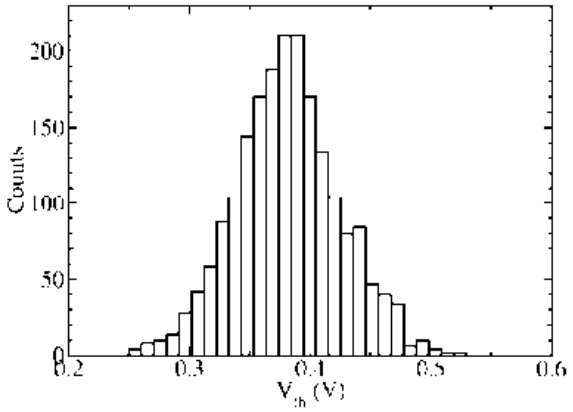

From J. Lorenz et al, SISPAD 2014



# Methodology Used: Statistical Device Simulation

- Statistical device simulation based on geometries and doping of continuum devices (e.g. matrix of *L* and *W*), including RDF, MGG, LER

⇨ Statistical probability densities $g_s$ of electrical data for devices with identical geometry/continuum doping profiles




From J. Lorenz et al, SISPAD 2014

# Methodology Used: Variation-Aware Compact Model

- Combination of equipment/process and device level by taking probability of geometry/continuum doping into account
- Extraction of hierarchical compact model

⇨ Statistical distribution $h_s$ of electrical data for given probability p(P) of some varyiing process parameters (e.g. distribution of focus, dose, energy in PI3 implantation, temperature profiles in annealing, ….

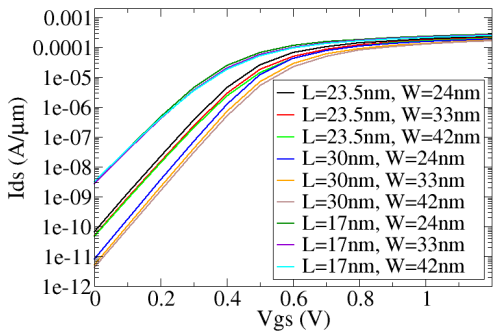
$$h_s = \int g_s(L(P),W(P))\, p(P)\, dP$$



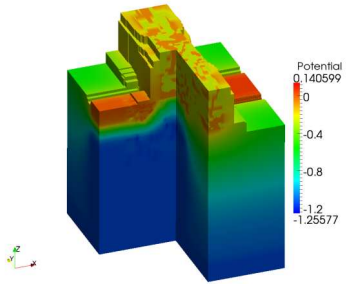
# Example: 23.5 nm CMOS Transistor

- Continuum devices considered: Planar bulk NMOS transistors,
  - Mean values L =23.5nm, W =33nm
  - 5 x 5 matrix, L between 17nm and 30nm, W between 24nm and 42nm

❑ Example of results for continuum devices

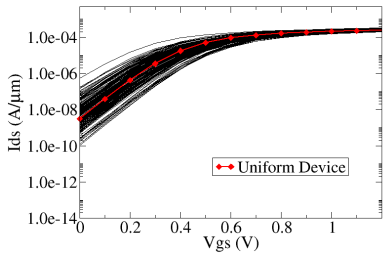



❑ Potential for nominal device with RDF, MGG and LER (simulated with GARAND)

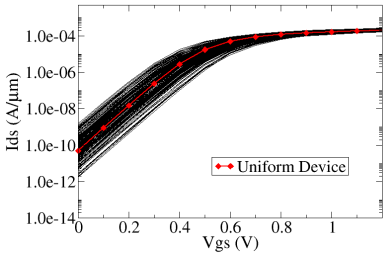


# Example: 23.5 nm CMOS Transistor (II)

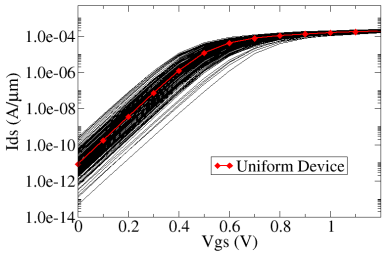
- Statistical device simulation including RDF, MGG and LER for matrix of 5 x 5 continuum devices
- Example: Output characteristics at $V_D$= 0,05V for devices with different L and W




*min. L / max W*
*L= 17 nm, W= 42 nm*




*nominal device*
*L = 23.5nm, W = 33 nm*



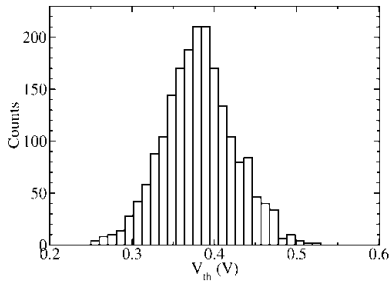

*max. L / min. W*
*L = 30 nm, W = 24 nm*

From J. Lorenz et al, SISPAD 2014

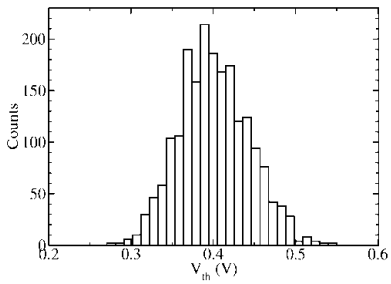


# Example: 23.5 nm CMOS Transistor (III)

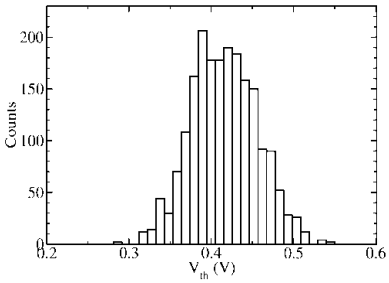
- Statistical device simulation including RDF, MGG and LER for matrix of 5 x 5 continuum devices
- Example: Probability densities for $V_{th}$ at $V_D$ = 0,05 V for devices with different L and W: Different minimum, mean and maximum values of $V_{th}$ distribution




*min. L / max W*
*L= 17 nm, W= 42 nm*




*nominal device*
*L = 23.5nm, W = 33 nm*



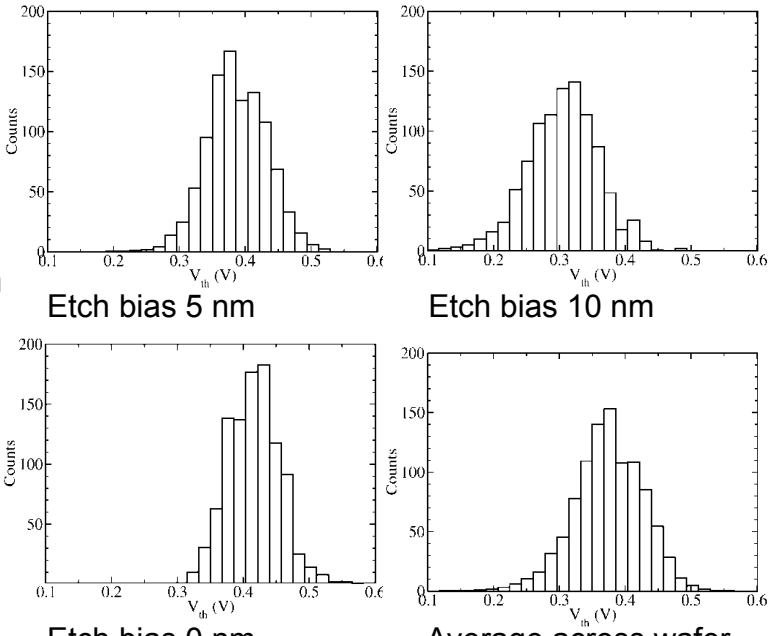

*max. L / min. W*
*L = 30 nm, W = 24 nm*

From J. Lorenz et al, SISPAD 2014

# Example: 23.5 nm CMOS Transistor (IV)

- Hierarchical compact model extracted
- Simulation of coupled influence from lithography (focus, dose), etching (equipment-induced bias variations), RDF, LER, MGG
- Example: $V_{th}$ for average etch bias (5nm) and for different positions at the wafer
- PDF caused by litho variations, RDF, LER and MGG is strongly modified by etch bias variations across wafer

From J. Lorenz et al, SISPAD 2014





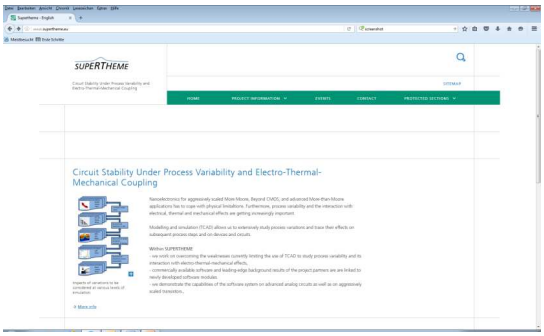

# Some glimpse on further results (I)

SUPERTHEME

- This workshop:
  - Presentation by M. Nedjalkov
  - Presentation by C. Millar
- SISPAD 2016 conference:
  - Variability simulation of 14 nm FinFET: Combined impact of systematic variations and pattern effects in SADP, and statistical variations: Papers O14.1 by E. Bär et al. and O14.2 by X. Wang et al.
  - Uniformity of growth rates in plasma-enhanced oxidation: Paper O8.3 by E. Bär and J. Niess

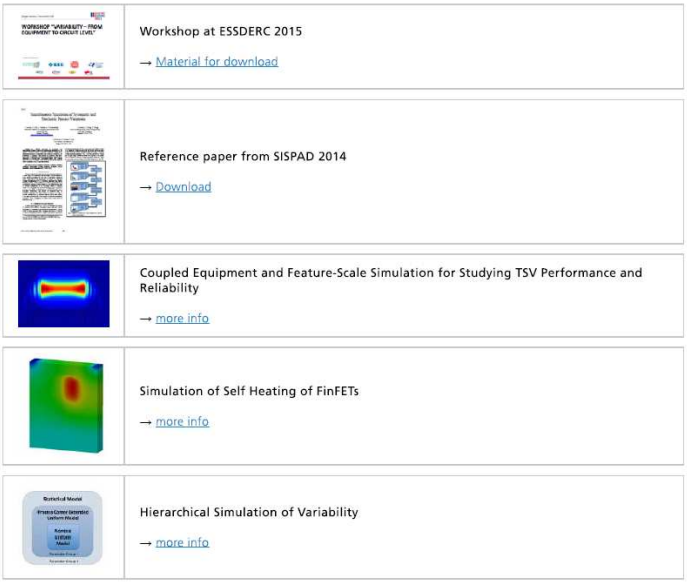
# Some glimpse on further results (II & III)

- SUPERTHEME WWW page at www.supertheme.eu:




- SUPERTHEME Highlights at WWW page

Below you will find project highlights (including references). Material for download can also be found in the sections on Events and Publications.






# Some glimpse on further results (IV)

SUPERTHEME

- 27 publications until beginning of 2016 – more being added:

**SUPERTHEME Overview Posters**

SUPERTHEME Posters shown at the European Nanoelectronics Forum 2015, December 1-2, Berlin

SUPERTHEME Posters shown at the European Nanoelectronics Forum 2013, November 27-28, Barcelona

SUPERTHEME Poster for 9th International Nanotechnology Conference on Communication and Cooperation (INC9), Berlin, May 14-17, 2013

**Publications 2016**

A. Burenkov, J. Lorenz, Simulation of Thermo-mechanical Effect in Bulk-silicon FinFETs, Materials Science in Semiconductor Processing 42 (2016) 242

L. Wang, T. Sadi, M. Nedjalkov, A. R. Brown, C. Alexander, B. Cheng, C. Millar, A. Asenov, Simulation Analysis of the Electro-thermal Performance of SOI FinFETs, in: Proc. of Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS) 2016

**Publications 2015**

E. Baer, P. Evanschitzky, J. Lorenz, F. Roger, R. Minixhofer, L. Filipovic, R.L. de Orio, S. Selberherr, Coupled Simulation to Determine the Impact of across Wafer Variations in Oxide PECVD on Electrical and Reliability Parameters of Through-silicon Vias, Microelectronic Engineering 137 (2015) 141

A. Burenkov, J. Lorenz, Y. Spiegel, F. Torregrosa, Simulation of Plasma Immersion Ion Implantation into Silicon, in: Proceedings of Conference on Simulation of Semiconductor Processes and Devices 2015 (SISPAD 2015), p. 218 Download

L. Filipovic, A.P. Singulani, F. Roger, S. Carniello, S. Selberherr, Intrinsic Stress Analysis of Tungsten-lined open TSVs, Microelectr. Reliab. 55 (2015) 1843

A. Lange, I. Harasymiv, O. Eisenberger, F. Roger, J. Haase, R. Minixhofer, Towards Probabilistic Analog Behavioral Modeling, in: Proc. of 2015 IEEE International Symposium on Circuits and Systems (ISCAS), p. 2728 Download

R. Nagy, A. Burenkov, J. Lorenz, Numerical Evaluation of the ITRS Transistor Scaling, J. Comput. Electron. 14 (2015) 192

F. Roger, A. Singulani, S. Carniello, L. Filipovic, S. Selberherr, Global Statistical Methodology for the Analysis of Equipment Parameter Effects on TSV Formation, in: Proceedings VARI Conference 2015, p. 39

L. Wang, A. R. Brown, M. Nedjalkov, C. Alexander, B. Cheng, C. Millar, A. Asenov, Impact of Self-Heating on the Statistical Variability in Bulk and SOI FinFETs, IEEE Trans. Electr. Dev. 62 (2015) 2106

. . . . . .

# Conclusions

- SUPERTHEME has demonstrated:
  - Feasibility of hierachical variability simulation equipment/process/device/circuit
  - Important impacts on device and circuits
  - Correlations can and must be included
  - Gaussian sources of variability frequently lead to highly non-Gaussian variations at device or circuit level
- Very promising prospects for application and extension of work
- Follow-up activities on aggressively scaled nanotransistors in EC Horizon 2020 project SUPERAID7



# Acknowledgements

- Contribution of all colleagues at partners highly appreciated
- Valuable inputs from EC review team and from SUPERTHEME ISAB
- Funding from EC highly appreciated

This project has received funding from the European Union's Seventh Framework Programme for research, technological development and demonstration under grant agreement no 318458.