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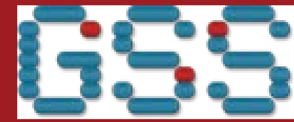
European Project SUPERTHEME



PROCESS VARIATIONS

- Equipment-induced inhomogeneities of process results – e.g. layer thickness across wafer
- Uncertainties / drifts of equipment settings – e.g. distance between last lense and illuminated area in lithography
- Stochastic variations of process results due to granularity of matter – e.g. random dopant fluctuations (RDF) for very small devices with only some dopants in the channel

IMPACT OF PROCESS VARIATIONS

- Process variations are propagated through the fabrication process
- Consequence: Variations of device (e.g. threshold voltage) and circuit properties (e.g. static noise margin) – reducing yield

CURRENT STATUS IN SIMULATION

- Device simulation based on simple assumptions for only some process variations – esp. RDF
- Most process variations (e.g. variations of gate length and width) not considered

SUPERTHEME PROJECT

- Close critical gaps: Simulate variations from their source (largely at equipment level) up to device and circuit level
- Include electro-thermal-mechanical effects
- Complement commercial software with tools from consortium
- Funded by European Union within FP7 from Oct. 2012 to Sept. 2015, grant agreement no. 318458

CONSORTIUM

- Semiconductor company: ams
- Equipment companies: ASML, HQD, Excico, IBS
- Software house: GSS
- Research institutes: Fraunhofer IISB (coordinator), Fraunhofer IIS/EAS
- Universities: Univ. Glasgow, TU Vienna

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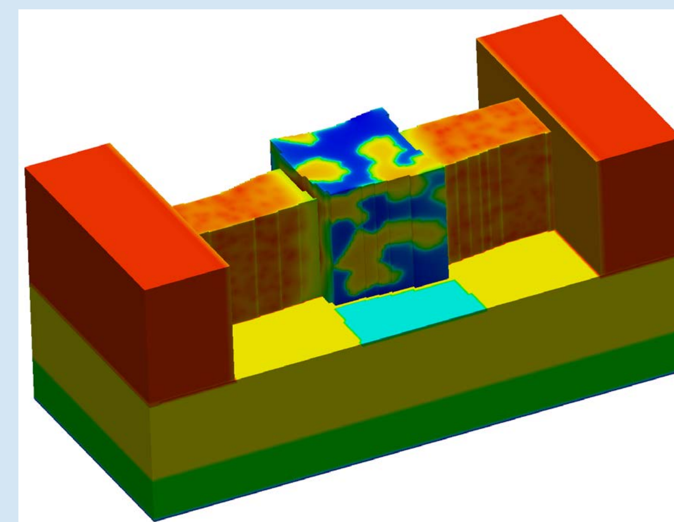
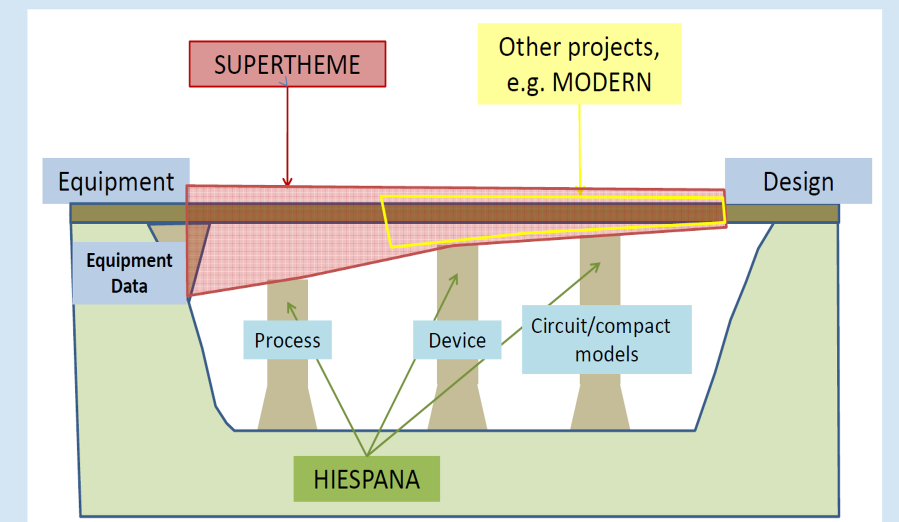
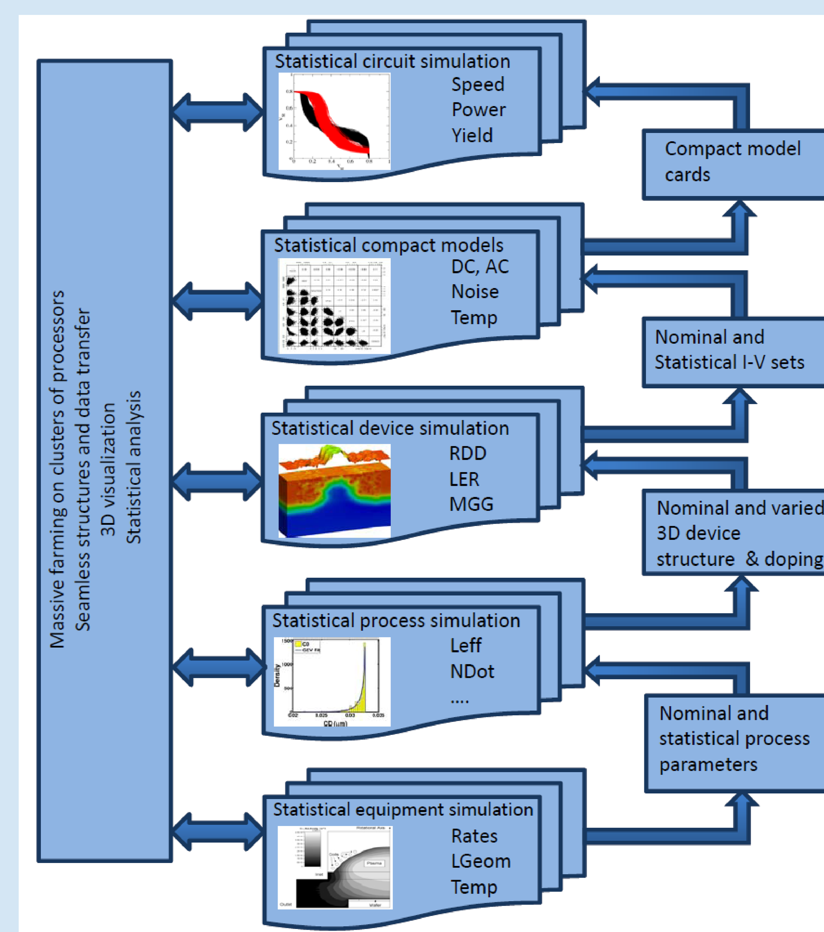


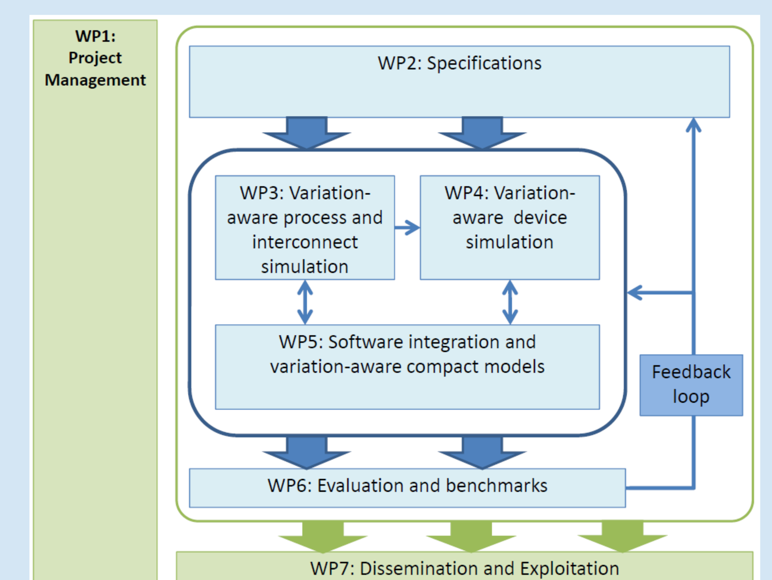
Device simulation including statistical variability, using GARAND (© GSS)



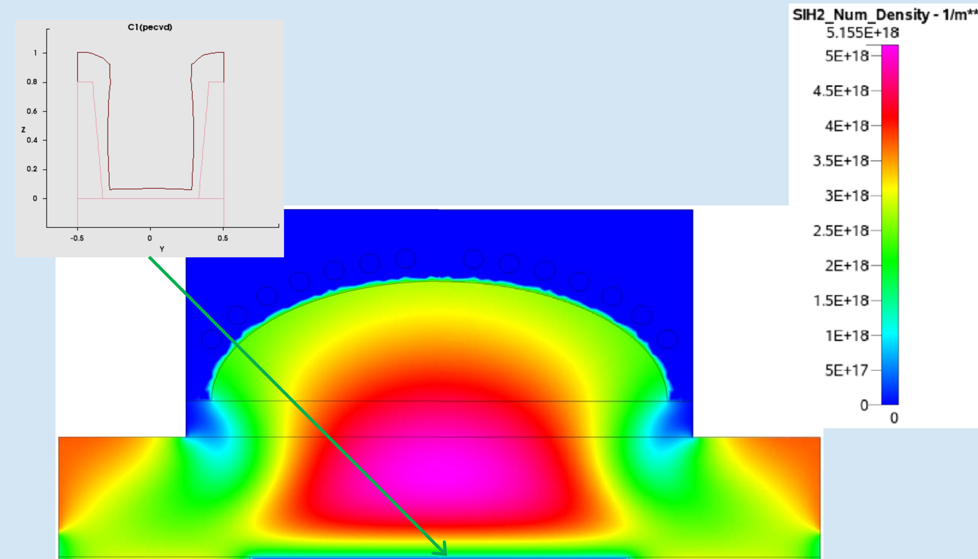
SUPERTHEME closes critical gaps between equipment and design (© Fraunhofer IISB)



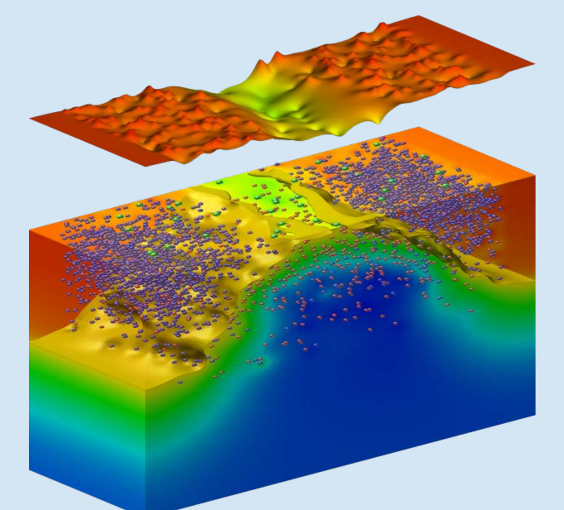
Levels of simulation being addressed by SUPERTHEME (© GU / Fraunhofer IISB)



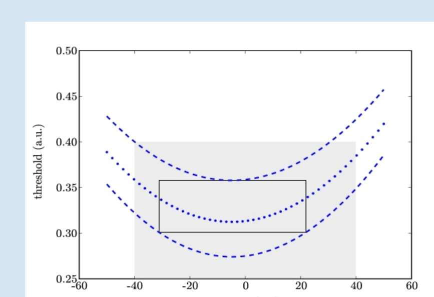
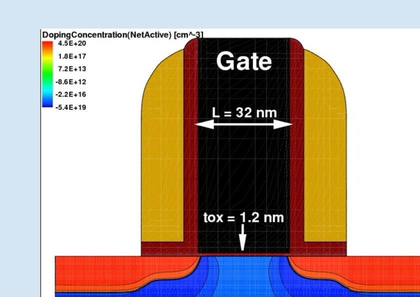
Structure of the SUPERTHEME project (© Fraunhofer IISB)

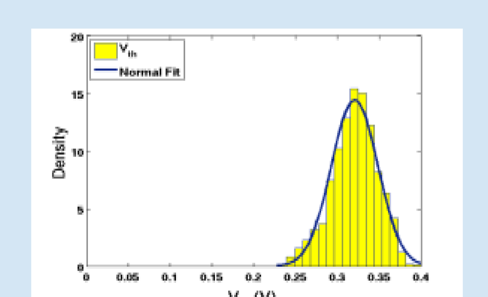
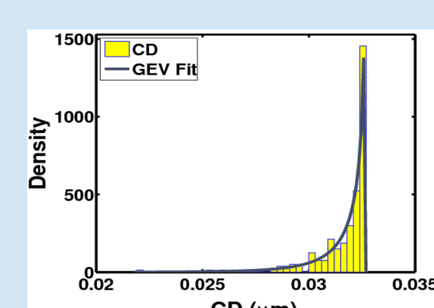


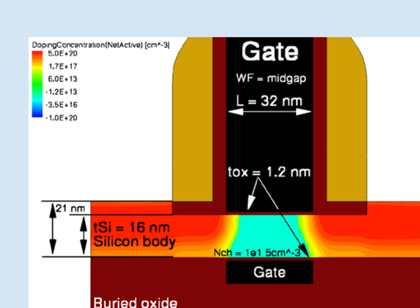
Simulated distribution of SiH_2 radicals and the layer profile in a contact hole in an ICP reactor for oxide PECVD (© Fraunhofer IISB)

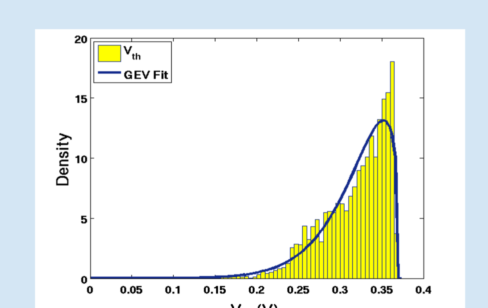


Simulation of a 45 nm technology transistor in the presence of discrete dopants, line edge roughness and poly-silicon gate granularity (© Univ. Glasgow)





Impact of lithography variations (defocus/dose – top left) on critical dimensions (CD – bottom left) for bulk (top) and FD double gate SOI (bottom) transistors (© Fraunhofer IISB)

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European Project SUPERTHEME – Examples

COUPLED SIMULATION ON EQUIPMENT- AND FEATURE-SCALE WITH LINK TO ELECTRICAL EXTRACTION

- Oxide deposition as part of a fabrication sequence for a Through-Silicon Via (TSV, **Figure 1**) is studied.
- A PECVD plasma reactor with TEOS / oxygen chemistry has been simulated with the software Quantemol Q-VT.
- For the wafer surface, the fluxes of ions and radicals have been extracted for various positions (**Figure 2**).
- These fluxes provide the boundary conditions for feature-scale simulation with the IISB inhouse tool DEP3D. As result, the profiles for different positions are obtained.
- Electrical simulation using COMSOL has been used to determine coupling capacitances for the various positions (**Figure 3**).

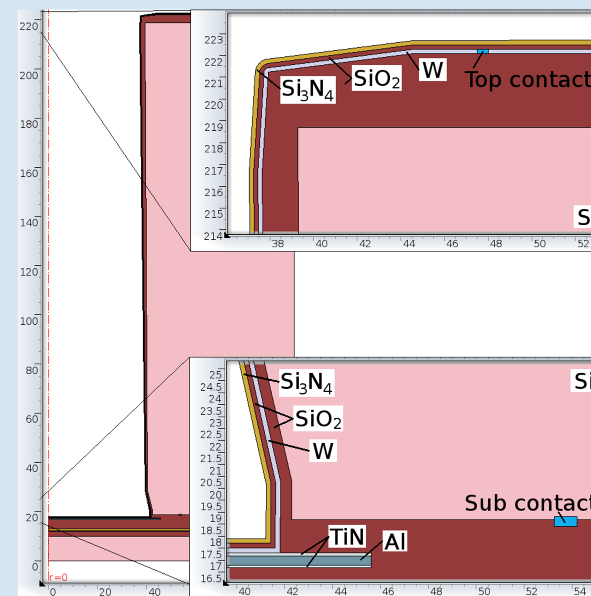

***Figure 1**: TSV structure (cross section). (© TU Vienna)*

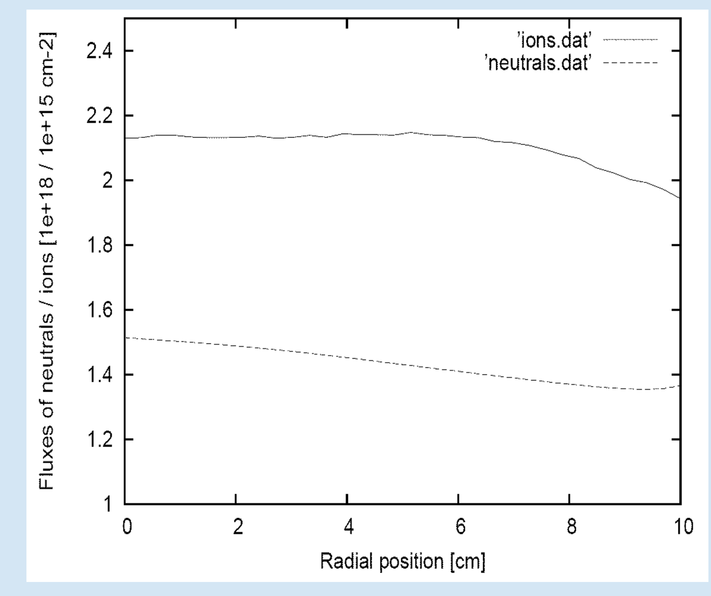

***Figure 2**:Simulated fluxes of oxygen neutrals (radicals) and O_2^+ ions at the substrate versus distance to the center axis for a PECVD reactor. (© Fraunhofer IISB)*

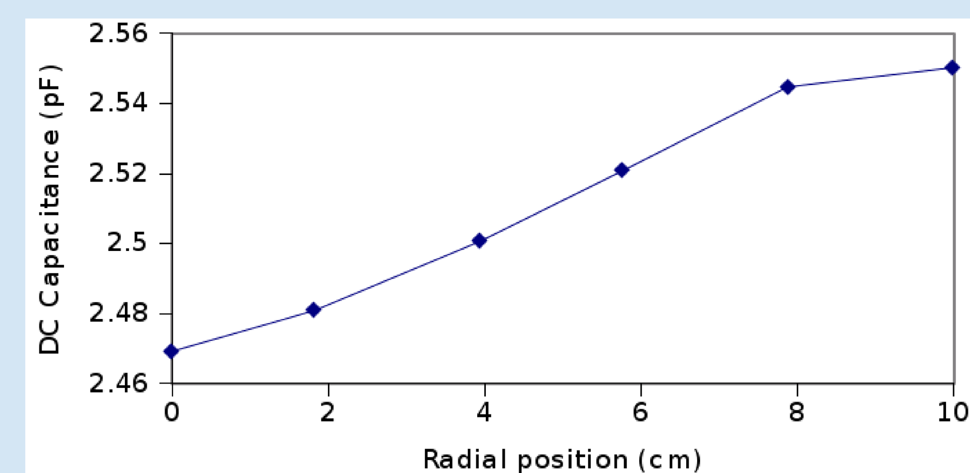

***Figure 3**: Simulated radial dependence (distance to center axis of PECVD reactor) of DC capacitance between the Top contact and the Sub contact from Fig. 1. (© TU Vienna)*

DOUBLE PATTERNING FOR ADVANCED CMOS TRANSISTORS: SIMULATING A VARIABILITY CHALLENGE

- Example: **SRAM circuit with 20 nm SOI MOSFETs**
- Small pitch size of the gate electrode lines requires double patterning (here LFLE) in photo-lithography.
- Layout of a fragment of the SRAM circuit (**Figure 4**).
- Transistors T1 to T6 (**Figure 4**) build one SRAM cell.
- The coupling of photo-lithography simulations and electrical simulations for the investigation of a 6T SRAM circuit generated with a LFLE double patterning process is demonstrated.
- Asymmetrical distributions of the performance parameters of SRAM (**Figure 5**) result from symmetrical variations of defocus and illumination dose threshold in the photo-lithography process .
- A rather long tail of the static noise margin distributions to smaller values of the READ and WRITE SNM is critical for SRAM performance.
- Mask splitting in LFLE critically affects variations.

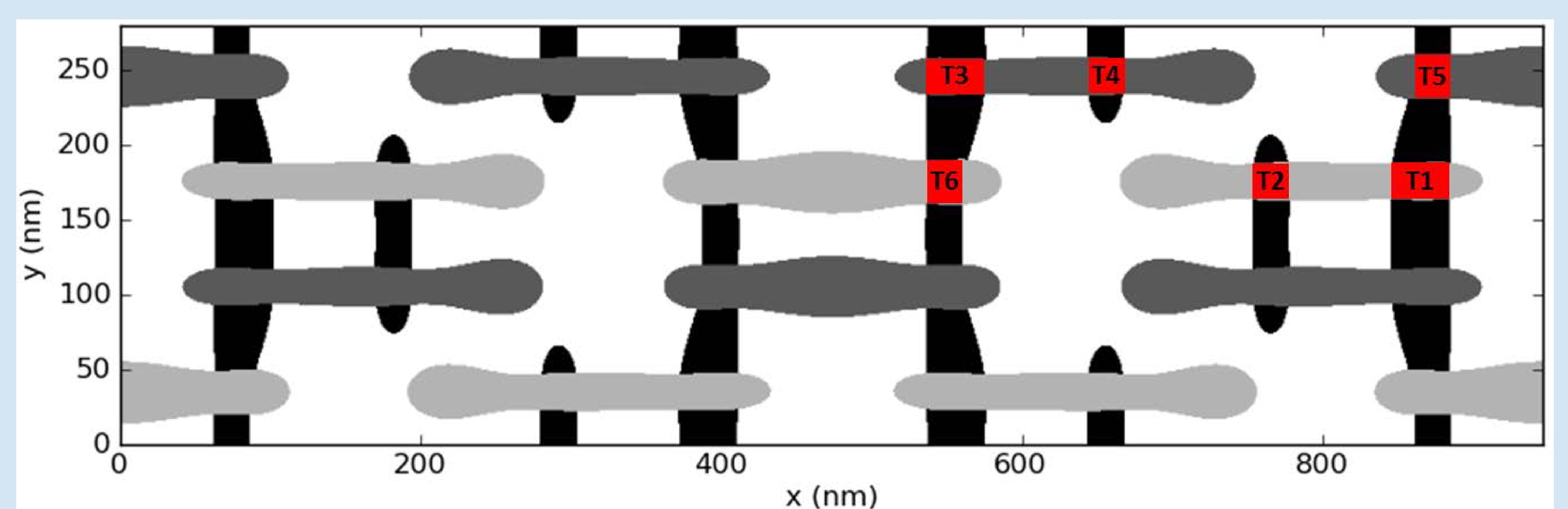

***Figure 4**: Simulated geometrical shape of the active regions (horizontal lines) and of the gate electrodes (vertical lines) in a SRAM circuit (© Fraunhofer IISB)*

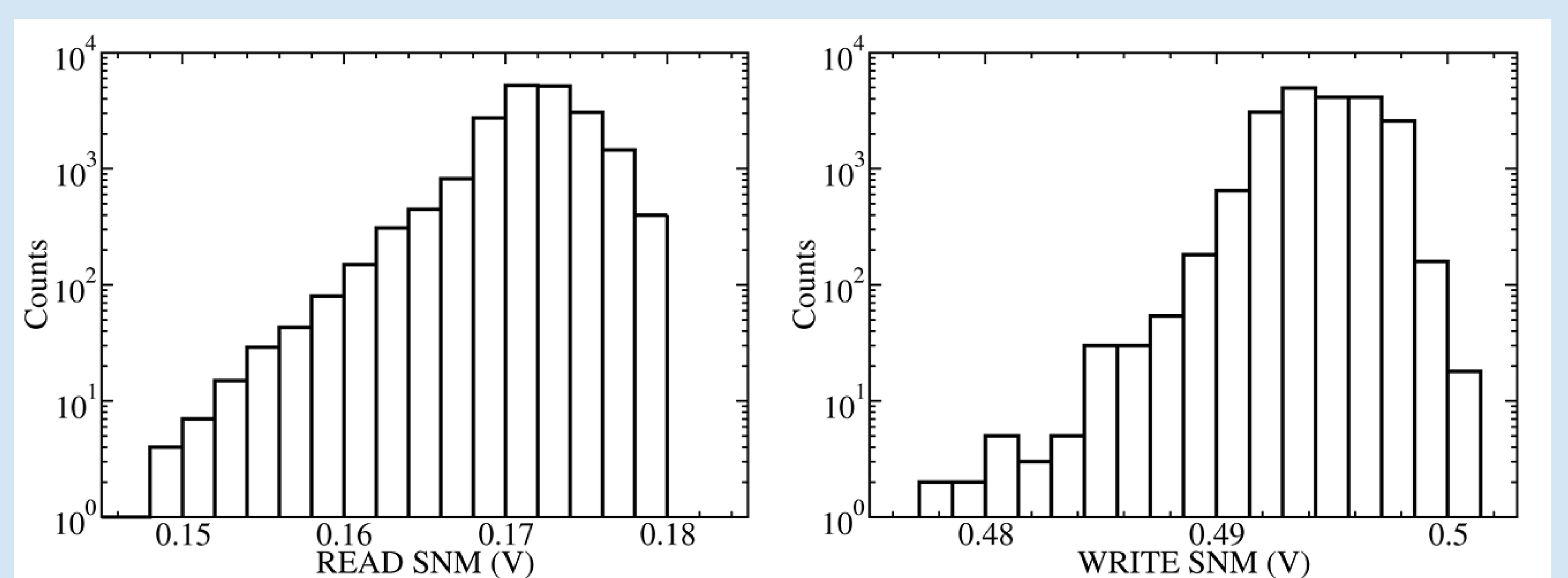

***Figure 5**: Electrical performance variability simulation of SRAM circuit: Statistical distribution of the READ static noise margin (left) and of the WRITE static noise margin (right) (© Fraunhofer IISB)*

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