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ESSCIRC ESSDERC 2015

VARIABILITY SIMULATION WITHIN SUPERTHEME

Covering variability from unit process up to circuit level for mixed-signal circuits

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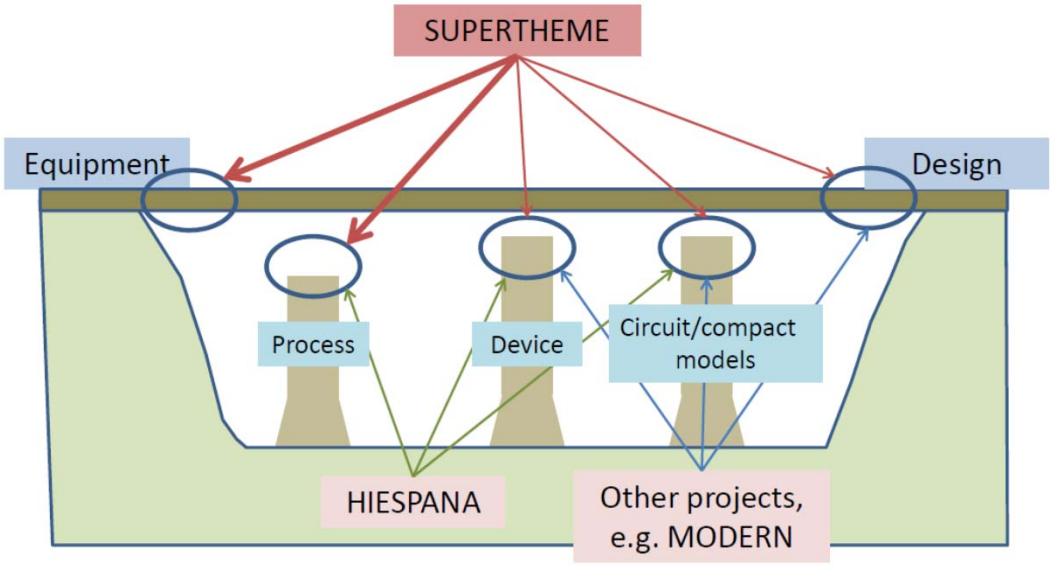
OUTLINE

1. Introduction: Multi-hierarchical simulation strategy for variability
2. Description of benchmarks and results
    1. System Level
    2. Circuit Level
    3. Circuit Element Level
    4. Process Level
3. Conclusions and Outlook

1

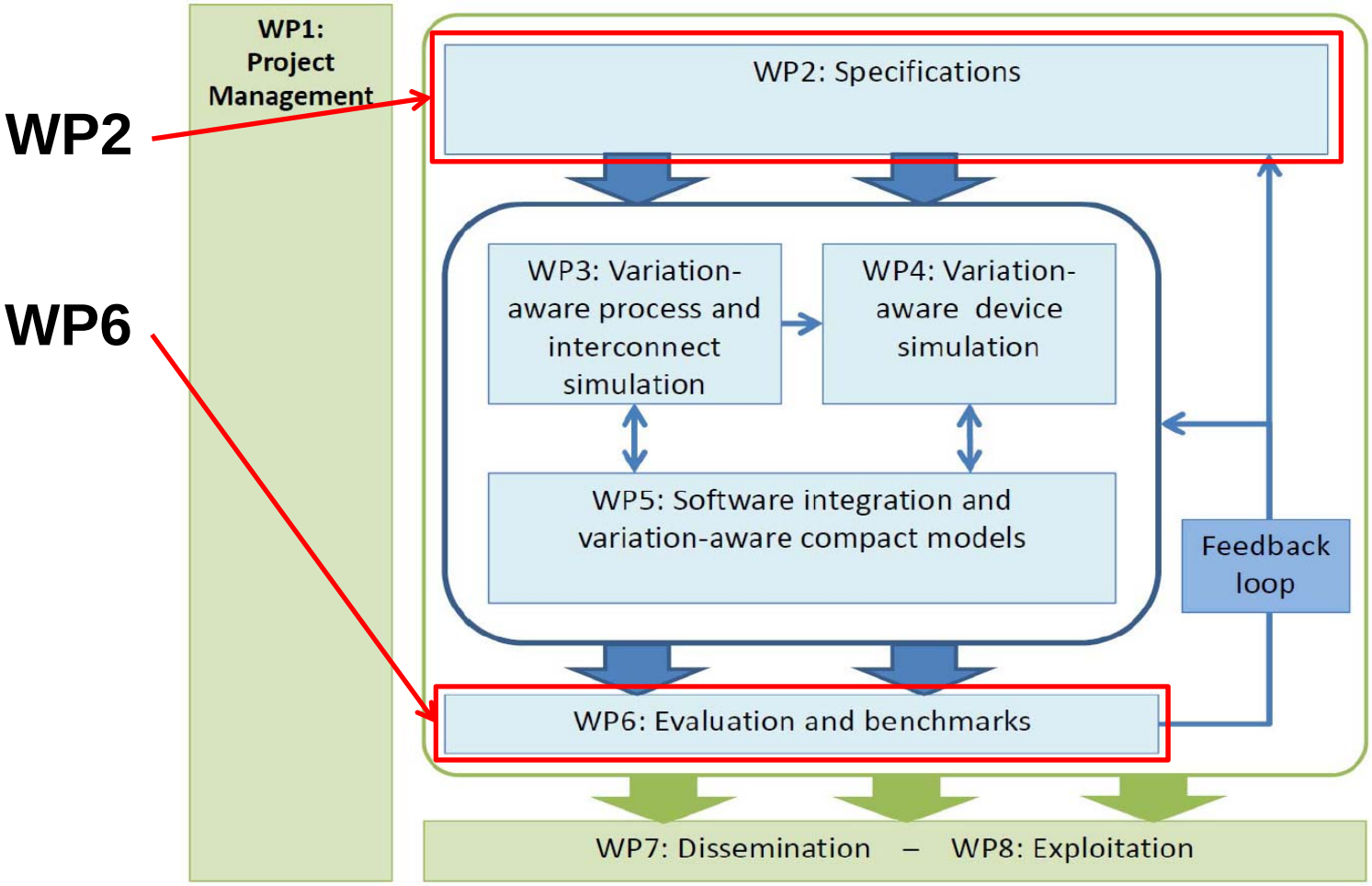
INTRODUCTION: MULTI-HIERARCHICAL SIMULATION STRATEGY FOR VARIABILITY

FROM EQUIPMENT TO DESIGN



- Use existing frameworks (especially HIESPANIA and MODERN) to finalize „bridge“ from Equipment to Design
- Take HPA(high performance analog) parameters as benchmarks to assess environment built up during project

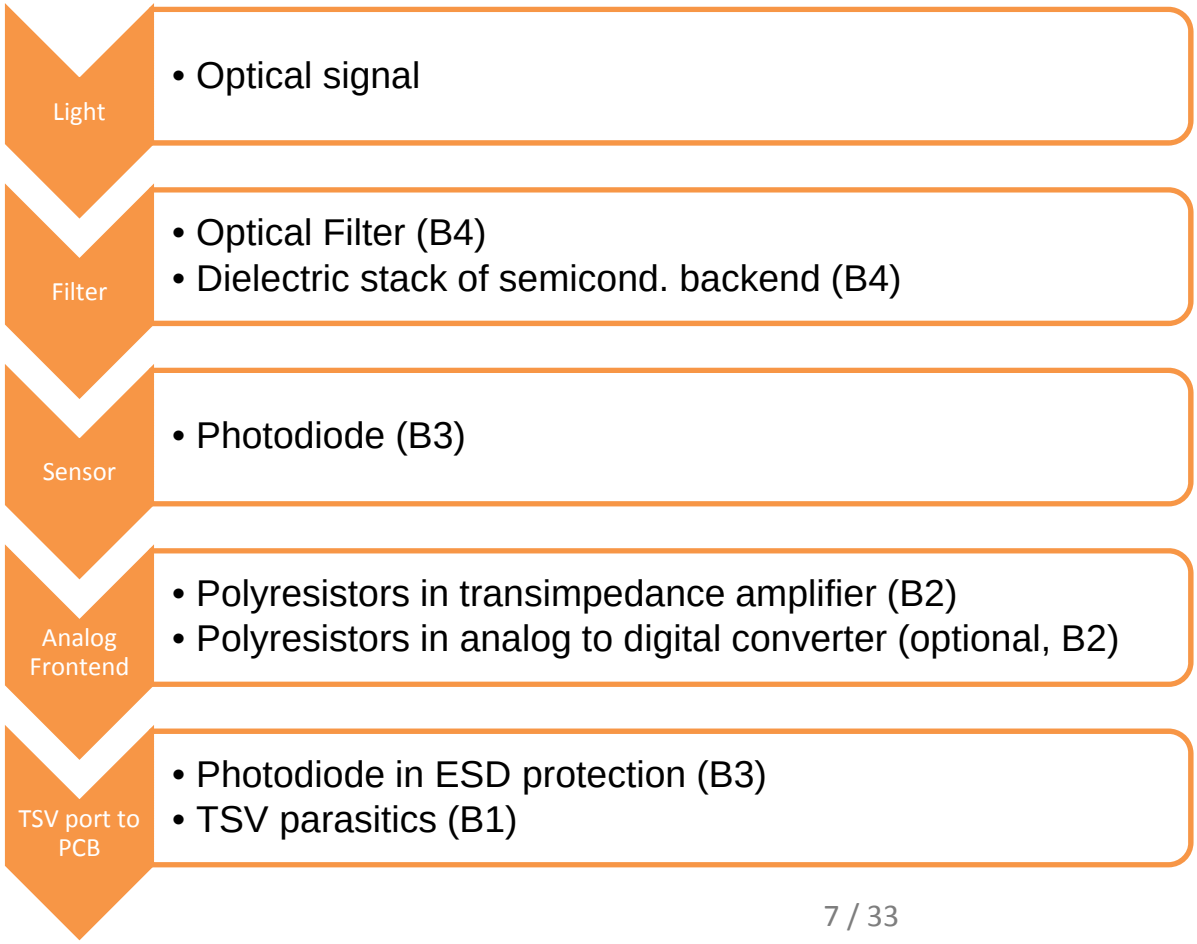
SUPERTHEME WORKPLAN CONTEXT



2

DESCRIPTION OF BENCHMARKS AND RESULTS

STRUCTURE OF BENCHMARK



- Classical SoC design
- Covers relevant analog area
- Highly relevant market for ams
- Complementary to More Moore ITRS
- Representative high performance analog benchmark

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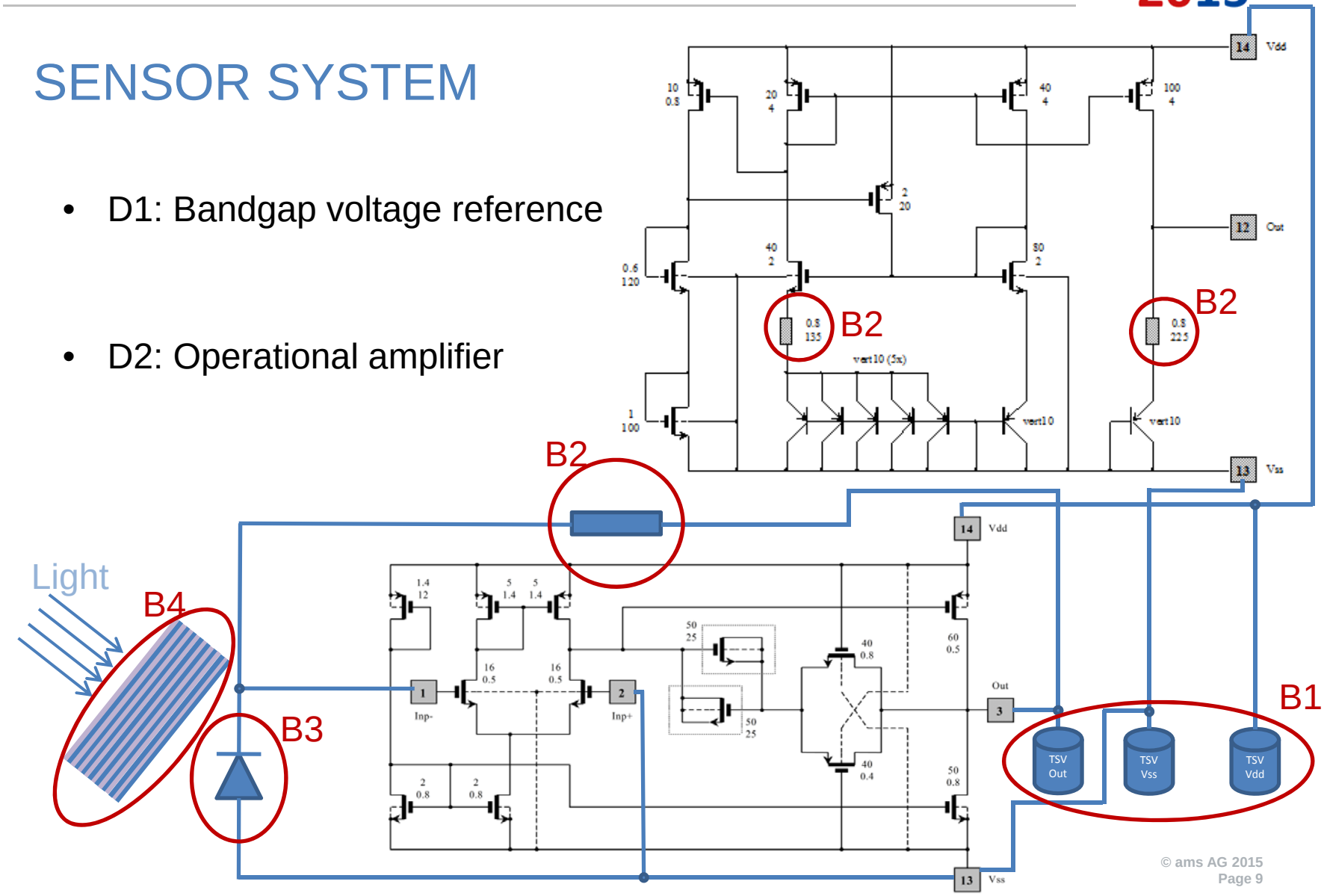
2.1

VARIABILITY ON SYSTEM LEVEL

SENSOR SYSTEM

- D1: Bandgap voltage reference
- D2: Operational amplifier



VARIABILITY SOURCES

Label	Benchmark	Expected output	Relevant simulation features before device simulation
B1	Electrical performance and reliability of Through Silicon Vias (TSVs)	Variability of R/C and max. current density	Shape of TSV etch / shape of isolation deposition / shape of conductor deposition / electrical conductor properties
B2	Electrical performance of polycrystalline silicon resistors	Variability and matching of sheet resistance	Polysilicon morphology (grain size/grain shape/resistor shape) / doping distribution incl. segregation
B3	Electrical performance of junction diodes	Variability of blocking voltage and optical sensitivity	Doping distribution within device / contacts position and shape
B4	Optical performance of dielectric stacks	Variability and roughness of stack layers	Layer roughness / layer thickness / layer composition

- Selection of benchmark components
- Covers broad range of analog design components
- Good balance btw. relevance and complexity
- Representative demonstrators for other analog applications

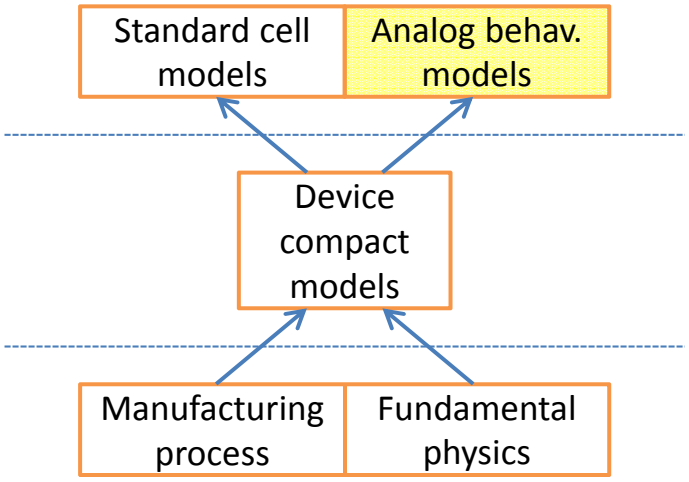
2.2

VARIABILITY ON CIRCUIT LEVEL

IP-BLOCK BENCHMARK D1 AND D2

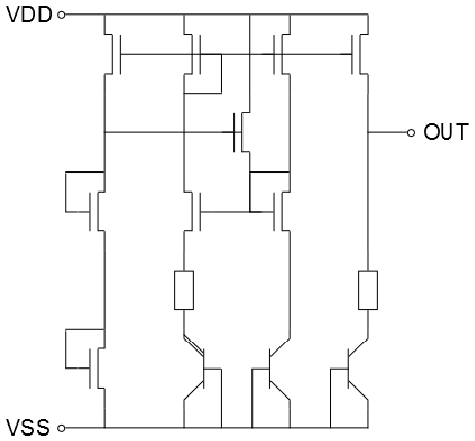
Motivation and Goals

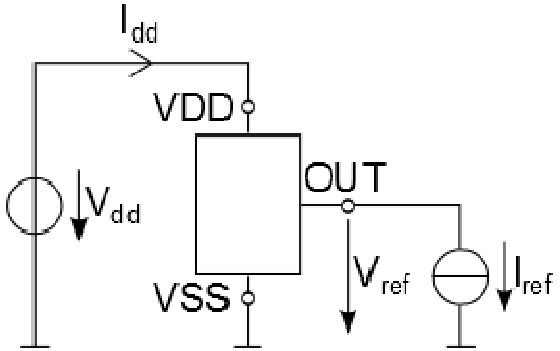
- Simulation of benchmark SoC circuit and comparison with measurement data
  - B1 – B4 as well as D1 and D2
- Use of SUPERTHEME results in circuit design
  - Transfer of variability information from process variations and atomic-level random fluctuations to higher levels of abstraction
    - Digital design: standard cells
    - Analog design: analog sub-blocks
- Model requirements
  - Gaussian and non-Gaussian distributions
  - Arbitrary correlations



D1: BANDGAP VOLTAGE REFERENCE

Basics





- Behavioral model

$$V_{ref}{}^{*} = A_1 + A_2 V_{dd}{}^{*} + A_3 T^{*} + A_4 (T^{*})^{2^{*}} + A_5 I_{ref}{}^{*} + A_6 V_{dd}{}^{*} T^{*}$$

$$I_{dd}{}^{*} = A_7 + A_8 V_{dd}{}^{*} + A_9 T^{*} + A_{10} (T^{*})^{2}$$

with

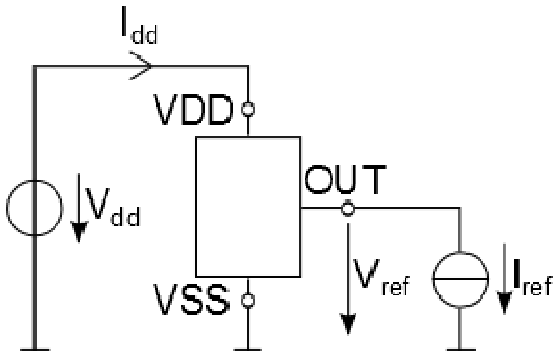
$$V_{ref}{}^{*} = \frac{V_{ref} - V_{ref,0}}{V_{ref,0}},\ V_{dd}{}^{*} = \frac{V_{dd} - V_{dd,0}}{V_{dd,0}},\ T^{*} = \frac{T - T_0}{T_0},\ I_{ref}{}^{*} = \frac{I_{ref} - I_{ref,0}}{I_{ref,0}},$$

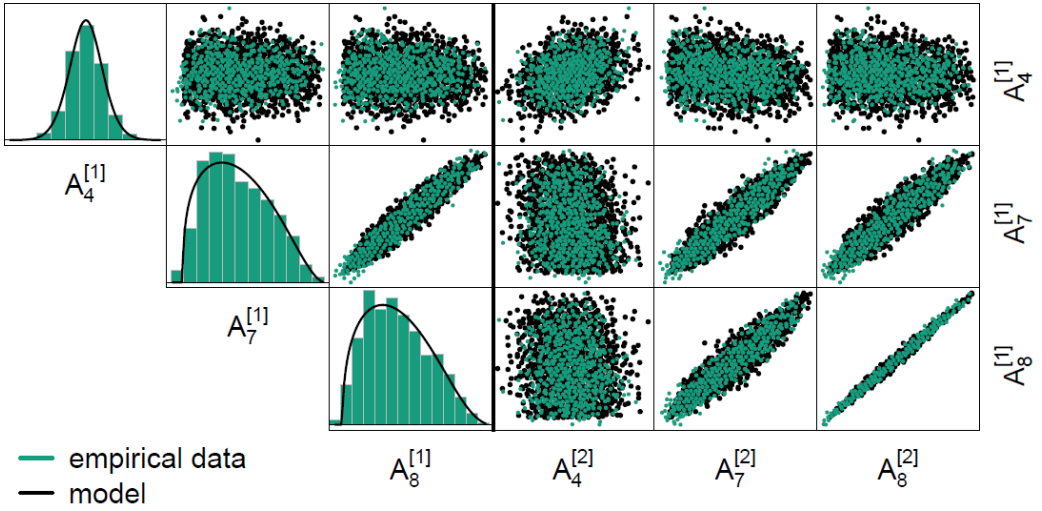
$$I_{dd}{}^{*} = \frac{I_{dd} - I_{dd,0}}{I_{dd,0}}$$

D1: BANDGAP VOLTAGE REFERENCE

Variation-Aware Behavioral Model

- Model calibration: coefficients $A_1 \ldots A_{10}$ determined from circuit simulations varying V_{dd}, T, and I_{ref}
- Variation-aware model characterization: repetition of model calibration for MC samples of process parameters
- Variation-aware behavioral model: 10-dimensional random variable **A**

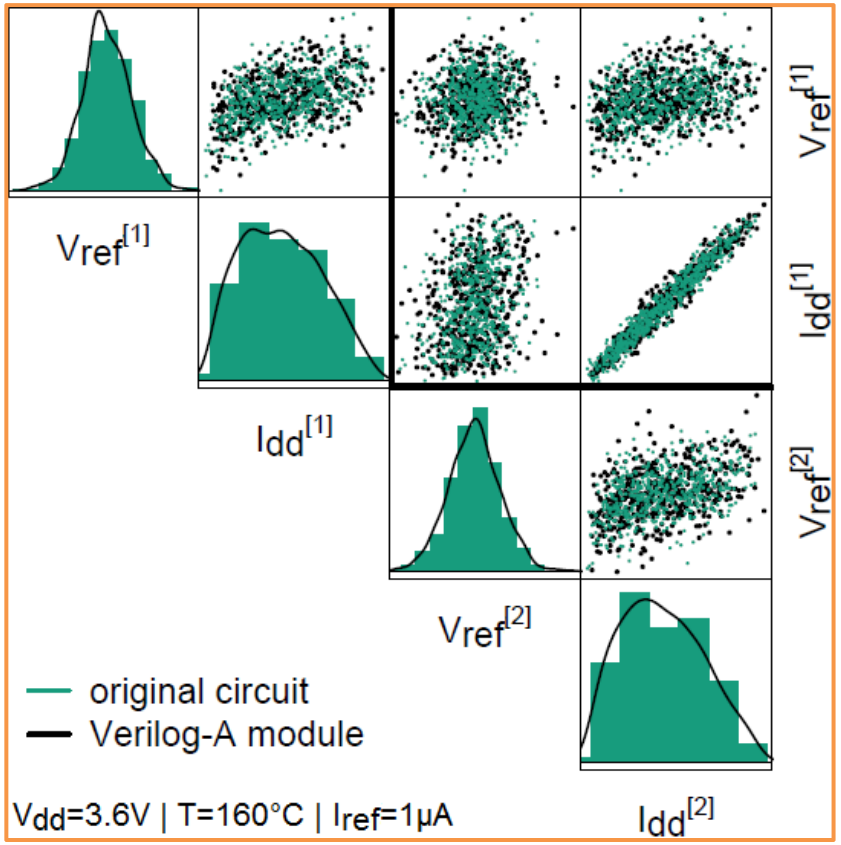




D1: BANDGAP VOLTAGE REFERENCE

Validation

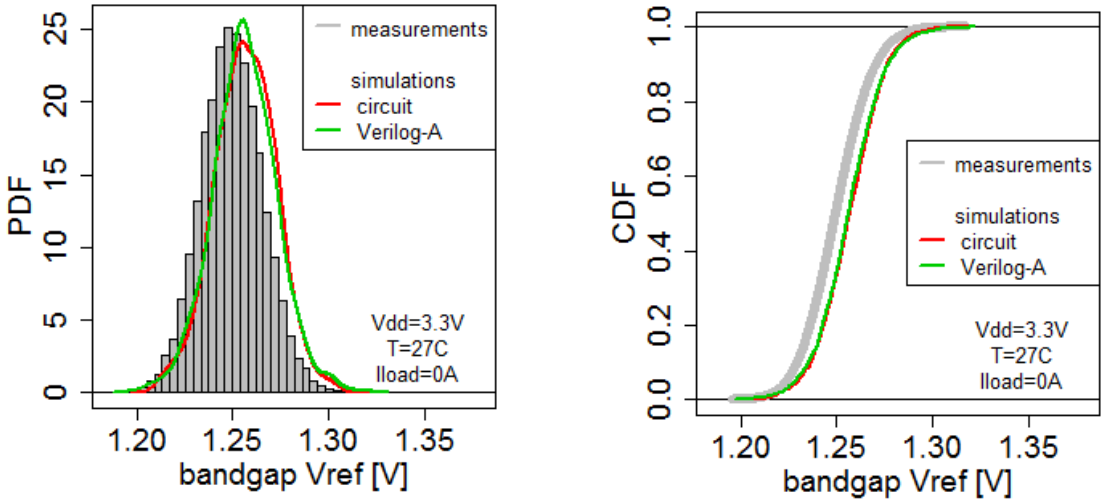
- Comparison of circuit simulations and Verilog-A model evaluations for various combinations of V_{dd}, T, and I_{ref}
  - No significant differences between circuit representations
  - No significant differences between bandgap instances
  - 4X speed-up with Verilog-A model (7.2s instead of 33s for 500 samples)



D1: BANDGAP VOLTAGE REFERENCE

Measurements vs Simulations

- Comparison of ams measurement results and simulations



- 0.5% mean shift
- Standard deviations practically identical

D1 AND D2

Variability sources

Benchmarks B1 to B4 Empirical models vs. equipment parameters:

- R_{TSV}, C_{TSV}
- $R_{polysilicon}$
- BV_{diode}, C_{diode}, Responsivity
- Filter variability

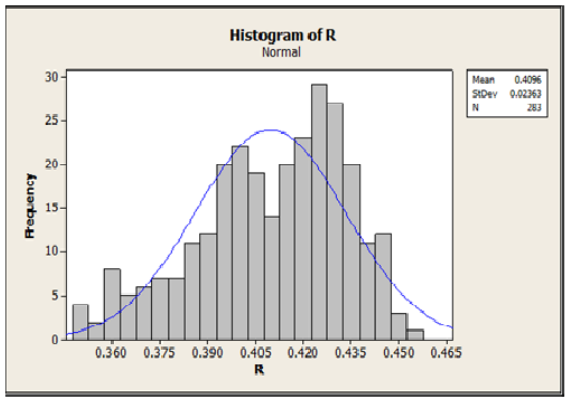
Simulation level

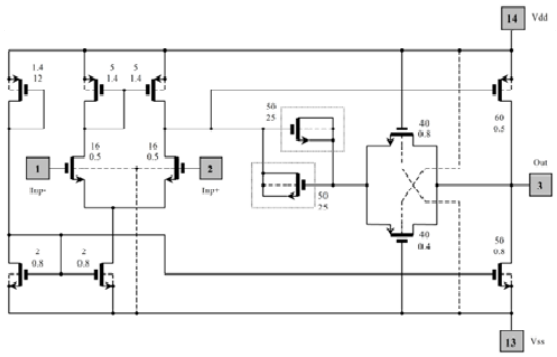
Empirical model included into Monte Carlo Spice simulation Analog Benchmarks D1, D2

Analysis

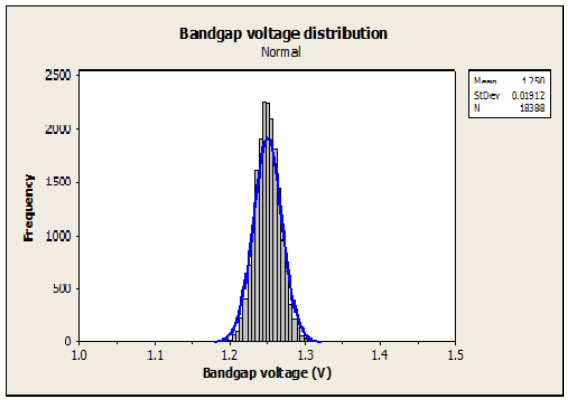
Sensitivity analysis of B1-B4 benchmarks on electrical parameters output of analog circuits D1 – D2

Comparison to electrical measurement distribution of electrical output





D1: Bandgap voltage reference



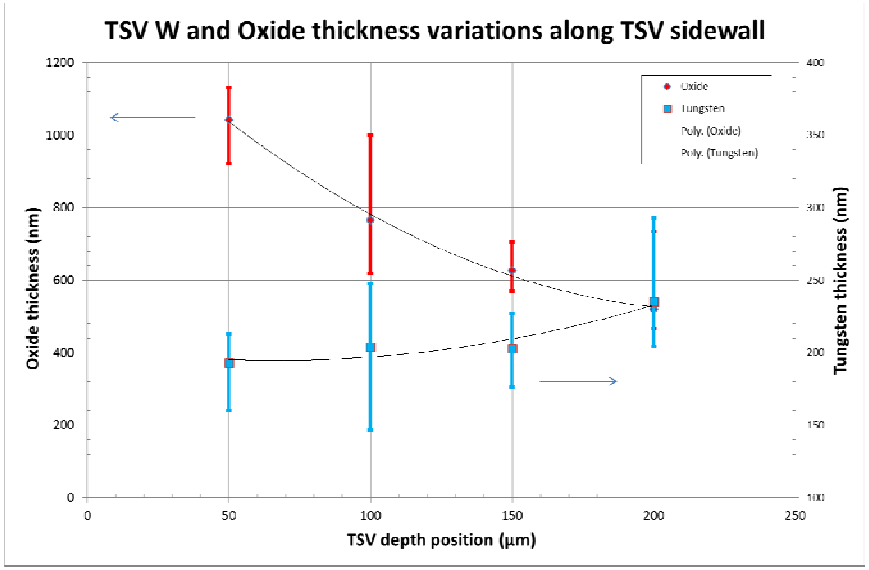
2.3

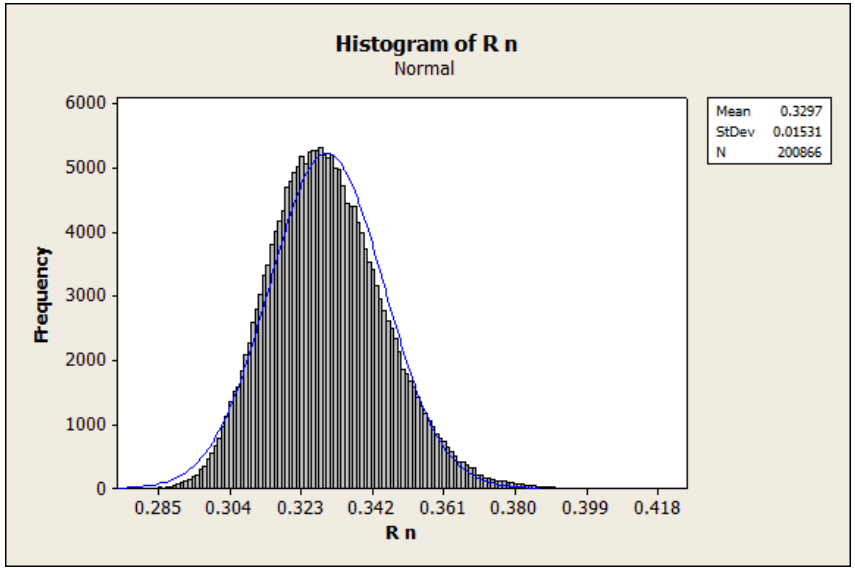
VARIABILITY ON CIRCUIT ELEMENT LEVEL

BENCHMARK B1

TSV processing

TSV resistance variation modelled vs. oxide and tungsten thickness variability observed in TEM images.





BENCHMARK B2

Polycrystalline resistor

Variability sources

Furnace temperature gradient
Grain size statistical distribution

Simulation level

3D Grain structure is converted into netlist by adding additional nodes: Volume Centroid and Face Centroid

Electrical Structure is assumed to consist of Grain interior and Grain boundaries

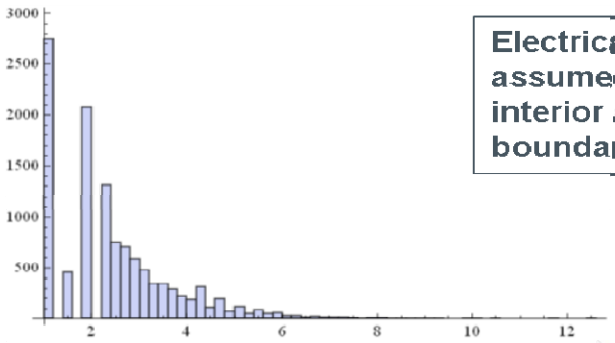
Responses surface modelling

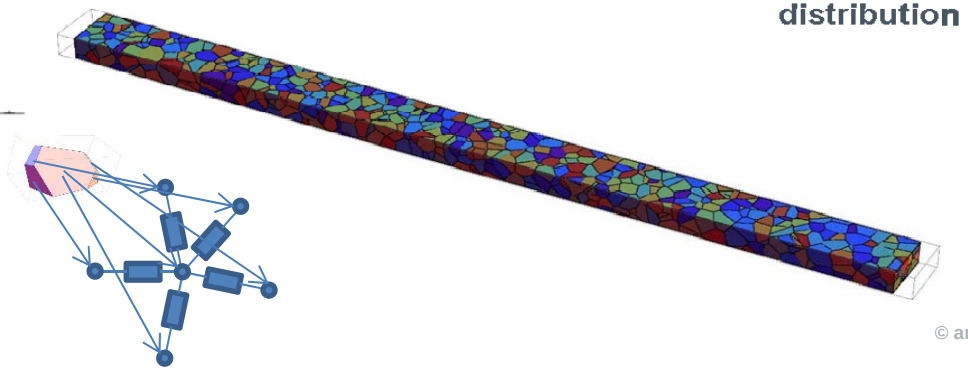
R

Analysis

Global sensitivity analysis on grain size

Comparison to poly-silicon resistance distribution

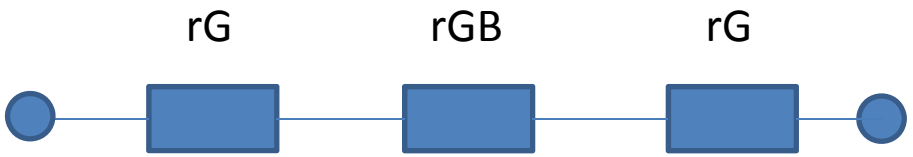


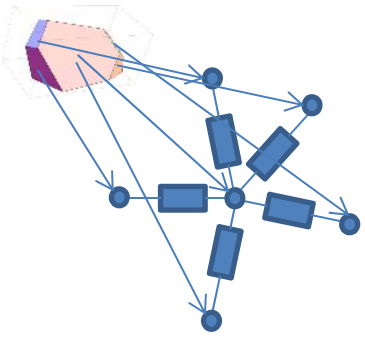


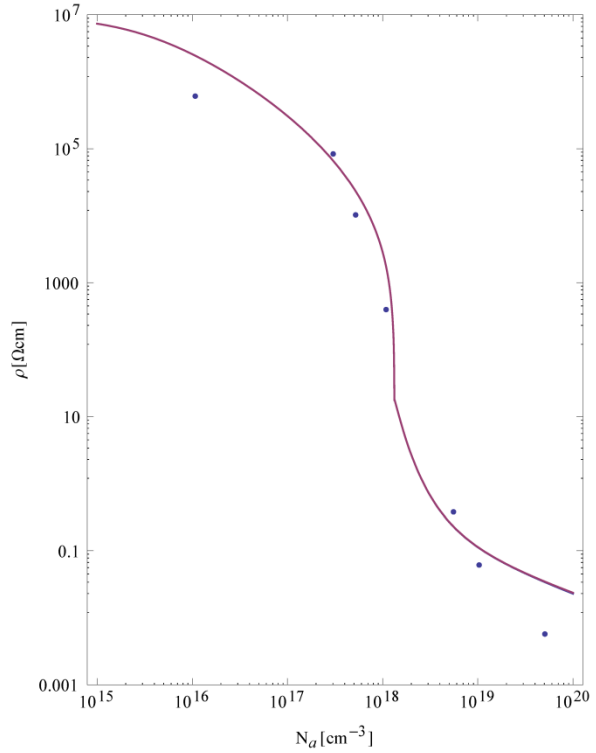
BENCHMARK B2

Polycrystalline resistor

- Further replace connection nodes at grain faces by additional resistor rGB
- Model rG with single crystal properties and rGB with amorphous material properties (Mott formalism, Khondker Model)
- Comparison to data collected on shortloops



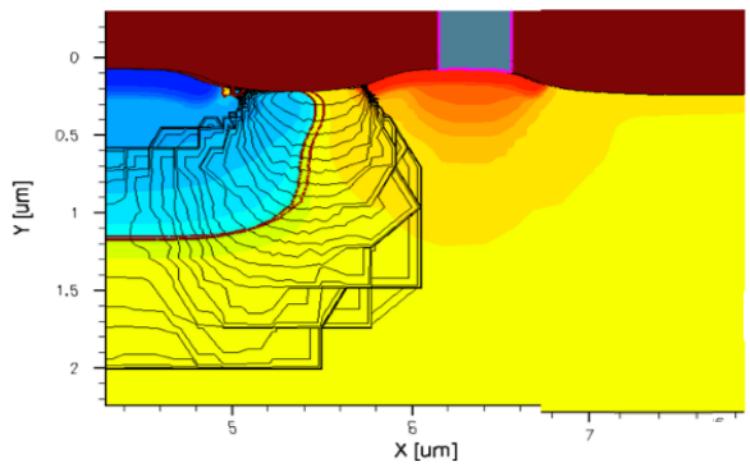


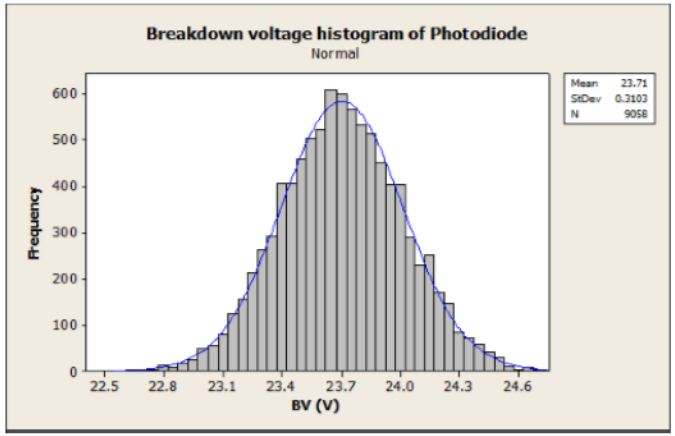


BENCHMARK B3

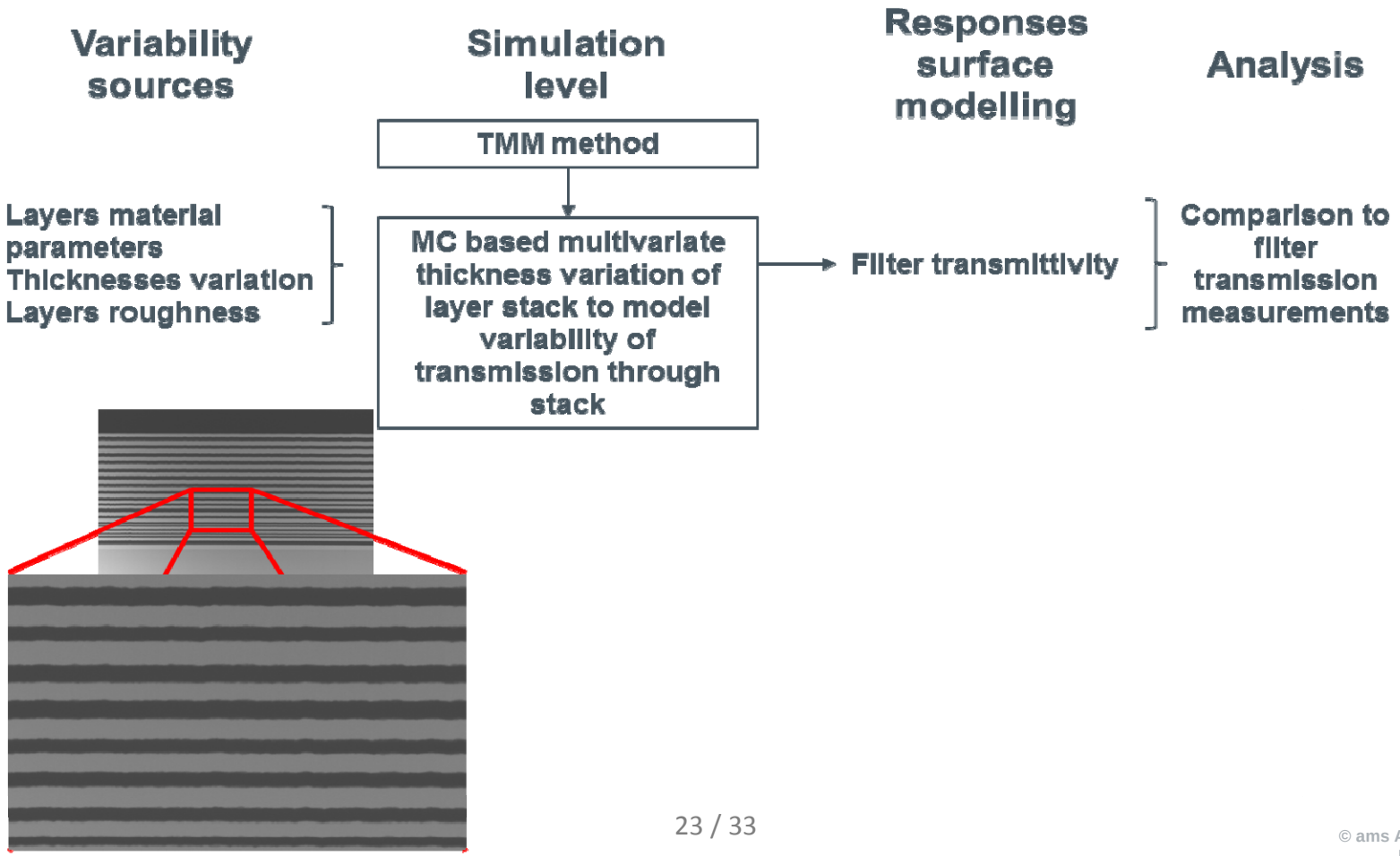
Photodiode & Reference diode

Variability sources	Simulation level	Responses surface modelling	Analysis
CD variation Implantation condition variation Oxide thicknesses	Synopsys TCAD Process, device Optical TMM simulation	BV Capacitance Optical responsivity	Comparison to online measurement of BV, C



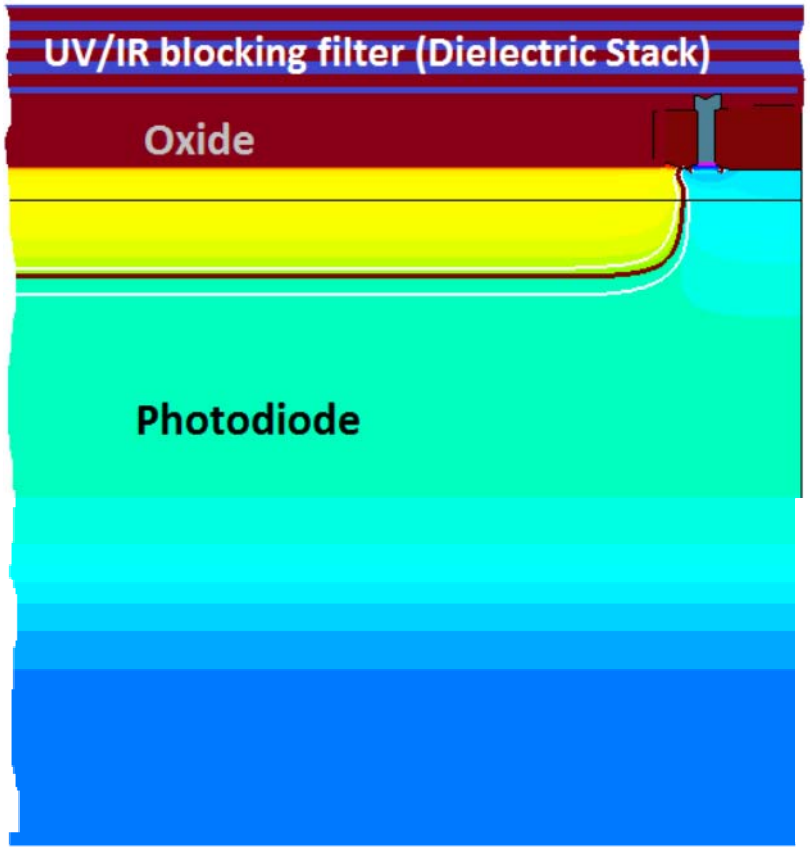


BENCHMARK B4



BENCHMARK B3 AND B4: PHOTODIODE + FILTER

UV/IR blocking filter + Photodiode



- 1. Dielectric thickness vs. transmission
  (1D TMM simulation with Mathematica)
- 2. Filter stack equipment simulation (DEP3D)
- 3. Filter + photodiode simulation
  (1D TMM simulations with TCAD)
- 4. Process variability: CD, overlay, implant dose/energy,Oxide thickness, substrate, epi-thickness
- 5. Investigation:
  - Photodiode: “Process variability” vs “Responsivity, Blocking voltage”
  - Filter + photodiode: responsivity

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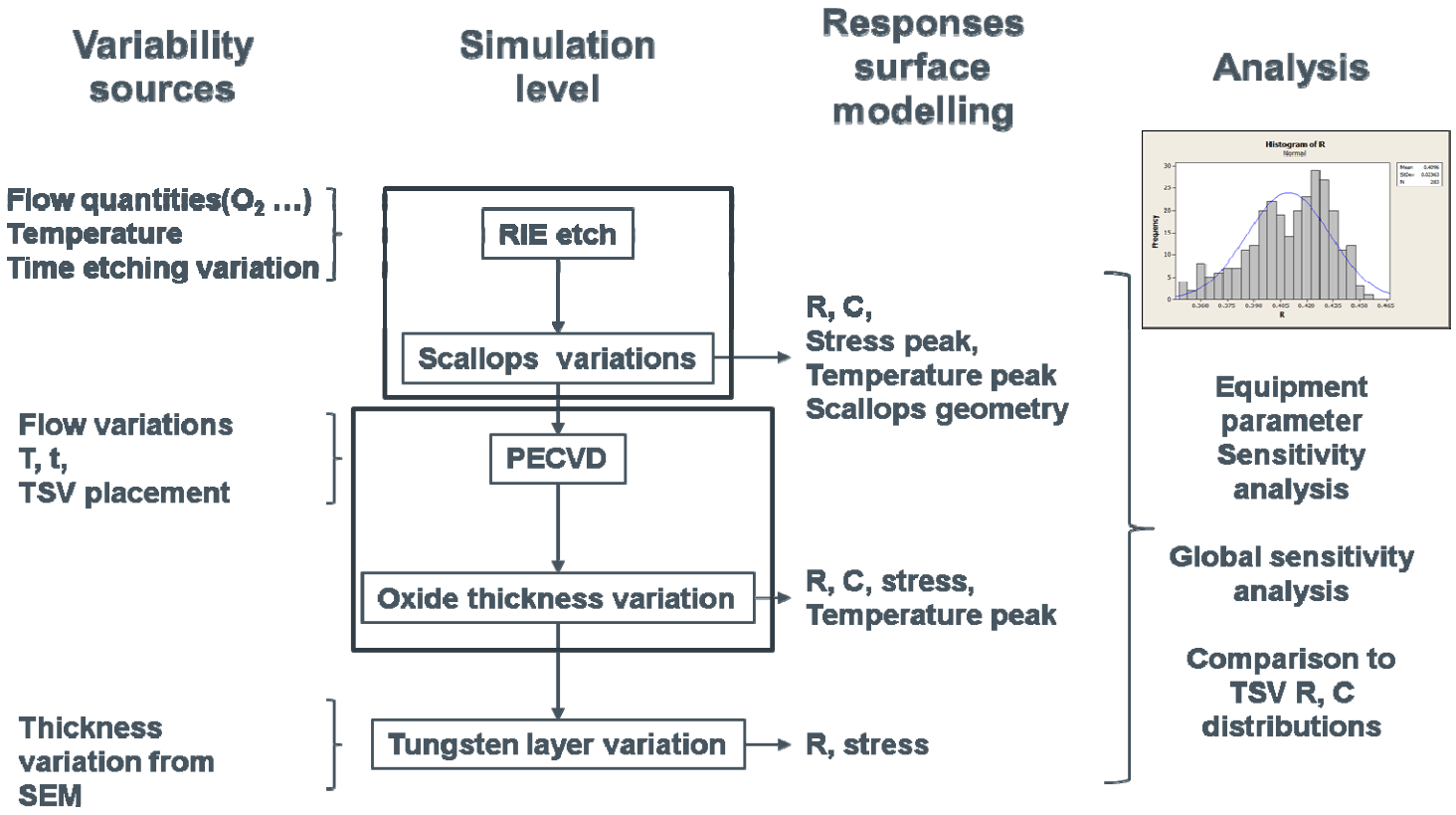
2.4

VARIABILITY ON PROCESS LEVEL

VARIABILITY GENERAL APPROACH

- Relation between variability sources and physical parameters of interest

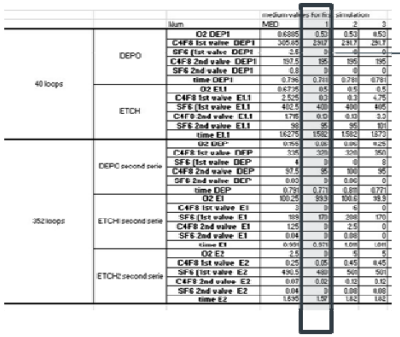


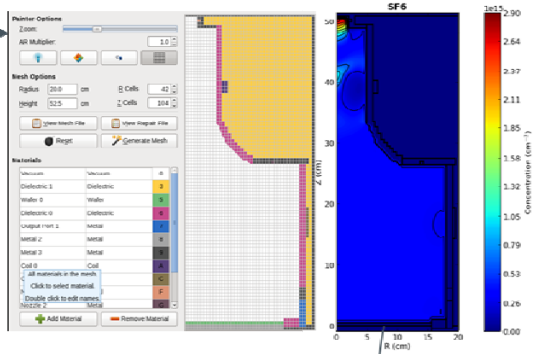
Final result will provide R, C, stress function of equipment/process parameters

VARIABILITY GENERAL APPROACH

Simulation loop up to scallops

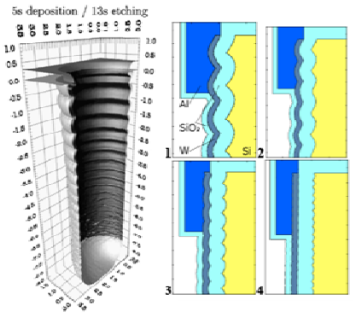
Parameters extraction from ams measurement

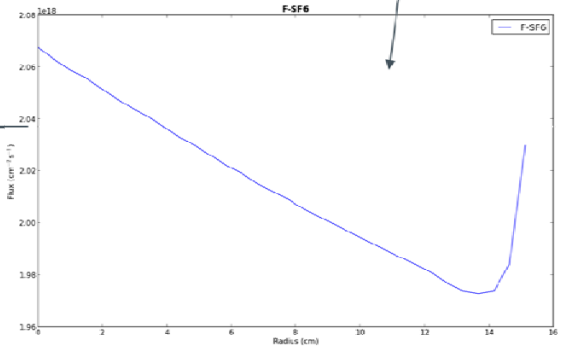




Species distribution in chamber during one sequence of DRIE process

Etching simulation at a wafer position 2D, 3D analytical/MonteCarlo

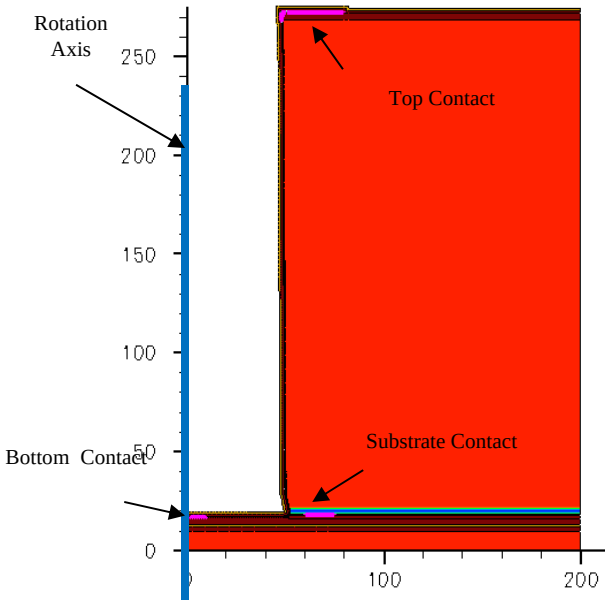


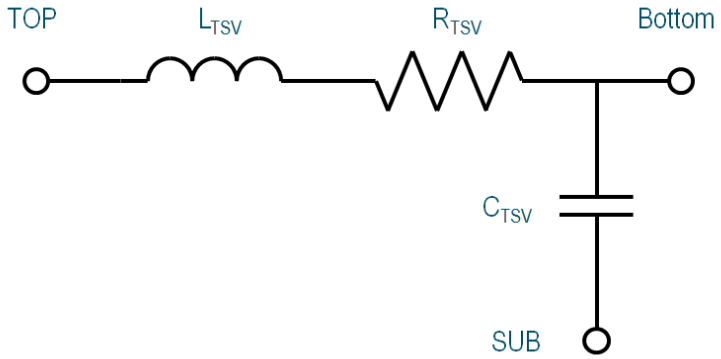


SF6 distribution on wafer surface at one sequence loop

TSV ELECTRICAL CIRCUIT

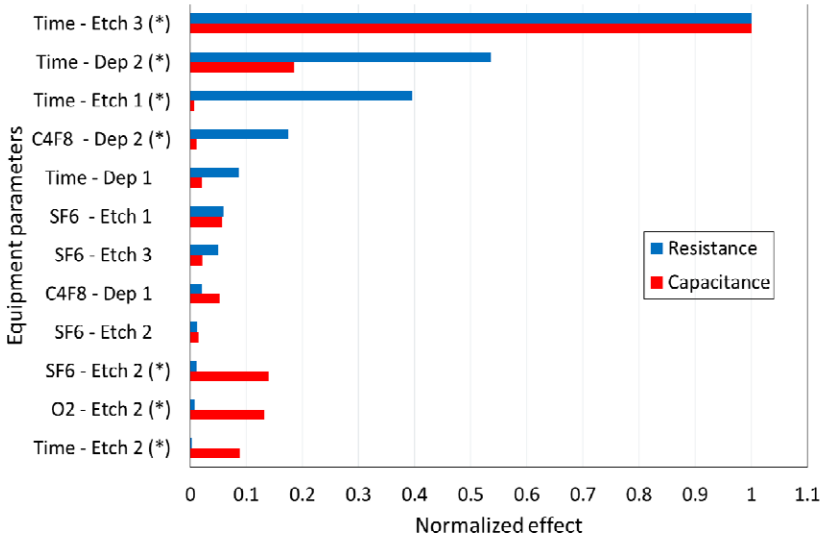
- TSV can be described as a RCL circuit (including S-parameters in a quadripole model)
- Typical values in the GHz frequency range: LTSV=12pH, RTSV=0.35Ohm, CTSV=3.4pF
- Resistance and Capacitance can be measured but inductance is impossible





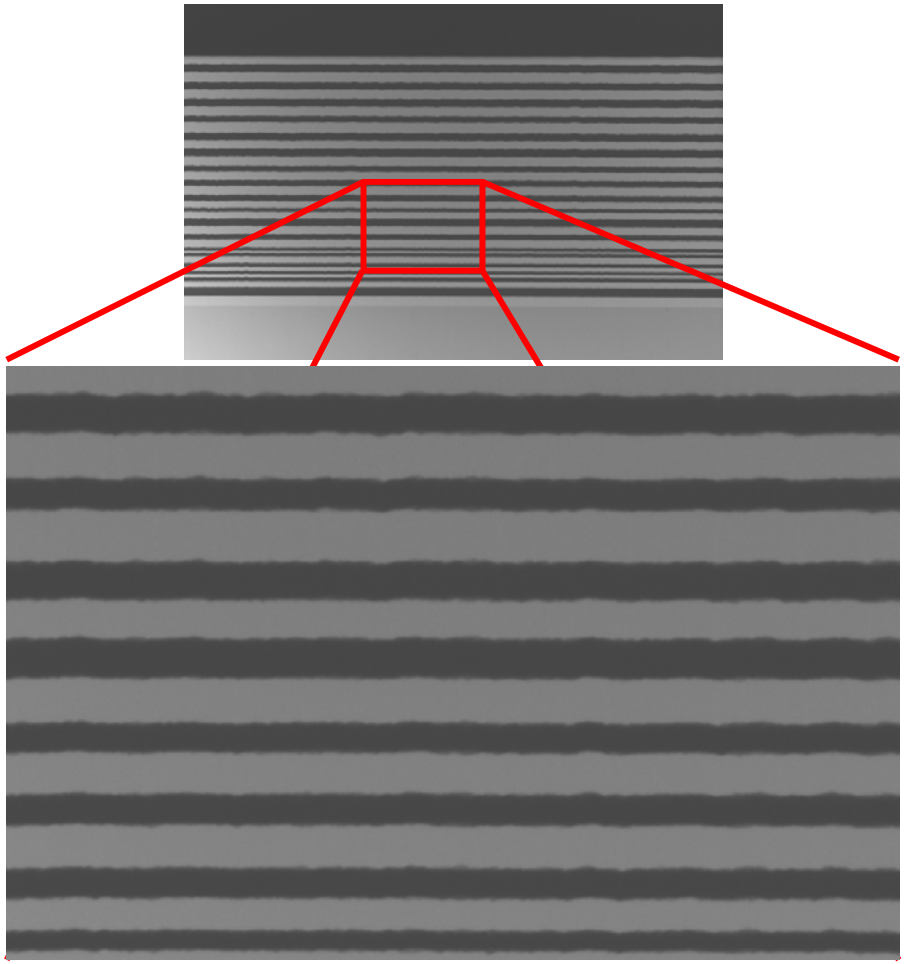
RESULTS

- **Pareto graph** of relevant equipment parameters on **resistance and capacitance response**
- Resistance and capacitance are very sensitive to the second stage etch-dep cycle (Large scallops cycle)
- Morphological variations (scallops width and height) **do not generate** large R,C, L and stress variations. Therefore, variations on TSV electrical and mechanical properties must have another source. (e.g. oxide and tungsten deposition)



	% Variation		% Variation
Large scallops width	9.64%	**R (mOhm)**	1.08%
Large scallops depth	10.34%	**C (pF)**	0.70%
Small scallops width	28.89%	**L (pH)**	1.20%
Small scallops depth	32.58%	**Average stress (MPa)**	3.04%

BENCHMARK B4

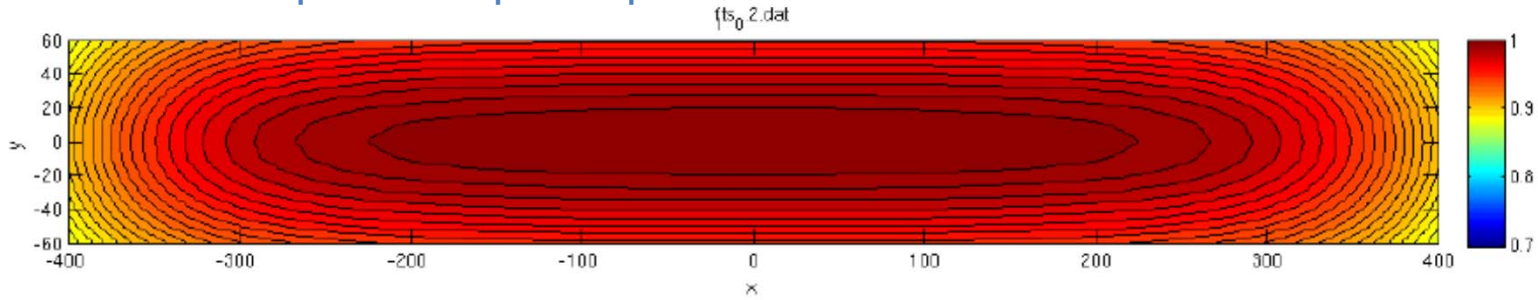


- Variability of interference filters and dielectric stacks
  - Overall system to model transmittivity by TMM method available.
  - MC based multivariate thickness variation of layer stack to model variability of transmission through stack has been implemented.
  - Furthermore the effect of layer roughness on transmittivity variation has been included into the benchmark

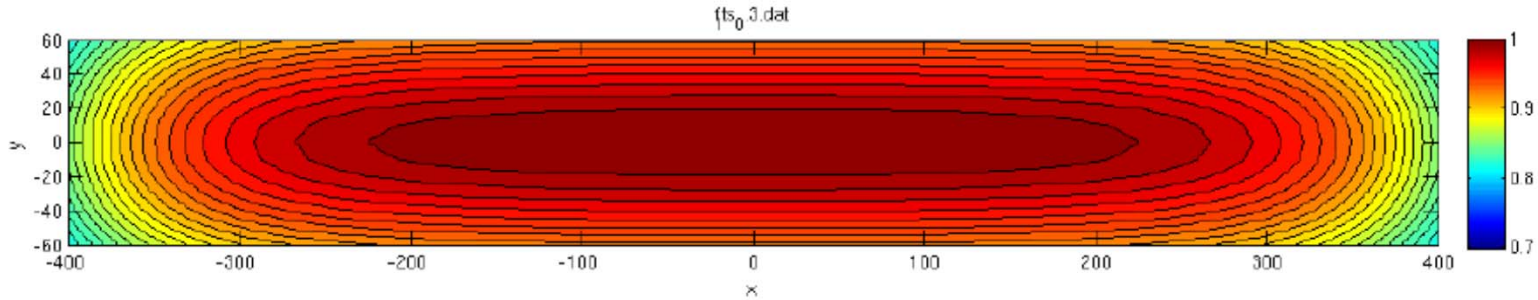
BENCHMARK B4

Dielectric Filter Sputter Dep.: Maps of relative thickness on substrate

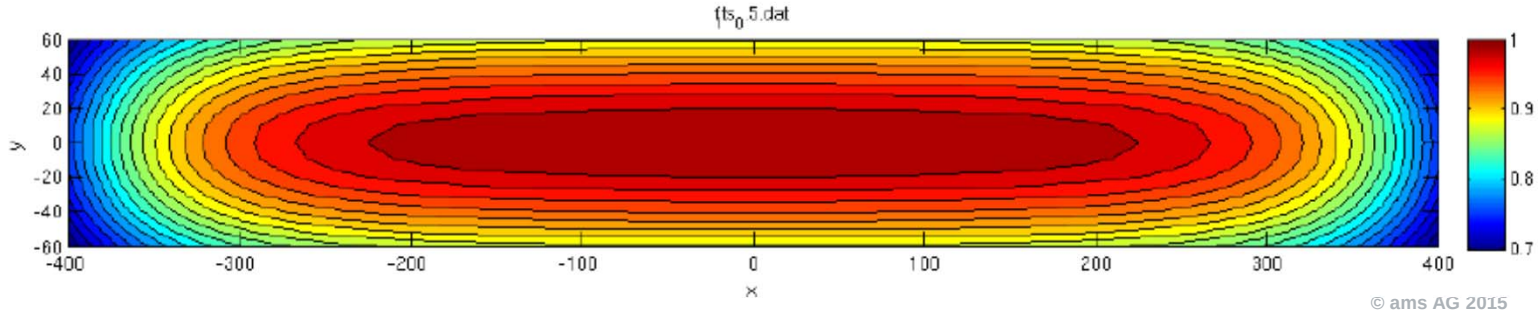
f_lts = 0.2



f_lts = 0.3



f_lts = 0.5



3

CONCLUSIONS AND OUTLOOK

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CONCLUSIONS & OUTLOOK

- A multi-hierarchical simulation system to model the variability behavior of high-performance analog circuits has been shown
- The vertical integration of multiple levels (process, device, circuit, system) enables optimization of key sources of variability
- The established causalities between system behavior and underlying processing variability will enable new much higher optimized integrated systems in future.

ams