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ESSCIRC ESSDERC 2015

OVERVIEW OF THE SUPERTHEME PROJECT

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OUTLINE

1. Introduction
2. Background pillars: Process and device
3. Consortium and project data
4. Project structure
5. Methodology used
6. Example: 23.5 nm transistor
7. Conclusion

INTRODUCTION: VARIATIONS

- Many variations have their source at equipment level

  ⇒ Equipment and process simulation core parts of the project

- Examples for variations at equipment level:
  - Lithography: Defocus; dose variations; (mis-)alignment, …
  - Etching/deposition: Inhomogeneities of gas flow, temperature; drifts, chamber coating; source characteristics, …
  - Ion implantation: Variations of angle(s) and dose; statistics, …
  - Annealing: Temperature variations in space/time, …
- Additional pattern-induced variations

INTRODUCTION: VARIATIONS

- Challenge: Insufficient quantitative data on variations in equipment
  - Data can only be gathered by / in cooperation with equipment companies
  - Use data from literature plus experiment on selected tools
- Combination with treatment of statistical variations necessary

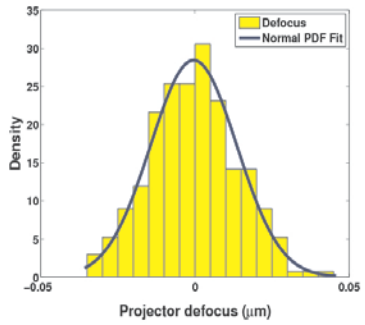
  $\Rightarrow$ Challenge: Predictive simulation chain equipment/process/ device/circuit for variations needed

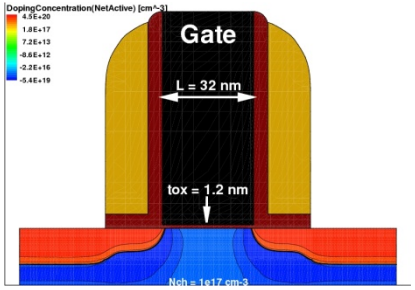
INTRODUCTION: SUPERTHEME OBJECTIVES

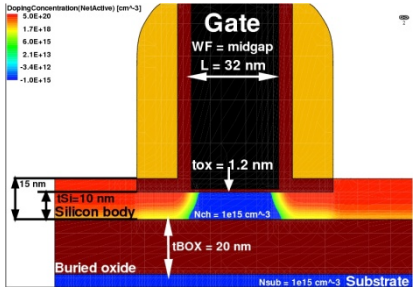
- Extend / integrate SW of partners
  + required third-party SW
- Data reduction / hierarchical simulation needed – from discretization of equipment to compact models
- Collect data for variability at process level
- Challenge: Correlations of variations must be included
- Exploit background of partners esp. for variabiliy simulation

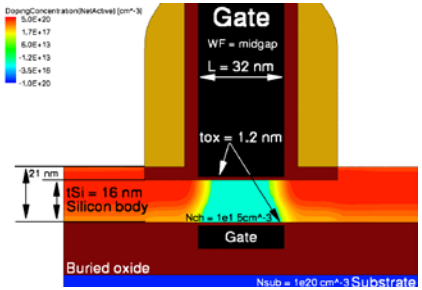
BACKGROUND PILLARS: PROCESS – IISB

Impact of lithography focus variations on transistor performance









Focus variations

⇩

CD variations

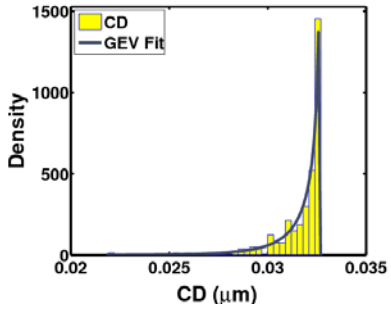
Bulk

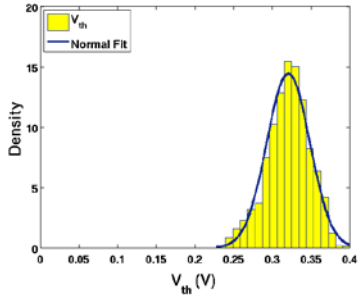
Device architecture

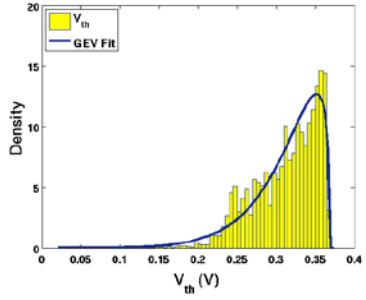
SG FD SOI

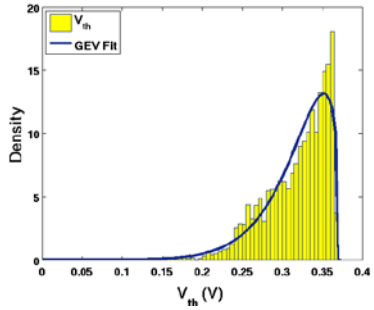
DG FD SOI

acts as filter for CD variations and leads to variations e.g. of V_{th}





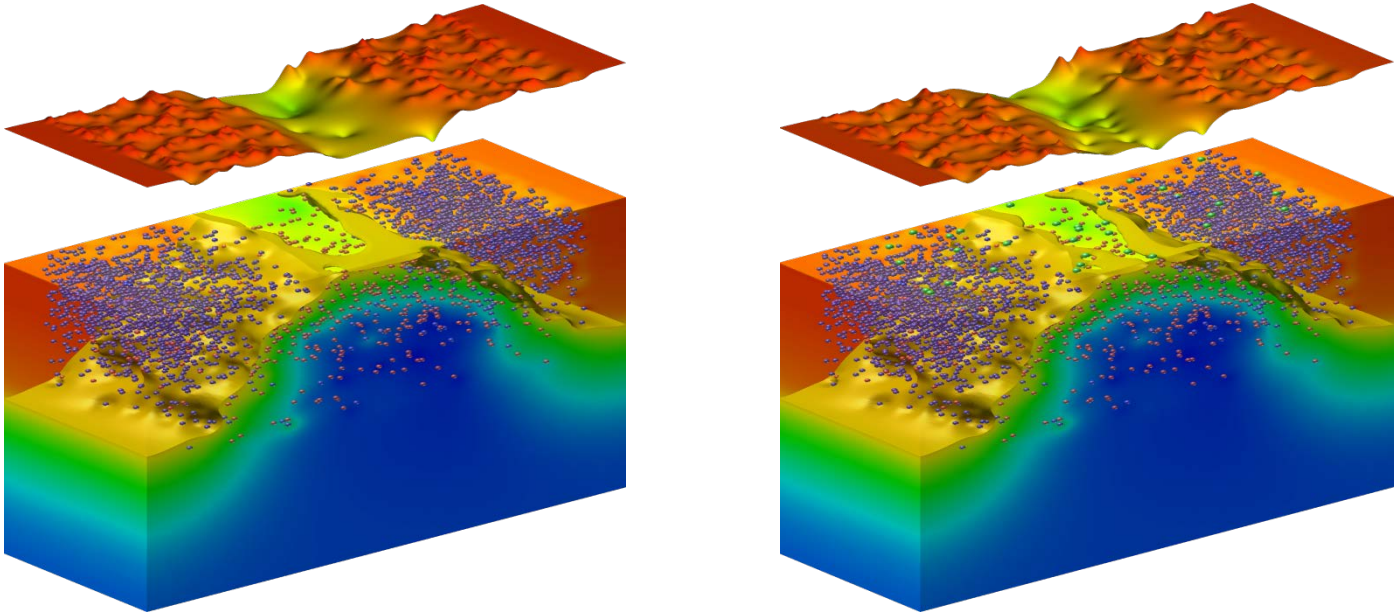




J. Lorenz et al., *Proc. 2009 Intl. Symposium on VLSI Technology, Systems and Applications*, Hsinchu, Taiwan, 2009, pp. 17-18.

BACKGROUND PILLARS: DEVICE – GU/GSS

Device simulation SW for the study of the impact of variations caused by the granularity of matter, esp. RDF, LER, MGG



Left: Simulation of a 45 nm technology transistor in the presence of discrete dopant, line edge roughness and polysilicon gate granularity. Right: Simulation of the same transistor subject to degradation. By chance two holes are trapped in the vicinity of the percolation path. From GU / GSS

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CONSORTIUM AND PROJECT DATA

- Project partners
  - Semiconductor industry: ams
  - Equipment companies: ASML, HQD, IBS, LASSE
  - SW house: GSS
  - Research institutes: Fraunhofer IISB (coord.), IIS/EAS
  - Universities: Univ. Glasgow, TU Wien
- Project period: 10/2012 – 12/2015
- EC funding: 3.3 M€ from FP7 ICT Call 8
  - Action line 3.1 “Very advanced nanoelectronic design, engineering, technology and manufacturability“
- See www.supertheme.eu

SUPERTHEME PROJECT STRUCTURE

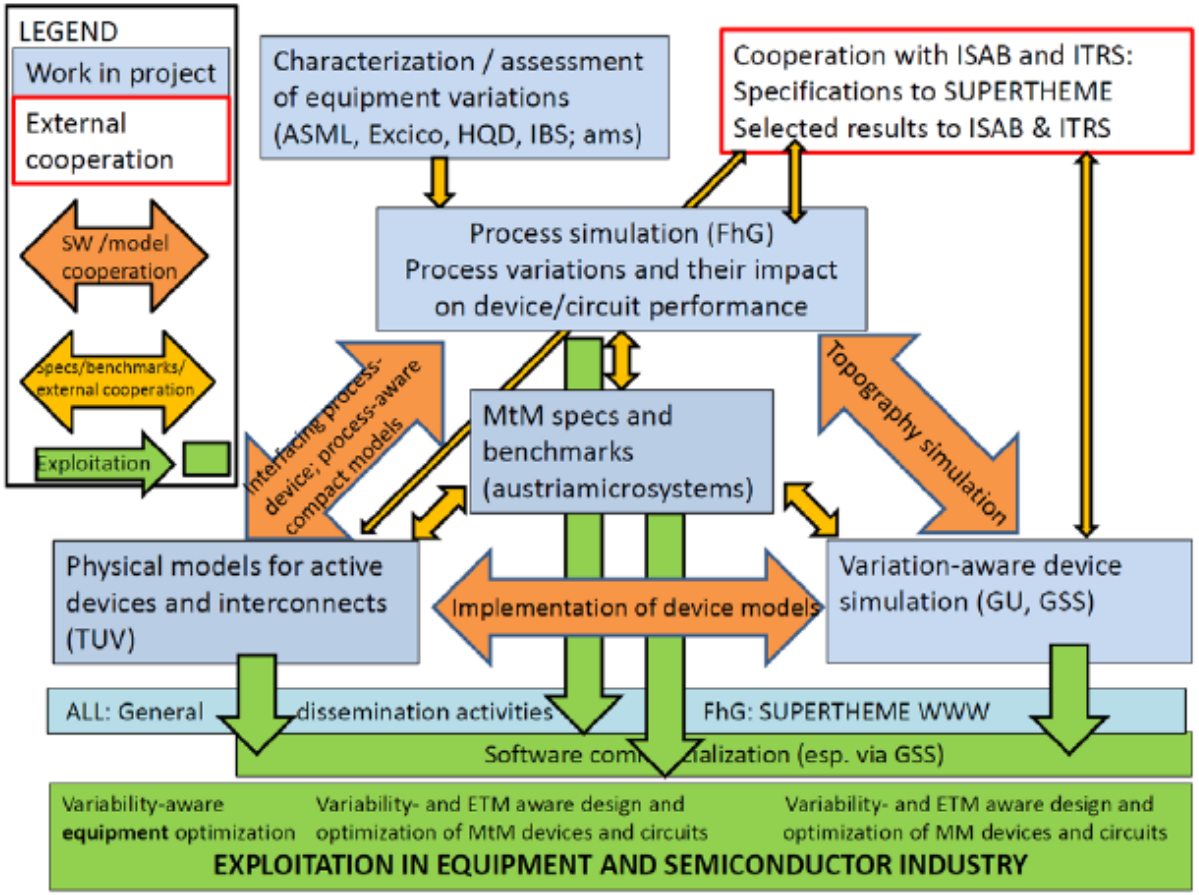
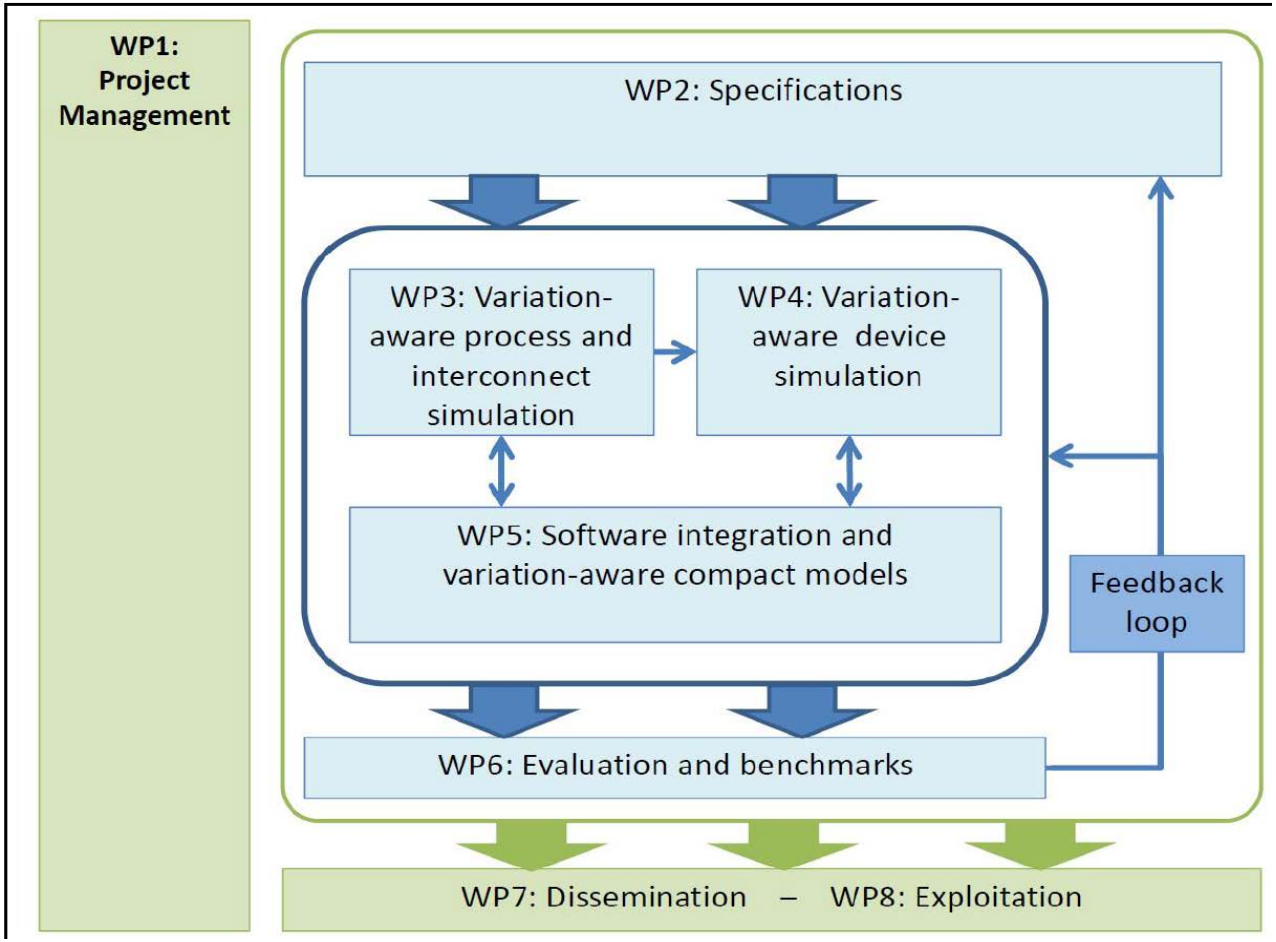


Fig. 2: Focal activities of SUPERTHEME partners and mutual interactions

(From SUPERTHEME proposal and DoW)

SUPERTHEME PROJECT STRUCTURE

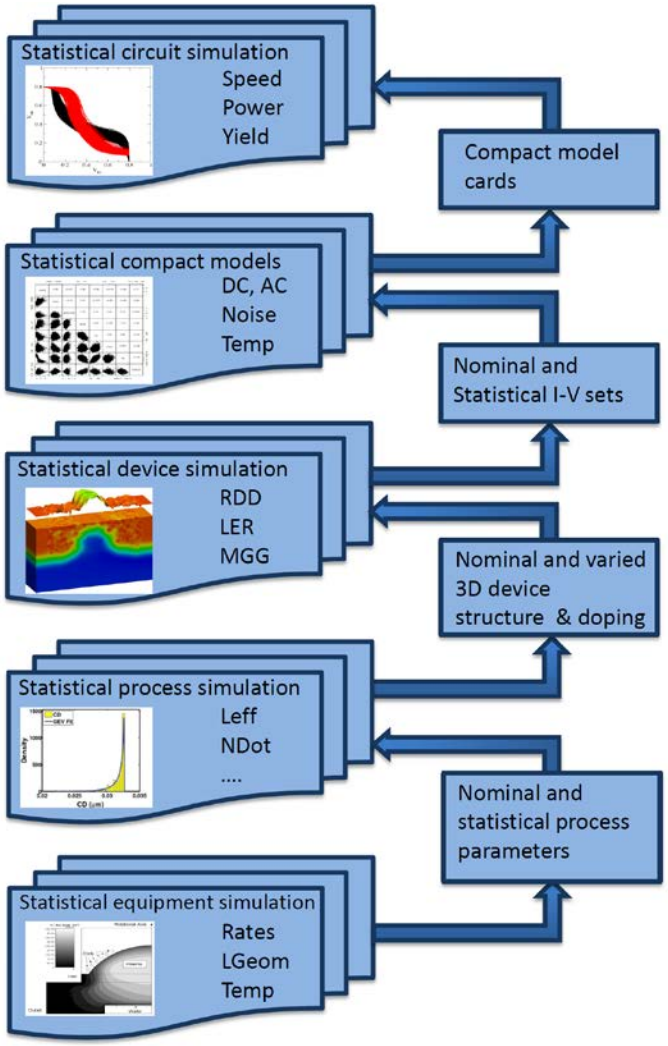


(From SUPERTHEME proposal and DoW)

METHODOLOGY USED

Simulation levels and tools used

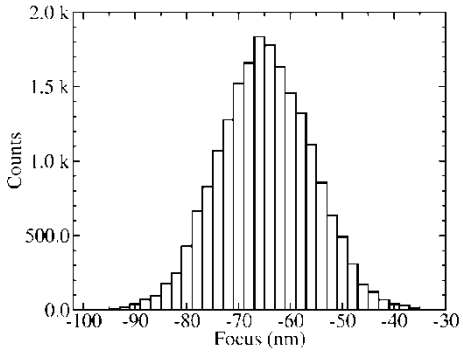
- Equipment simulation: Q-VT (Quantemol), CFD-ACE (ESI Group)
- Process simulation:
  - Lithography: Dr.LiTHO (Fraunhofer)
  - Etching/deposition: ANETCH / DEP3D (Fraunhofer)
  - Annealing: Sentaurus Process (SNPS)
- Device simulation: GARAND (GSS)
- (Statistical compact model extraction: MYSTIC (GSS))
- (Circuit simulation: RandomSpice (GSS))

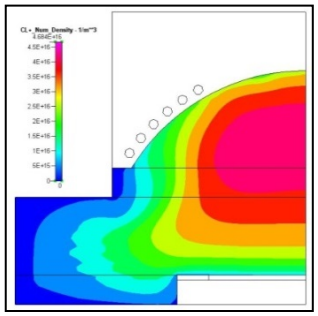


From J. Lorenz et al, SISPAD 2014

METHODOLOGY USED

- Assumed variations at equipment level – probability density p(P) of some varying parameter P (e.g. litho defocus/dose; position on wafer)





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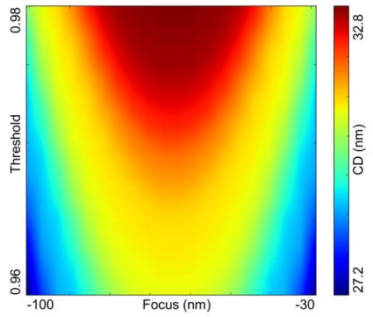
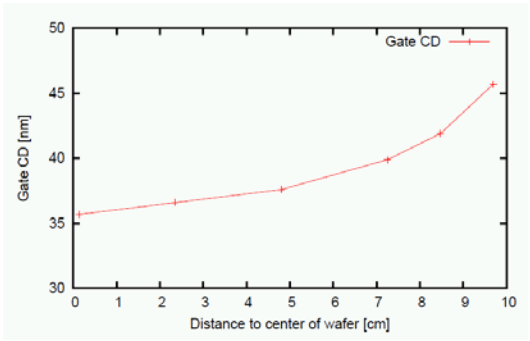
From J. Lorenz et al, SISPAD 2014

METHODOLOGY USED

- Integrated equipment and process simulation

  ⇨Variation of device geometries (and continuum doping) caused by process or equipment variations – e.g. *L(P)* and *W(P)*: ***Device Defining Data D3***

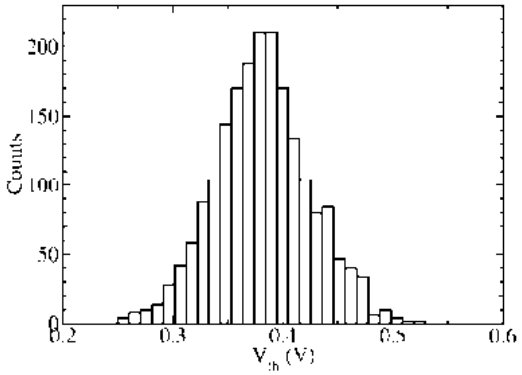




From J. Lorenz et al, SISPAD 2014

METHODOLOGY USED

- Stochastical device simulation based on geometries and doping of continuum devices (matrix of *L* and *W*), including RDF, MGG, LER
  - ⇨ Statistical probability densities g_s of electrical data for devices with identical geometry/continuum doping profiles



From J. Lorenz et al, SISPAD 2014

METHODOLOGY USED

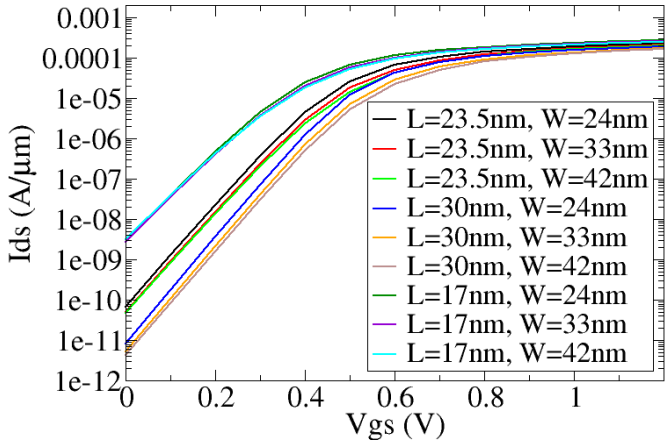
- Combination of equipment/process and device level by taking probability of geometry/continuum doping into account
- Extraction of hierarchical compact model

⇨ Statistical distribution h_s of electrical data for given p(P)

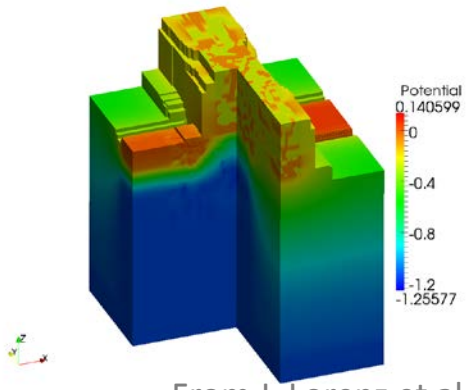
$$h_s = \int g_s(L(P),W(P))\, p(P)\, dP$$

EXAMPLE: 23.5 NM TRANSISTOR

- Continuum devices considered: Planar bulk NMOS transistors,
  - Mean values L =23.5nm, W =33nm
  - 5 x 5 matrix, L between 17nm and 30nm, W between 24nm and 42nm
- Example of results for continuum devices



- Potential for nominal device with RDF, MGG and LER (simulated with GARAND)



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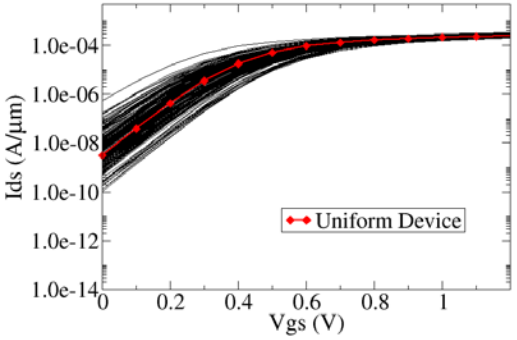
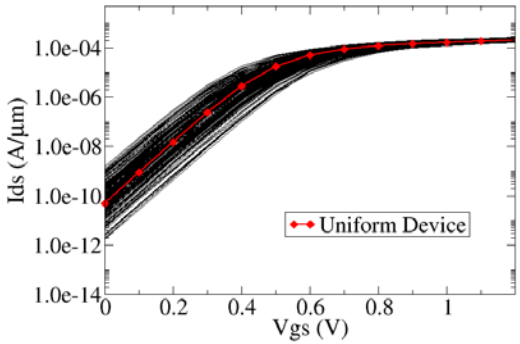
EXAMPLE: 23.5 NM TRANSISTOR

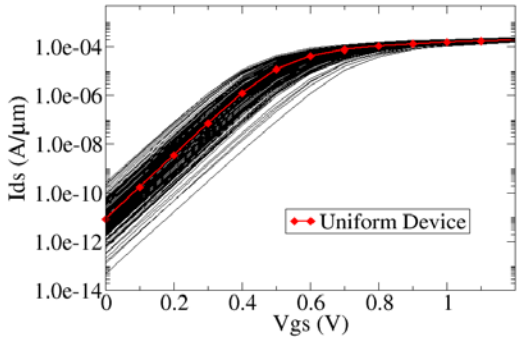
- Statistical device simulation including RDF, MGG and LER for matrix of 5 x 5 continuum devices
- Example: Output characteristics at V_D= 0,05V for devices with different L and W



min. L / max W
L= 17 nm, W= 42 nm



nominal device
L = 23.5nm, W = 33 nm

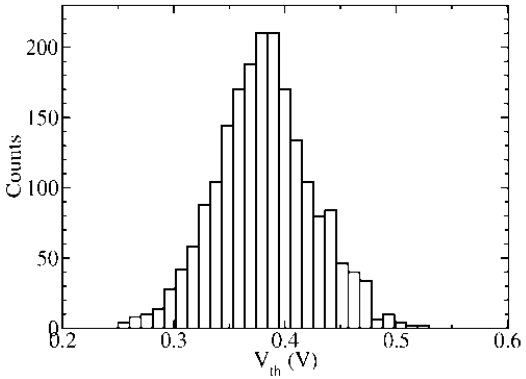


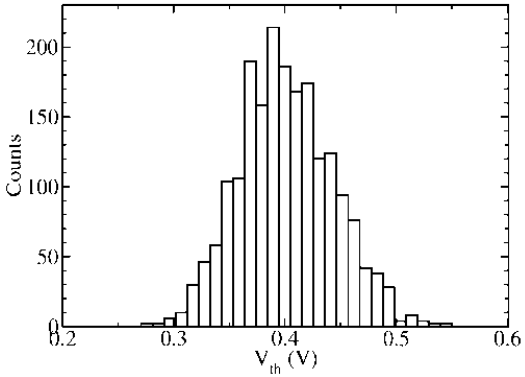
max. L / min. W
L = 30 nm, W = 24 nm

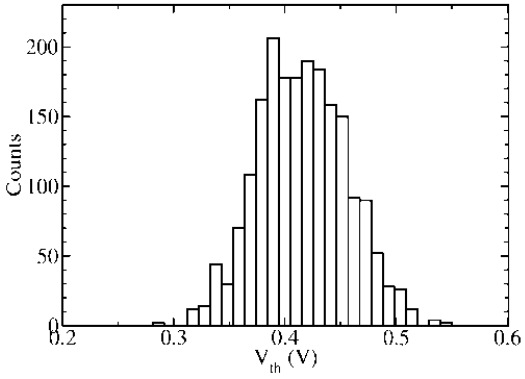
From J. Lorenz et al, SISPAD 2014

EXAMPLE: 23.5 NM TRANSISTOR

- Statistical device simulation including RDF, MGG and LER for matrix of 5 x 5 continuum devices
- Example: Probability densities for V_{th} at V_D = 0,05 V for devices with different L and W: Different minimum, mean and maximum values of V_{th} distribution







min. L / max W
L= 17 nm, W= 42 nm

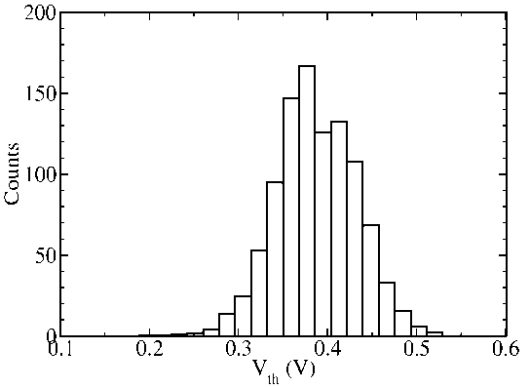
nominal device
L = 23.5nm, W = 33 nm

max. L / min. W
L = 30 nm, W = 24 nm

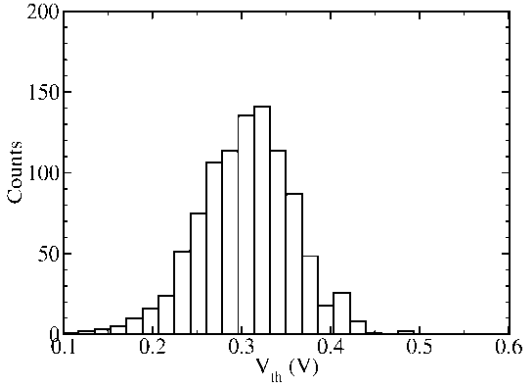
From J. Lorenz et al, SISPAD 2014

EXAMPLE: 23.5 NM TRANSISTOR

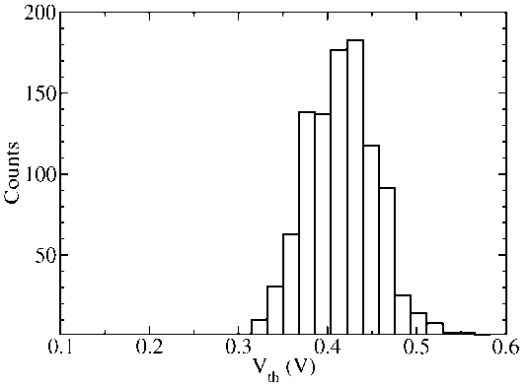
- Hierarchical compact model extracted
- Simulation of coupled influence from lithography (focus, dose), etching (equipment-induced bias variations), RDF, LER, MGG
- Example: V_{th} for average etch bias (5nm) and for different positions at the wafer
- PDF caused by litho variations, RDF, LER and MGG is strongly modified by etch bias variations across wafer



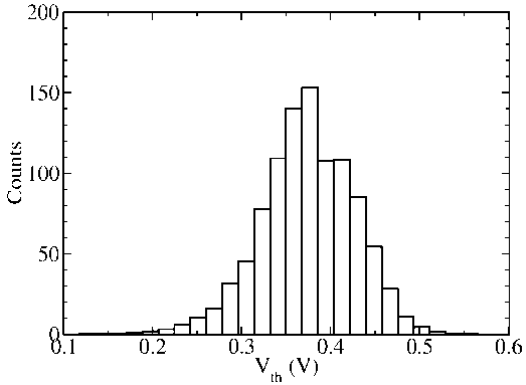
Etch bias 5 nm



Etch bias 10 nm



Etch bias 0 nm



Average across wafer

CONCLUSIONS

- SUPERTHEME has demonstrated:
  - Feasibility of hierachical variability simulation equipment/process/device/circuit
  - Important impacts on device and circuits
  - Correlations can and must be included
  - Gaussian sources of variability frequently lead to highly non-Gaussian variations at device or circuit level
- Very promising prospects for application and extension of work

ACKNOWLEDGEMENTS

- Contribution of all colleagues at partners highly appreciated
- Valuable inputs from EC review team and from SUPERTHEME ISAB
- Funding from EC highly appreciated

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