Ben Kaczer, imec

ESSCIRC ESSDERC 2015

HIERARCHICAL MODELING OF RELIABILITY AND TIME DEPENDENT VARIABILITY IN THE MORV PROJECT

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PROJECT MOTIVATION

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- Scope: Timing analysis of complex circuits with aging effects

- State of the art: timing analysis performed using aged liberty files
- With this approach
  - Local, per-node parameters (activity, temperature, voltage), i.e., actual workloads, are not considered
  - As a consequence, timing analysis is pessimistic

- Objective : to develop timing flow aware of per-gate instance parameters
- Benefits :
  - Greater accuracy
  - Reduced pessimism

PROJECT BACKGROUND

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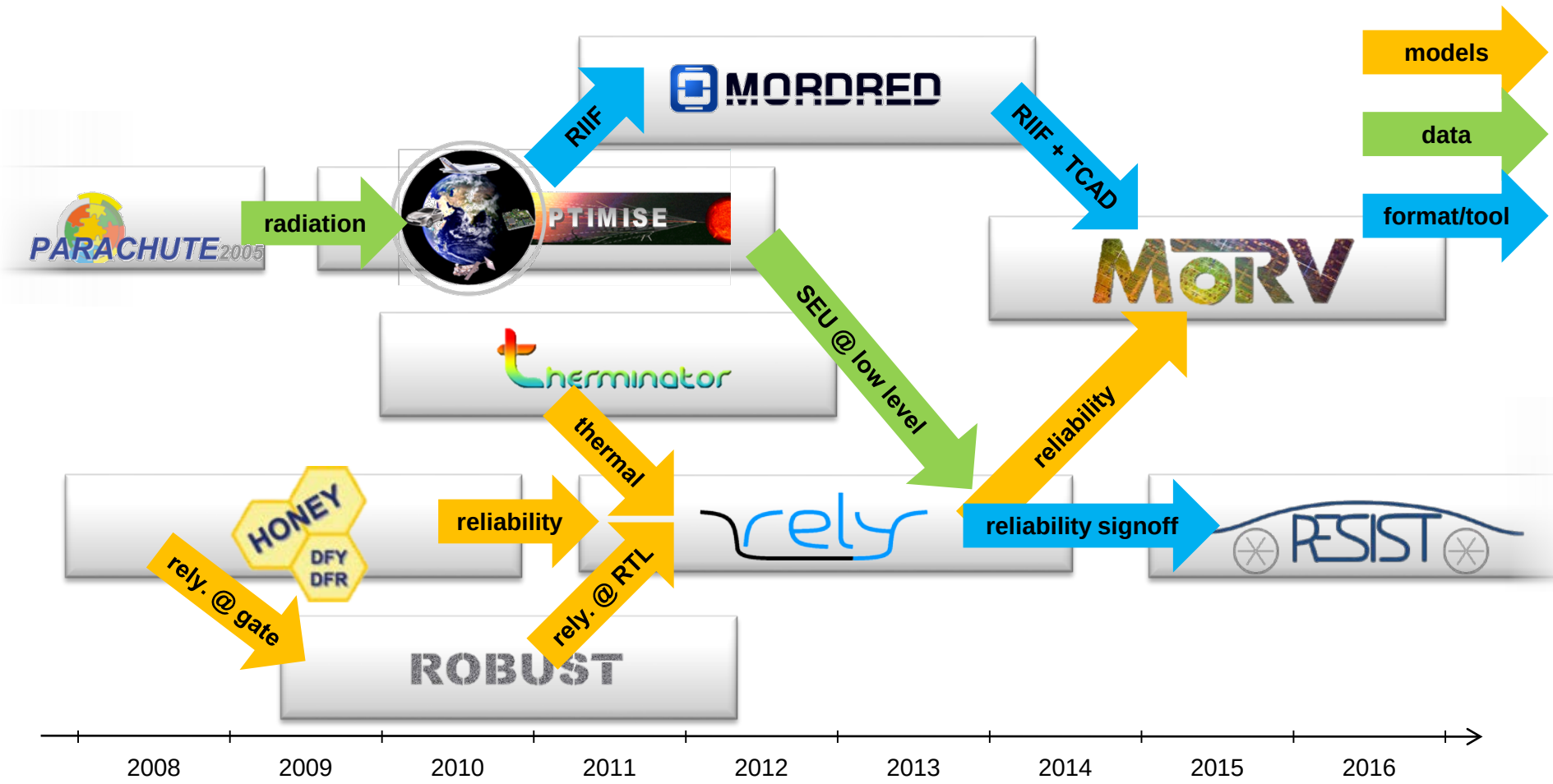

ABSTRACTION HIERARCHY

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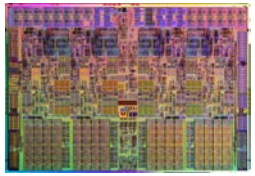
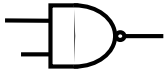
ESL



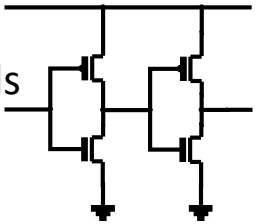
HDL/RTL

ALU

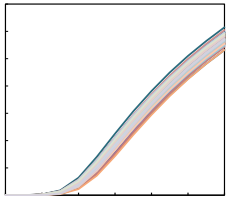
Gates



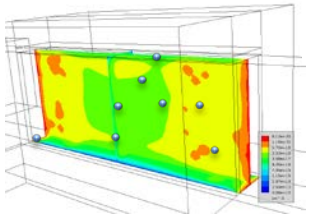
Circuits



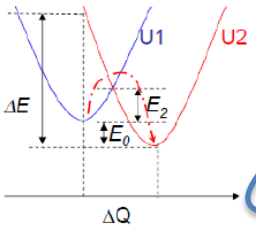
Compact models



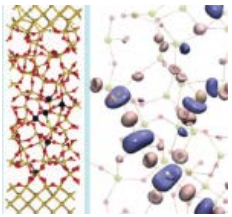
Device transport



Trap kinetics



1st principles



MORDRED

MoRV

OUTLINE

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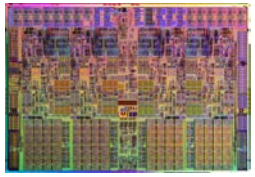
ESL



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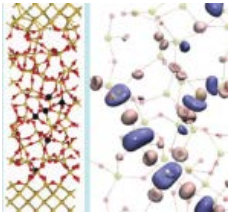

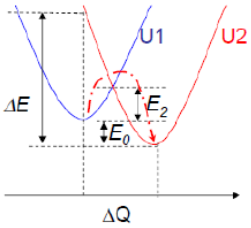

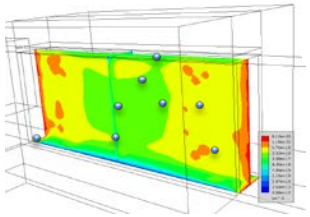

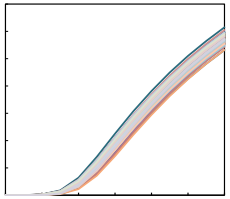

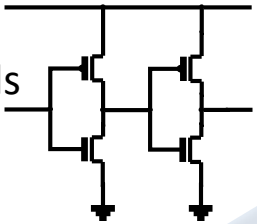

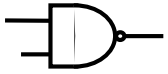

2

1

BIAS AND TEMPERATURE STRESS: TYPICAL DURING FET OPERATION

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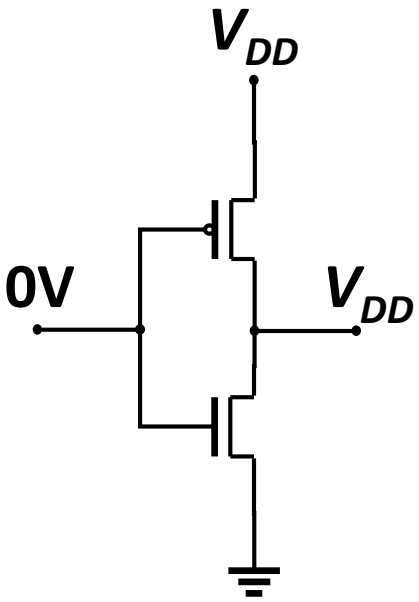
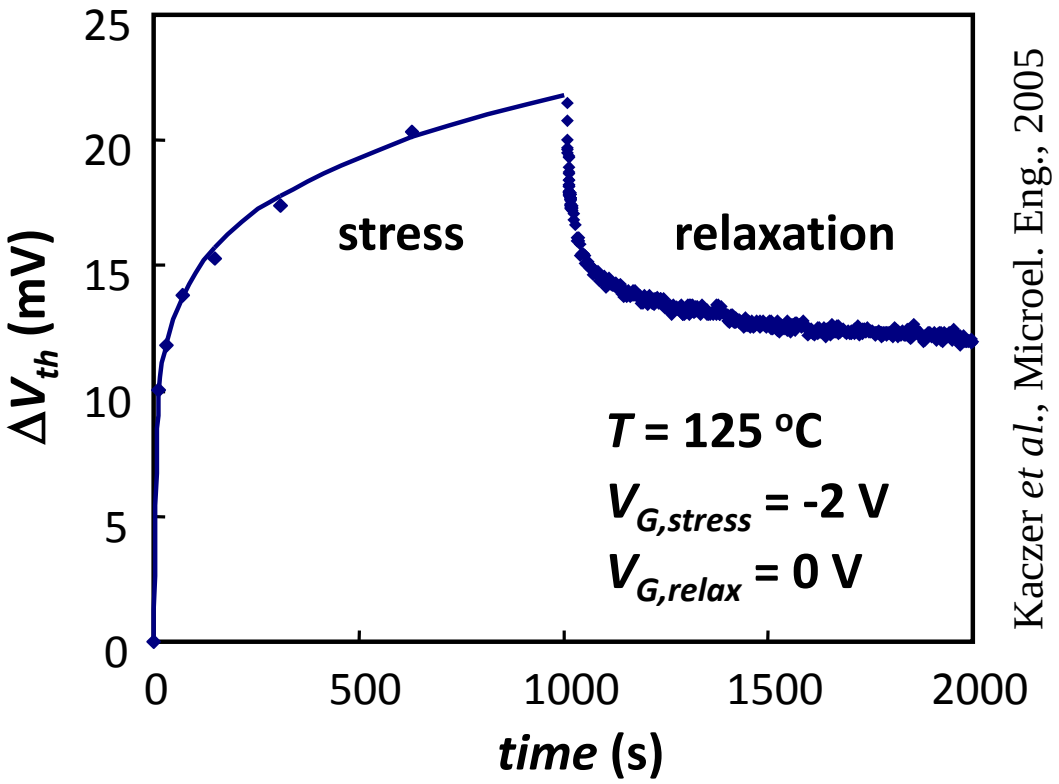
Example: PFET V_{th} at **N**egative gate **B**ias (and typically at elevated **T**emperature) starts shifting (shows **I**nstability) → **NBTI**





Charging of preexisting and fabricated interface and oxide defects

→ ΔV_{th} and $\Delta\mu$

DEEPLY-SCALED DEVICES: INDIVIDUAL EMISSION EVENTS VISIBLE IN NBTI RELAXATION TRACES

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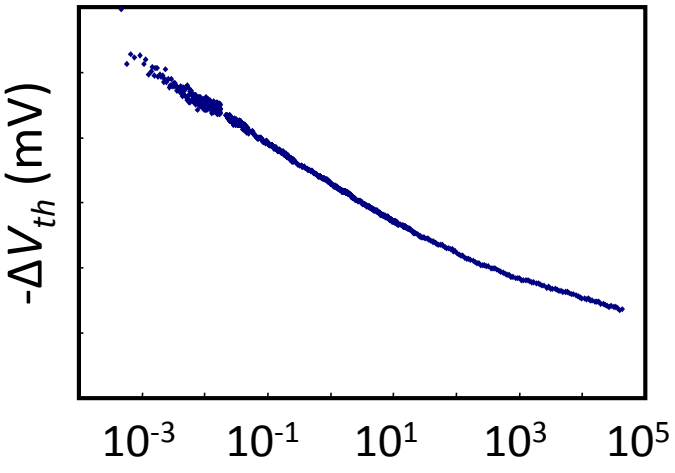
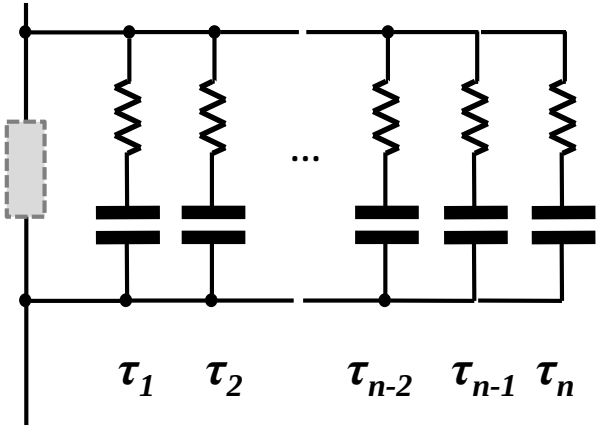
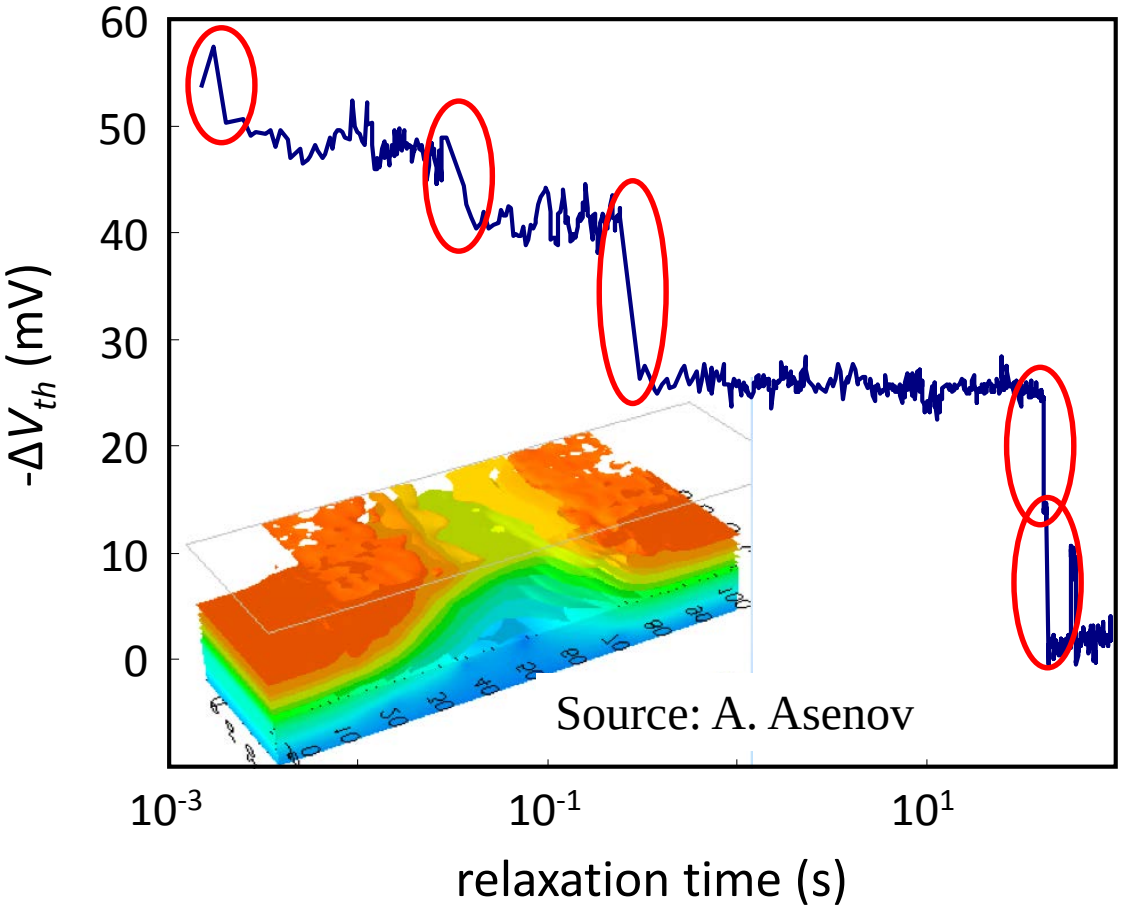
Large pFET



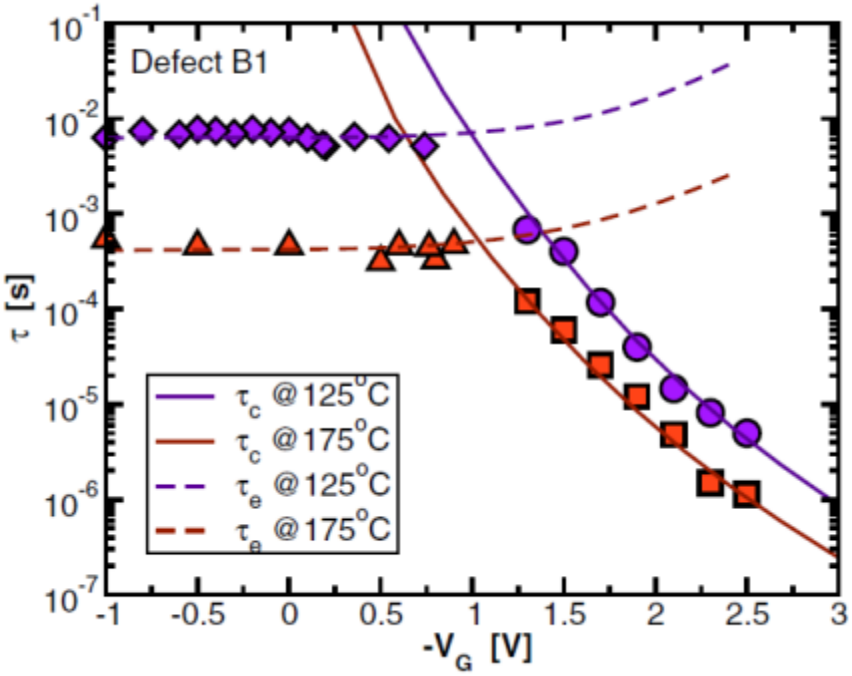


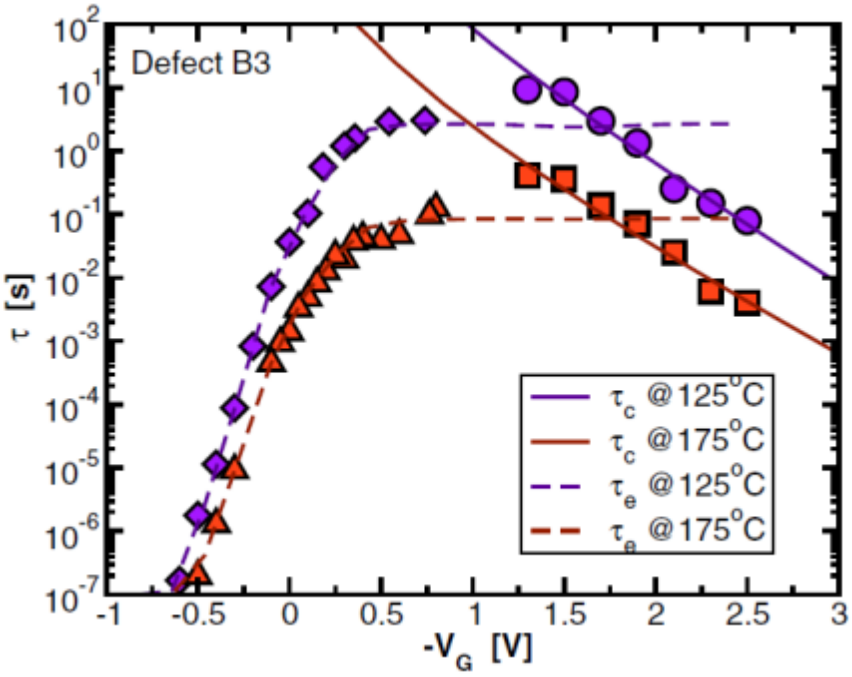
70 × 90 nm² pFET



Kaczer *et al.*, IRPS 2009

TRAP CONSTANTS *V* AND *T* DEPENDENT, DIFFERENT FOR EVERY TRAP





Grasser *et al.*, IRPS 2013

We need to know the **distributions of τ_c(V,T) and τ_e(V,T)**

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TRAPPING (CAPTURE) AND DETRAPPING (EMISSION): 2-STEP PROCESSES

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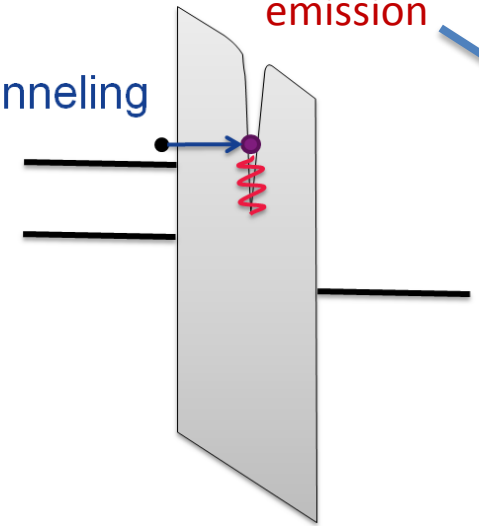
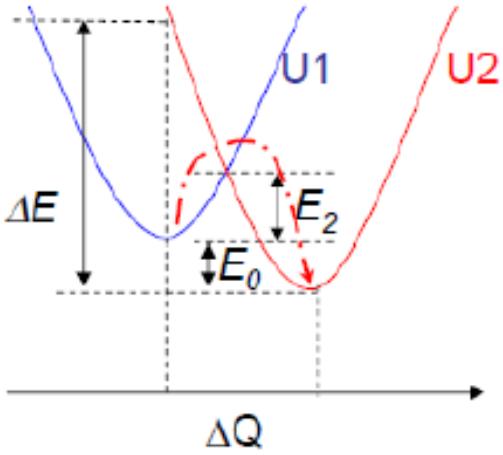
Structural relaxation + phonon emission

$$k_f = \frac{2\pi\rho_M(E_F)}{h}\left[\frac{\pi}{\lambda k_B T}\right]^{1/2}\int_{-\infty}^{\infty}[H_{DA}(\epsilon)]^2 \times \exp\left[-\frac{(\lambda + (E_{app} - E^\circ)e - \epsilon)^2}{4\lambda k_B T}\right] f(\epsilon)\, d\epsilon$$

Tunneling





DESCRIPTION OF DEFECTS

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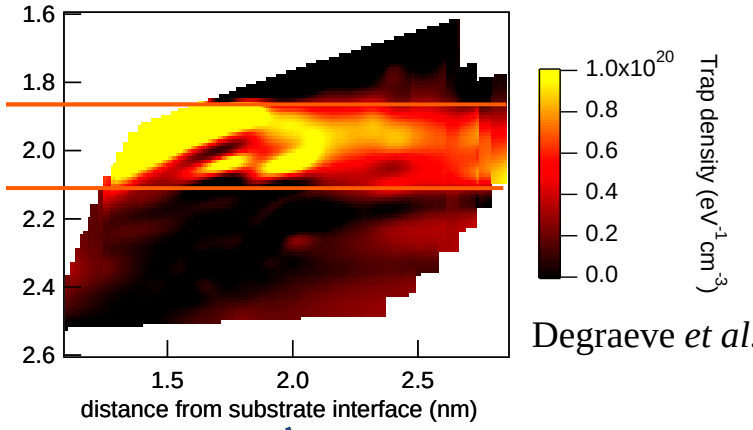
Defects characterized by **distributed** properties:

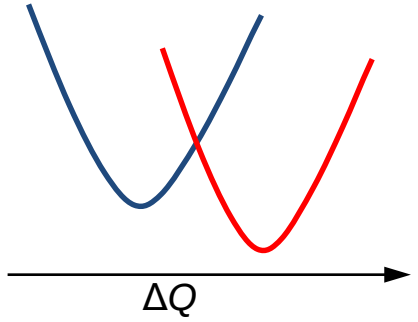
- Energy
  - wrt band gap
  - Structural
- Position in oxide
- Impact on device



Degraeve *et al.*

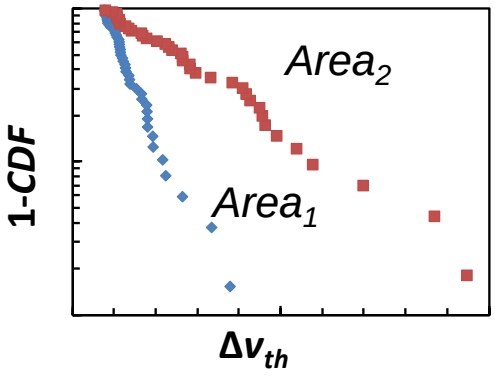
Adopted approach:

- **Discrete defects** (e.g., Sdevice: discrete solution of Grasser, Kaczer *et al.*, IRPS 2009)
- Properties taken from above distributions

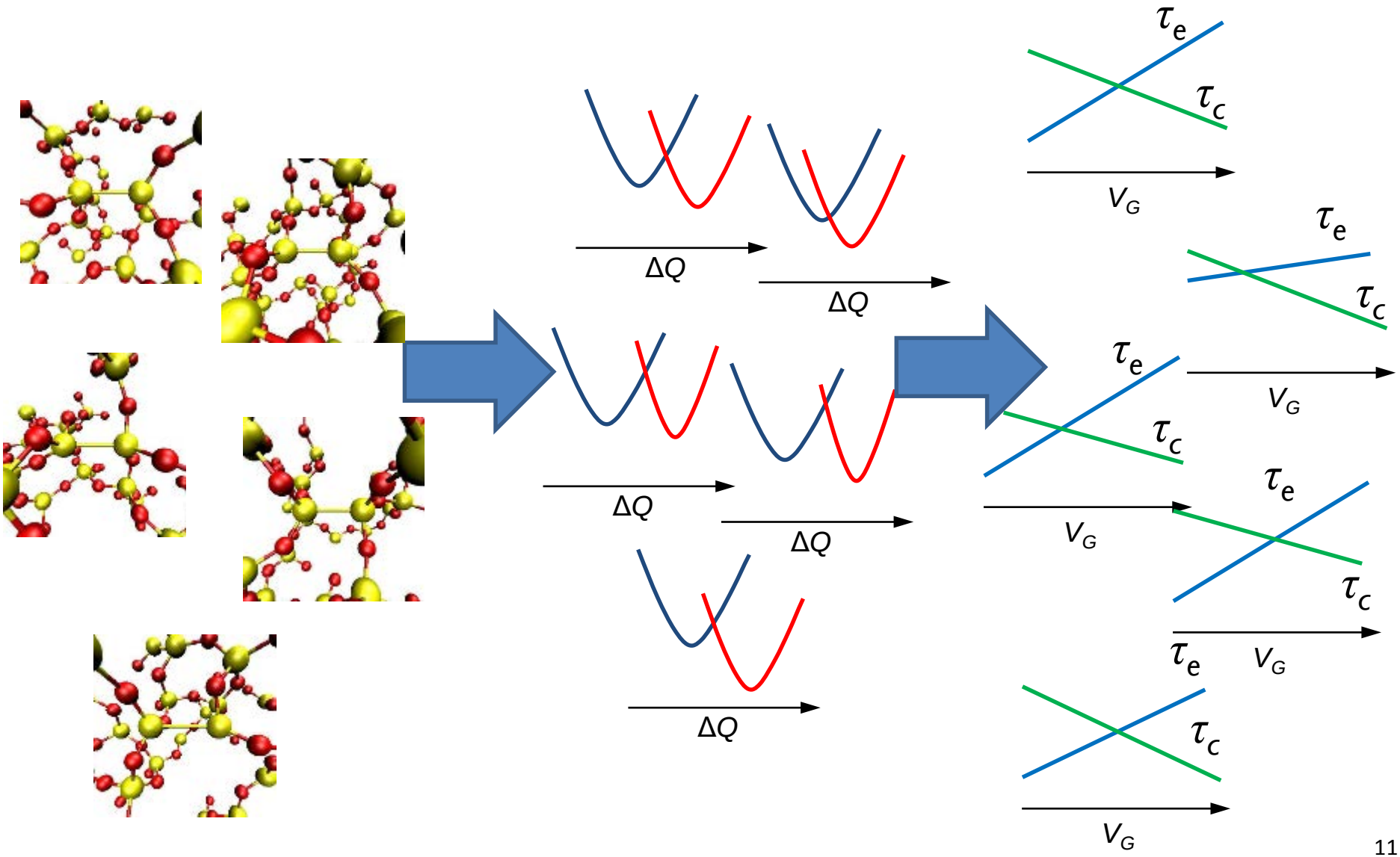


Advantages:

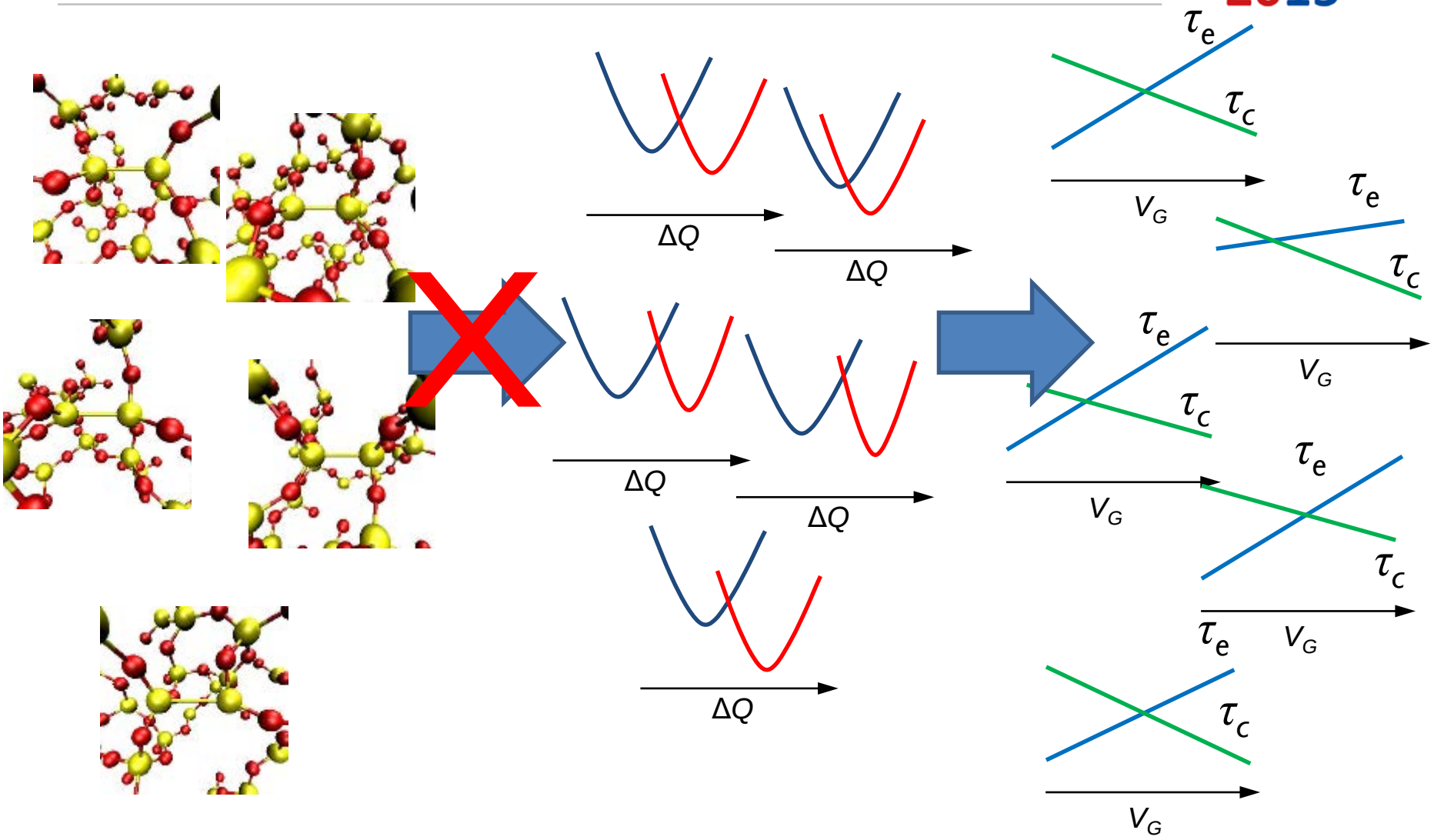
- Low level of abstraction
- Once properly set up, all trap-related effects come out "for free"



STRUCTURAL COMPONENT IN DISCRETE TRAPS APPROACH



PRAGMATIC ASSUMPTION



Assume normal distributions of parabolic well parameters

MEASURED BTI DEPENDENCES MODELED AND REPRODUCED IN TCAD

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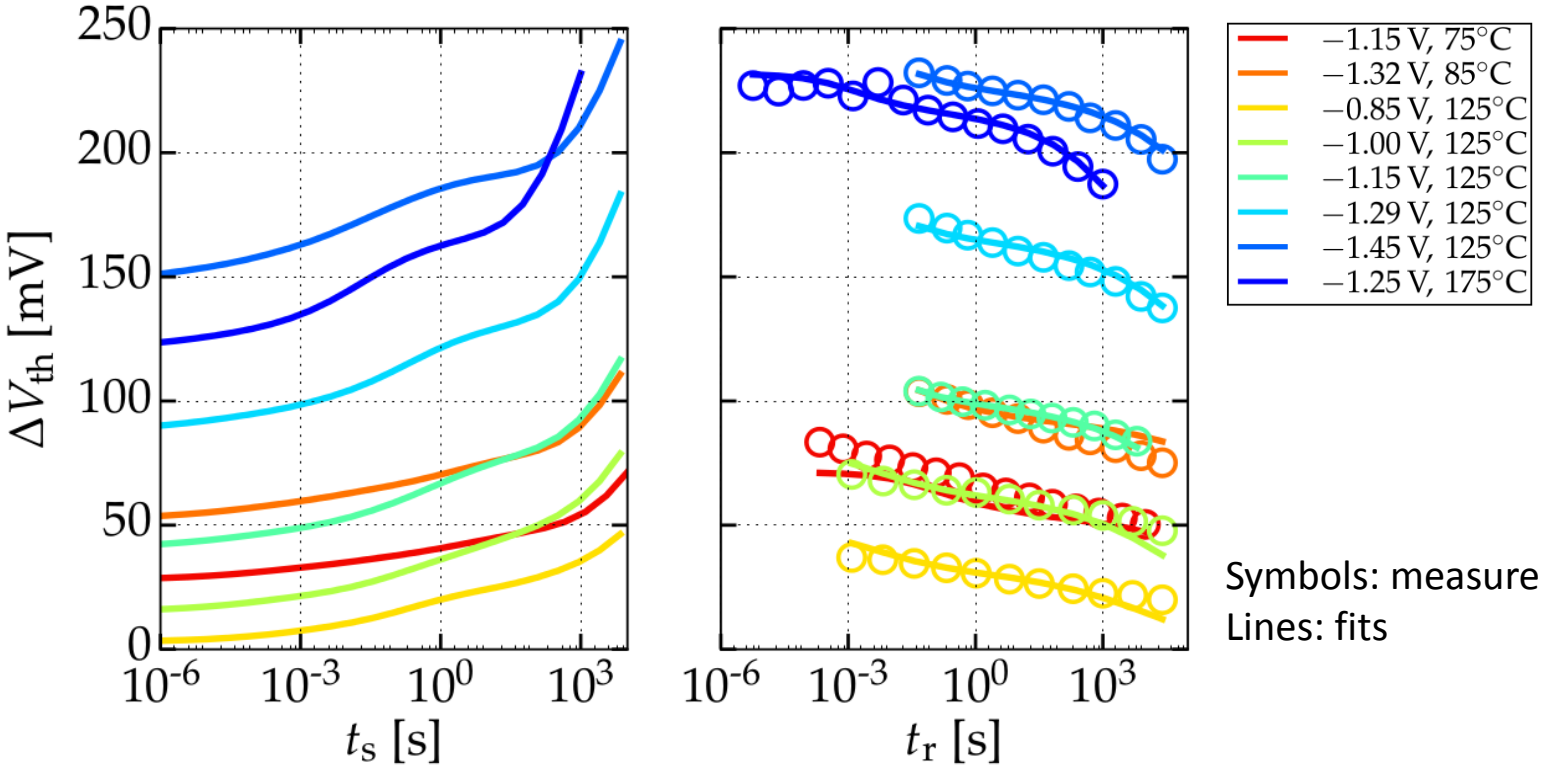
Extended-MSM measurements + “brute force” fitting with ~7000 “bulk” (full Non-radiative Multi-Phonon, NMP) and “interface” (dual-well, DW) defects

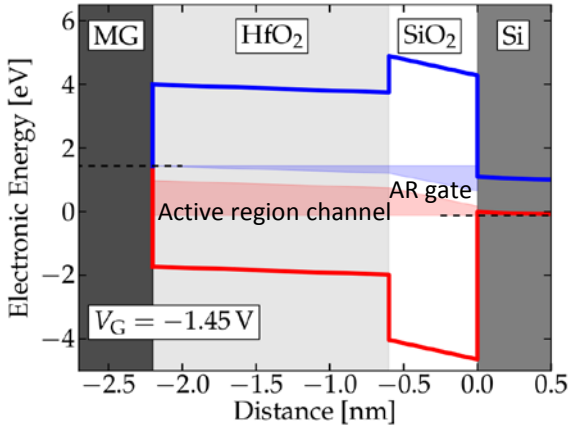


Symbols: measurements
Lines: fits

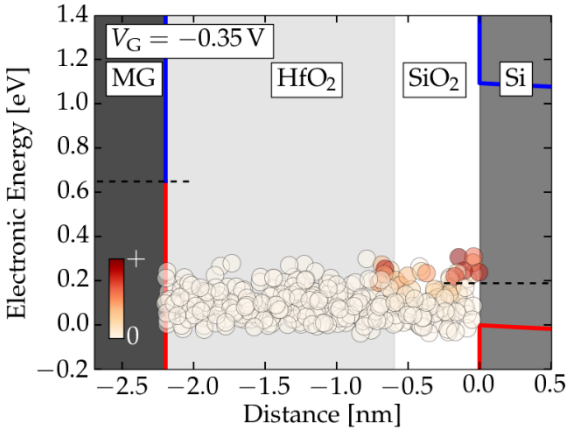
http://www.globaltcad.com

Courtesy G. Rzepa, TUW

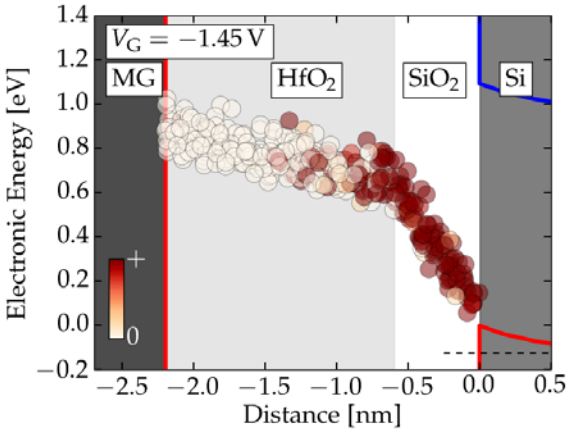
EXAMPLE OF FITTING



V_G = -0.35V

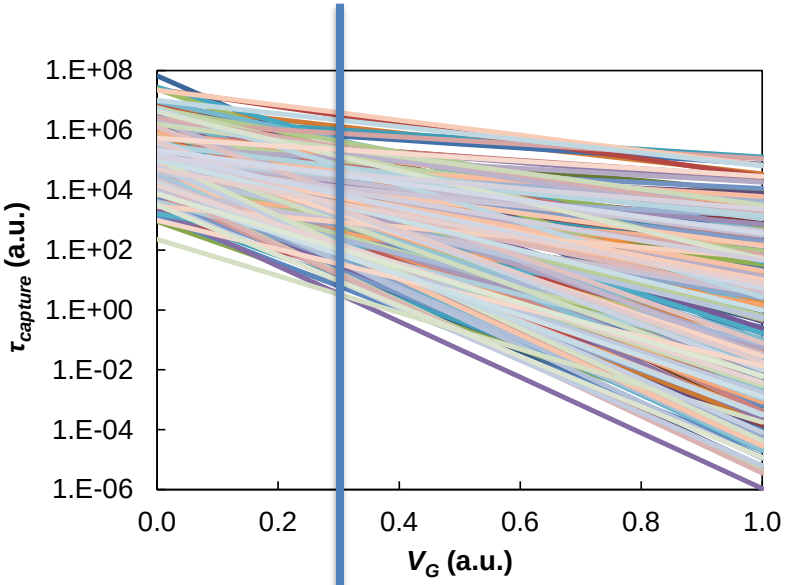


V_G = -1.45V



Courtesy G. Rzepa, TUW

RTN BEHAVIOR CAN BE REPRODUCED



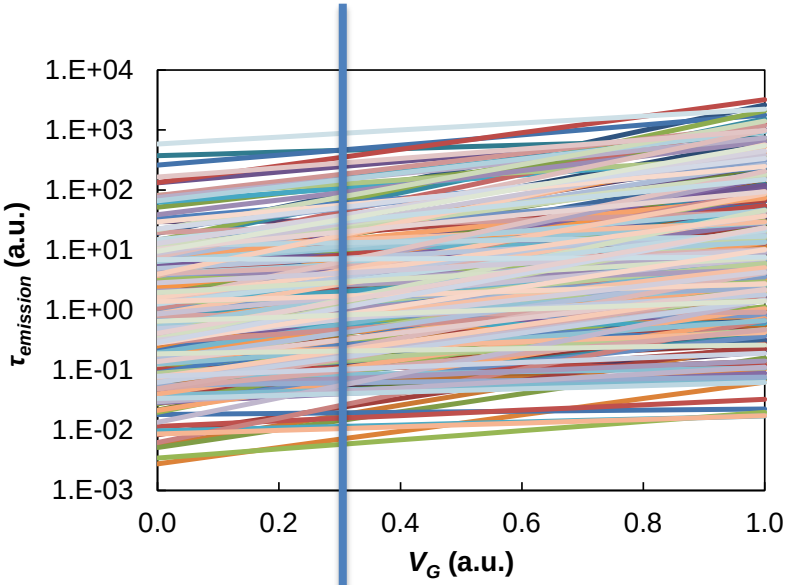
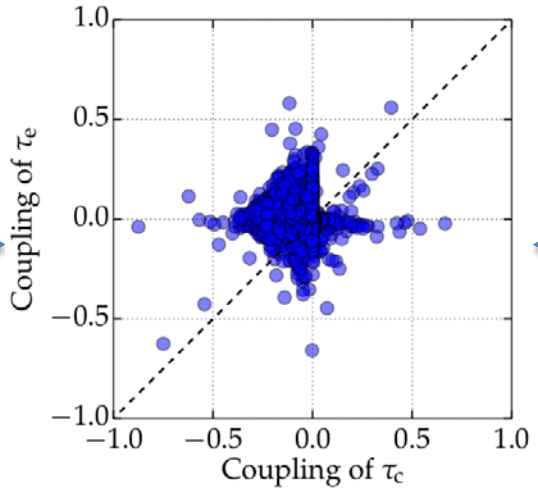
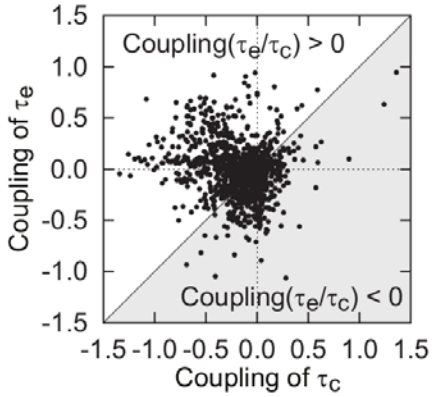


illustration only



RTN Measurement

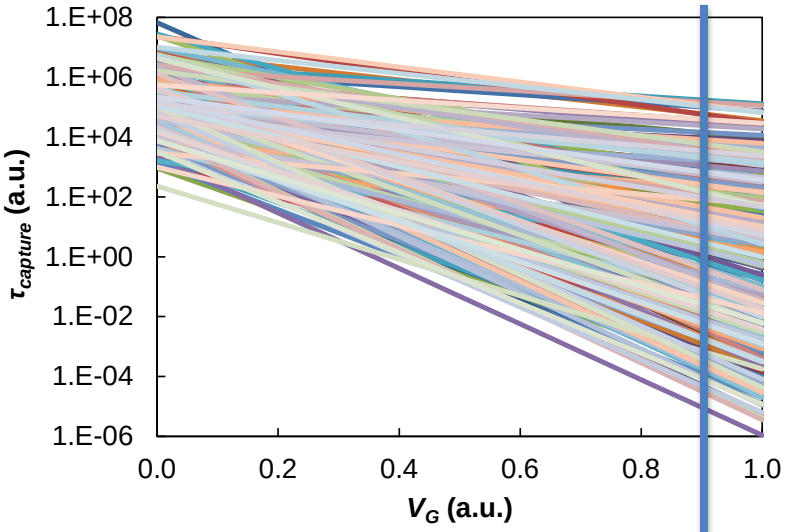


Miki *et al*, IEDM 2012

$$\text{Coupling} = \frac{kT}{q}\frac{\partial \ln \tau}{\partial V_G}$$

"slope" of $\tau(V)$ plot

SAME APPROACH ALLOWS CONNECTION TO BTI AND "CET MAPS" (LARGE DEVICES)



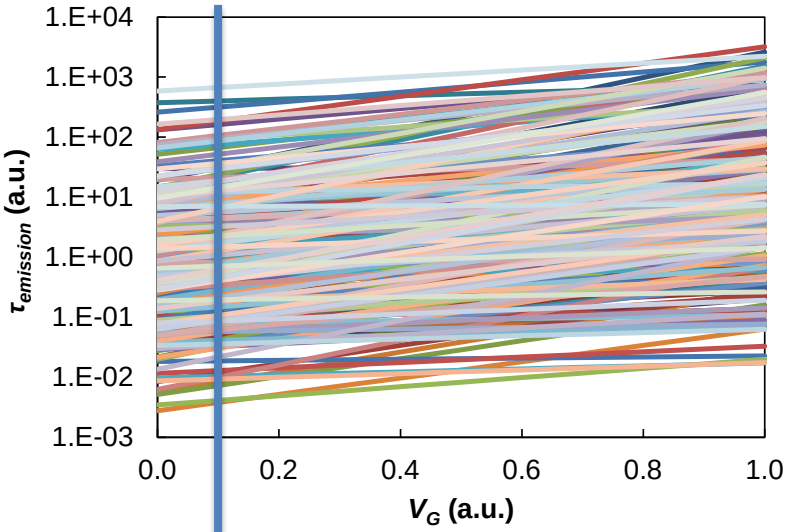
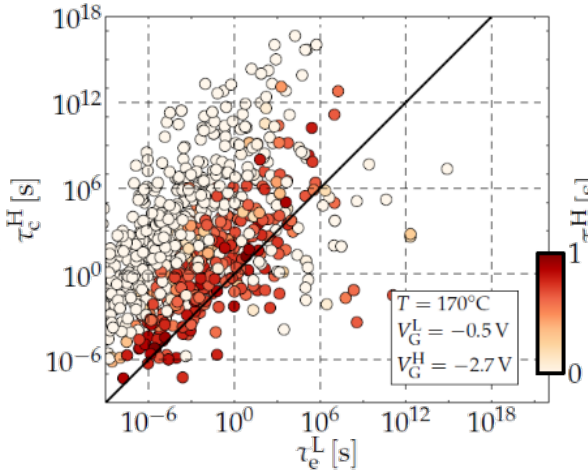
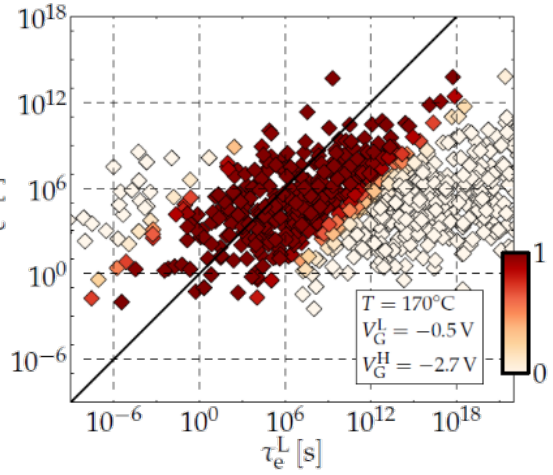


illustration only

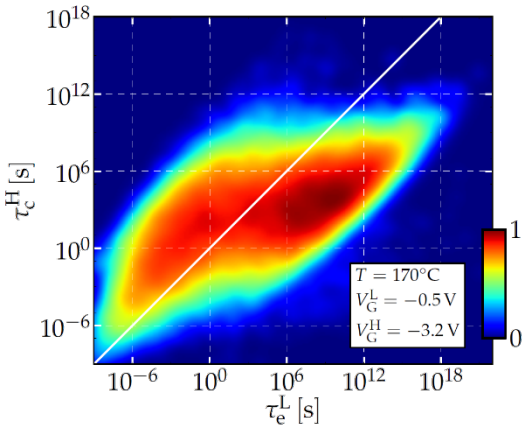
Bulk (NMP)



Interface (DW)

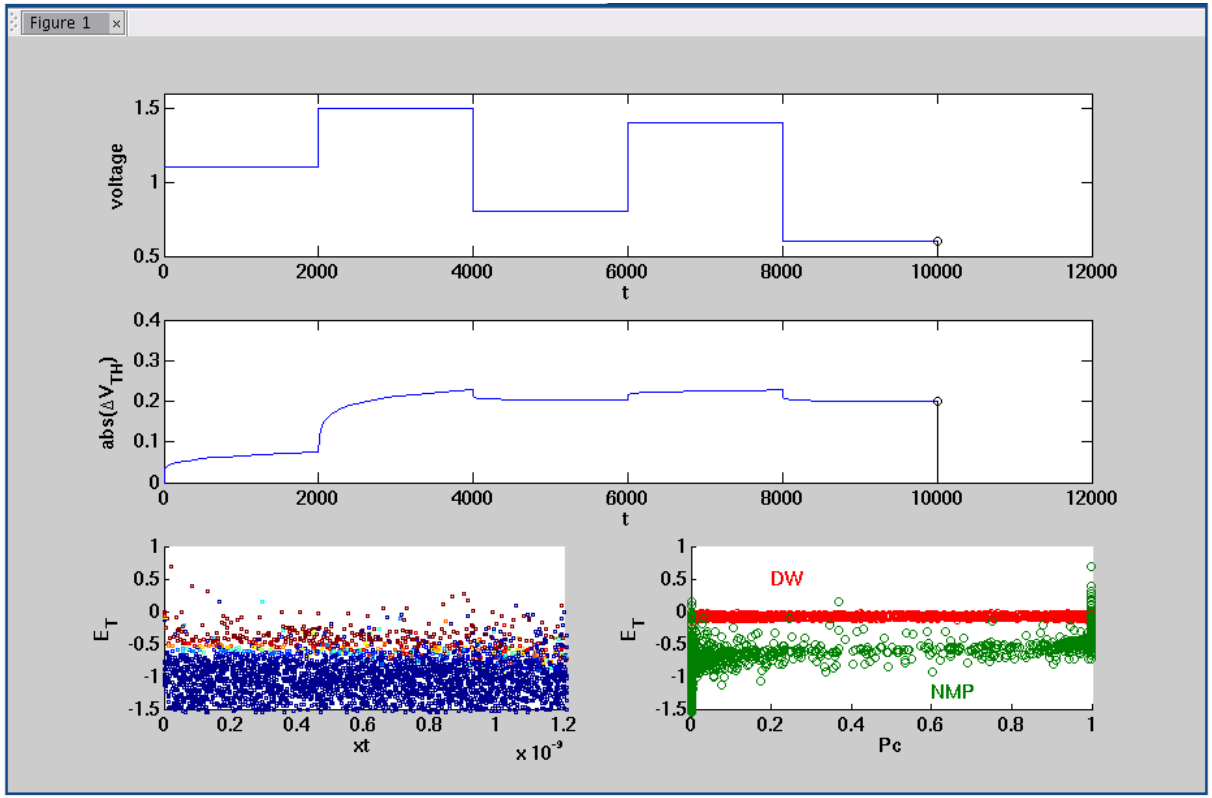


Capture/Emission Time (CET) Map



Rzepa *et al.*, SISPAD 2014

DEGRADATION DURING ARBITRARY $V_G(t)$ WAVEFORM CAN BE SIMULATED



- Trap occupation probability $P_c(t)$ calculated for every trap

(possible for constant and periodic phases, see e.g. Rodopoulos *et al.*, TDMR 2014; Giering et al., IIRW2014)

- Only impact on V_{th} considered
- In small devices with a handful of defects, variability naturally reproduced

DEEPLY-SCALED DEVICES CONTAIN ONLY A HANDFUL OF DEFECTS

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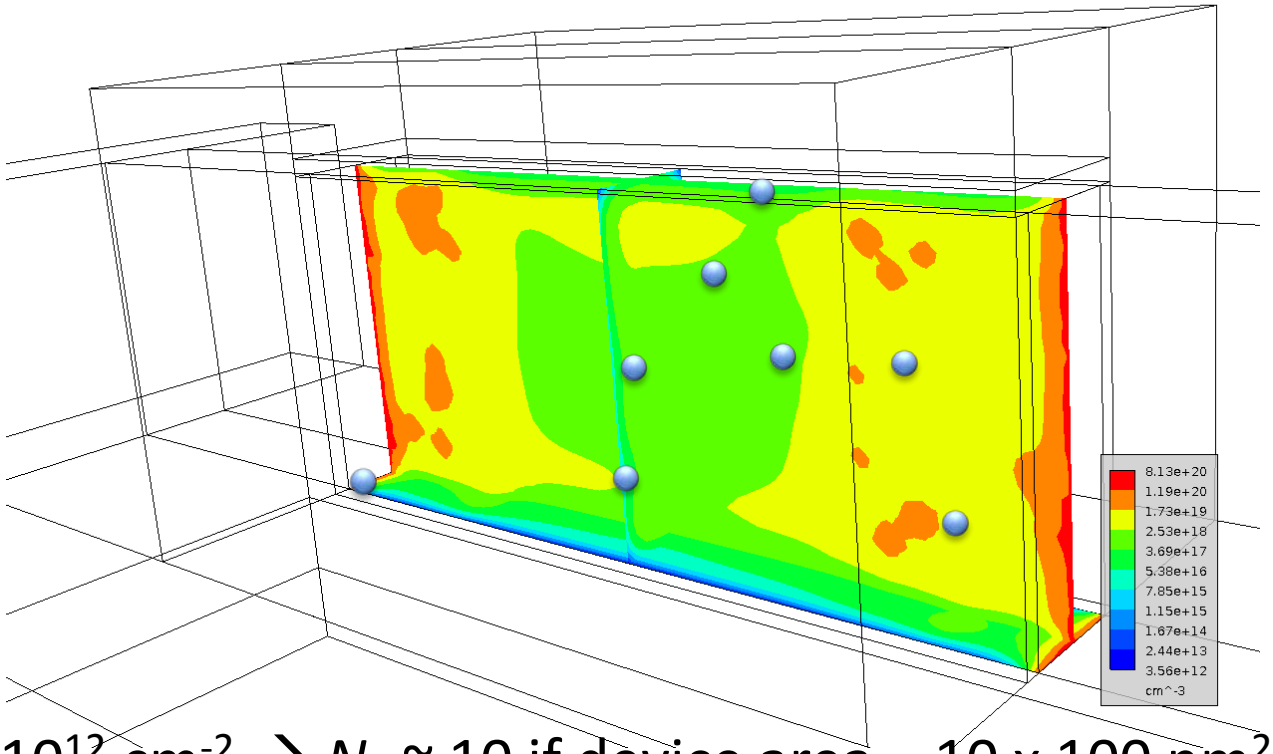
In deeply-downscaled technologies, only a handful of stochastically-behaving defects will be present in each device



Courtesy of M. Bina, TUWien

N_{ot} = 10^{12} cm^{-2} → N_T ~ 10 if device area = 10 x 100 nm^2

ΔV_{th} due to charged defects will be different in each device

→ **time-dependent variability** in addition to time-0 variability

INDIVIDUAL DEFECTS RESULT IN TIME-DEPENDENT VARIABILITY

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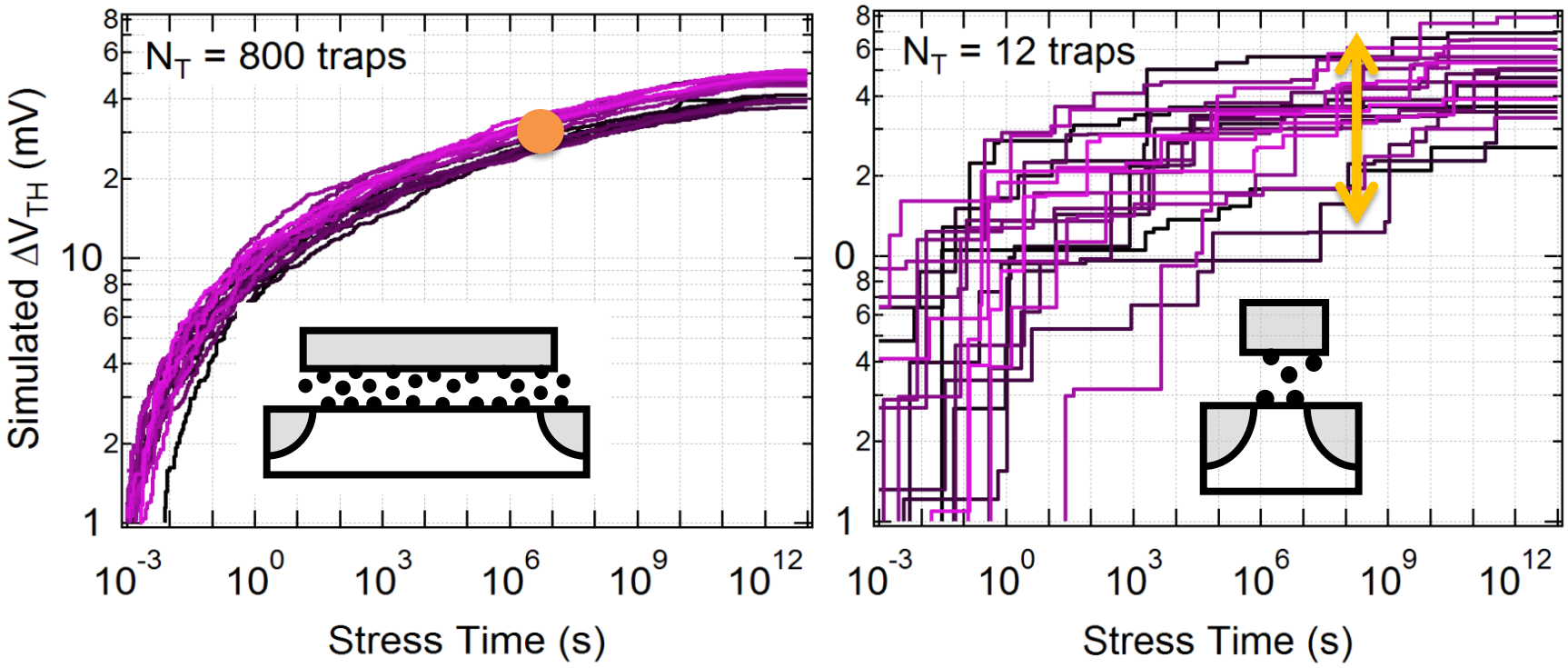

Grasser *et al.*, IEDM 2010

- Individual devices contain Poisson-*distributed* number of defects
- Individual defects have exponentially *distributed* impact on device

→ As opposed to large devices, the ΔV_{th} in deeply-scaled devices will be distributed

- Behavior naturally reproduced in the chosen discrete-defect approach

OUTLINE

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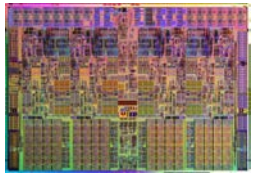
ESL



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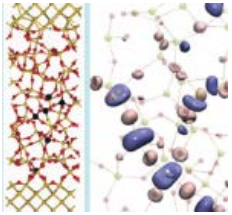

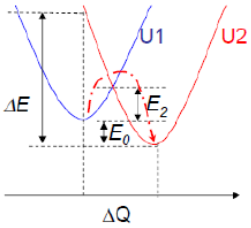

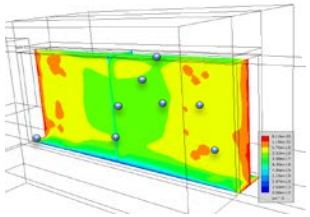

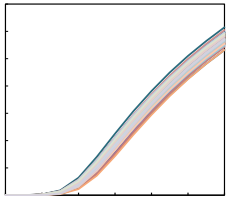

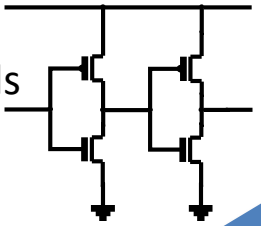

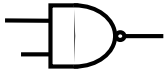

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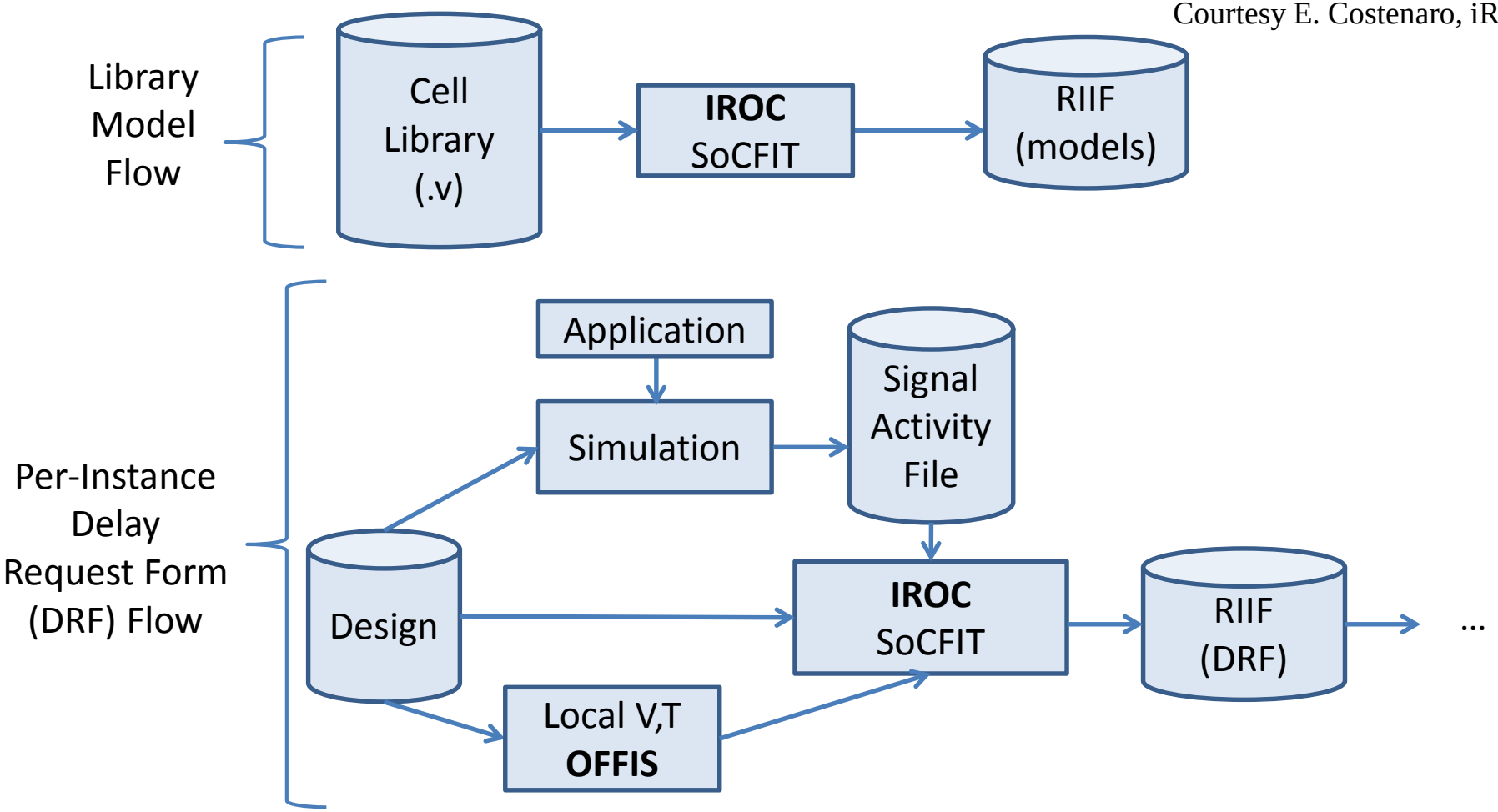
LIBRARY AND GATE LEVEL FLOW

ESSCIRC ESSDERC 2015

Courtesy E. Costenaro, iROC



- SoCFIT is IROC's internal chip-level reliability tool
- A cell library can be converted into per-cell type reliability models (RIIF)
- GLN of a design can be read, converted to per-instance **D**elay **R**equest **F**orms (DRF in RIIF)

EXAMPLE LIBRARY RIIF MODEL

ESSCIRC ESSDERC 2015

Courtesy E. Costenaro, iROC

```
component AND2_X1;
   // Operating parameters
   parameter VCC = 1.0;
   parameter TEMP = 25;

   parameter A_INP_ACTIVITY; // activity on A-input
   parameter B_INP_ACTIVITY; // activity on B-input
   parameter Y_OUT_ACTIVITY; // activity on Y-input

   // Failure modes (radiation induced)
   fail_mode SET_25ps = 10 ; // FIT
…
   fail_mode SET_150ps = 1; // FIT
 //-------------------------------------------------
 // Failure modes (EM induced)
   fail_mode EM_Y_STUCK = 0.02; // per-gate EM FIT rate
 //-------------------------------------------------
   // Added delay due to BTI
   parameter A_Y_RISE_INC_DELAY = 0;  // incr. delay (ps)
   …
   parameter B_Y_FALL_INC_DELAY = 0; // incr. delay (ps)
endcomponent // AND2_X1
```

- Generic RIIF model for a gate.
- By default assume nominal VCC and temperature.
- Default activity factor is unknown.
- BTI effect is modelled as incremental delay on each timing arc

REFINING LIBRARY GATES TO INSTANCES

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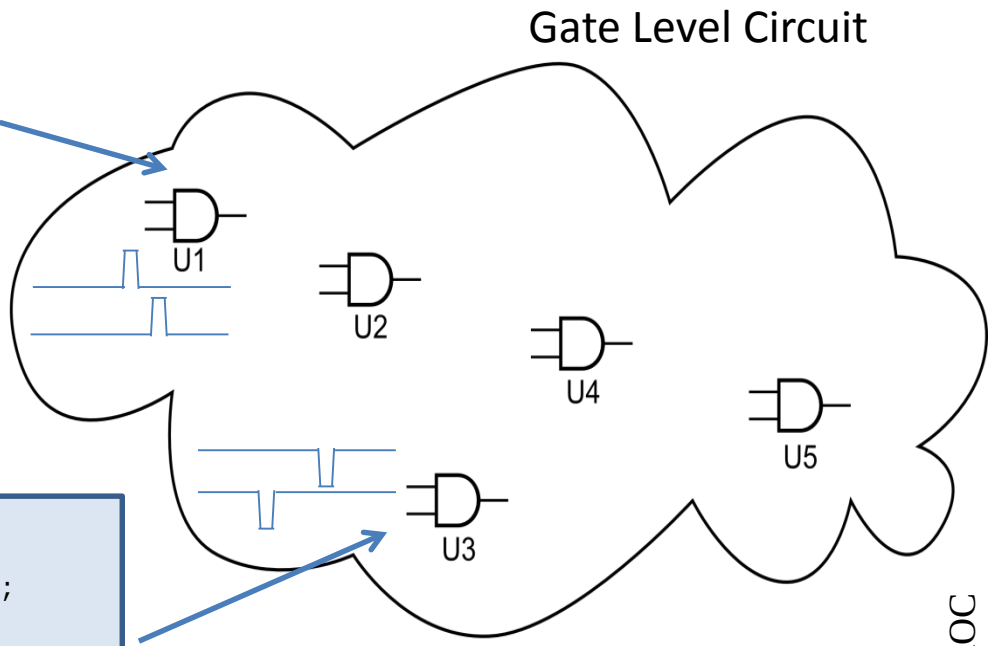
RIIF models refined on per Instance basic

```
component U1 extends AND2_X1;
   parameter VCC = 0.97;
   parameter TEMP = 85;

   parameter A_INP_ACTIVITY = 0.1;
   parameter B_INP_ACTIVITY=0.1;
   parameter Y_OUT_ACTIVITY=0.0;

endcomponent // U1
```

```
component U3 extends AND2_X1;
   parameter VCC = 0.91;
   parameter TEMP = 95;

   parameter A_INP_ACTIVITY = 0.9;
   parameter B_INP_ACTIVITY=0.9;
   parameter Y_OUT_ACTIVITY= 0.9;

endcomponent // U3
```



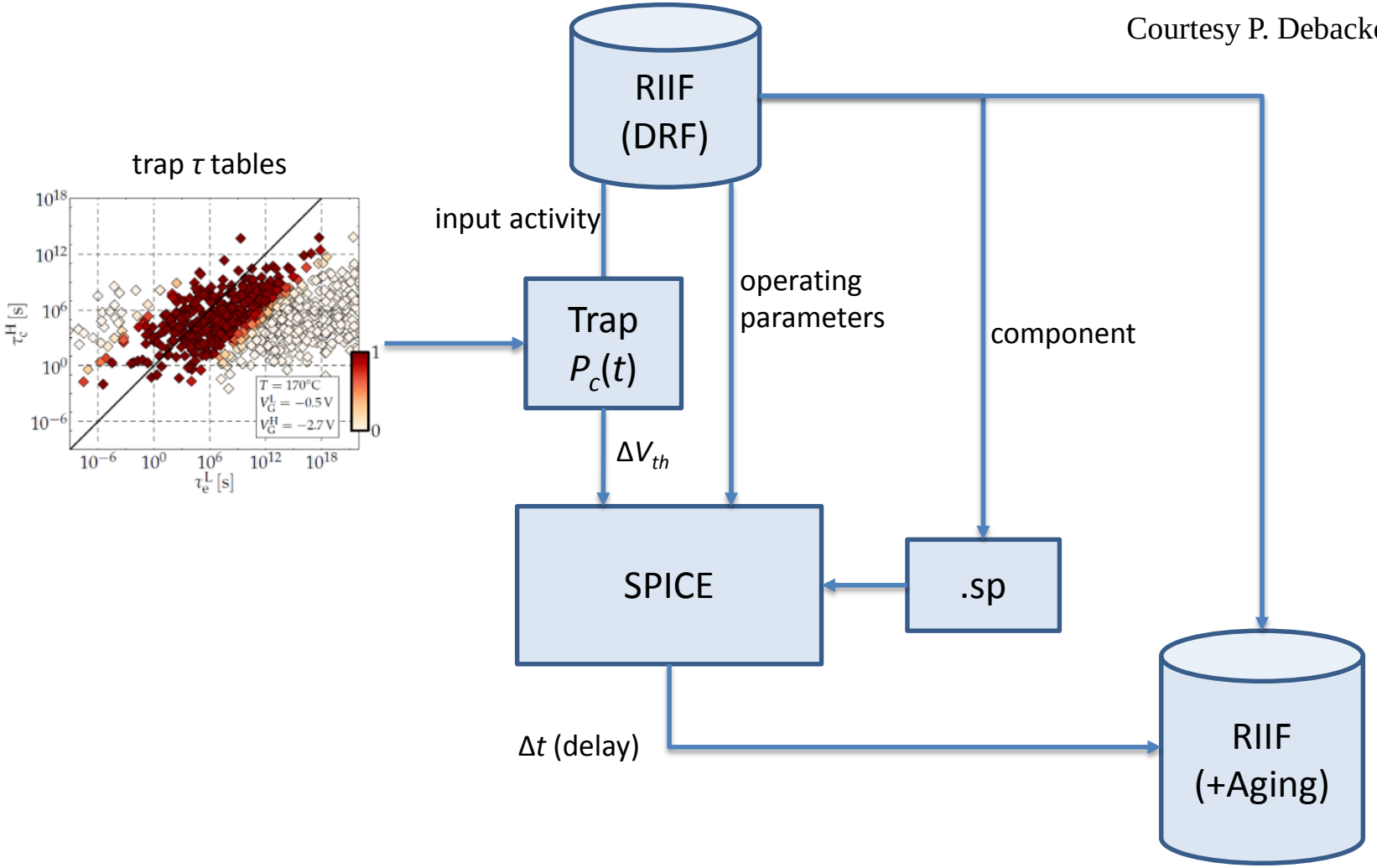
- By simulating gate-level circuit, activity factors for each instance are extracted
- Each instance's unique characteristics form a DRF = **D**elay **R**equest **F**orm

Courtesy E. Costenaro, iROC

INSERTING DEGRADATION

ESSCIRC ESSDERC 2015

Courtesy P. Debacker, imec

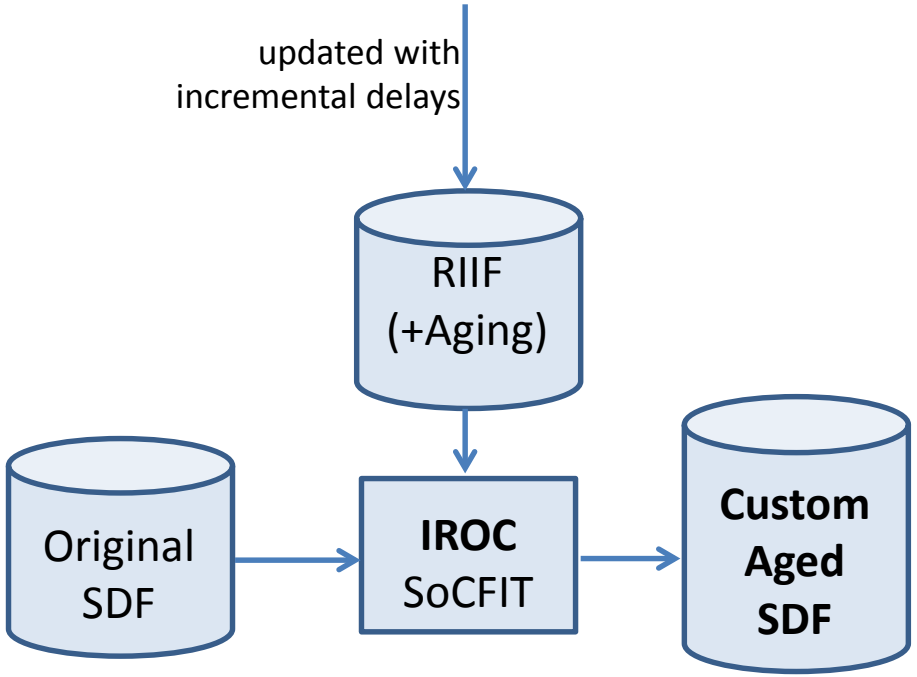


- In practice, more elaborate spice-level preprocessing schemes are used to reduce runtimes
- **In small devices with a handful of defects, variability is naturally generated**

WORKLOAD-SPECIFIC AGING INFORMATION PROPAGATED INTO THE FLOW

ESSCIRC ESSDERC 2015

Courtesy E. Costenaro, iROC

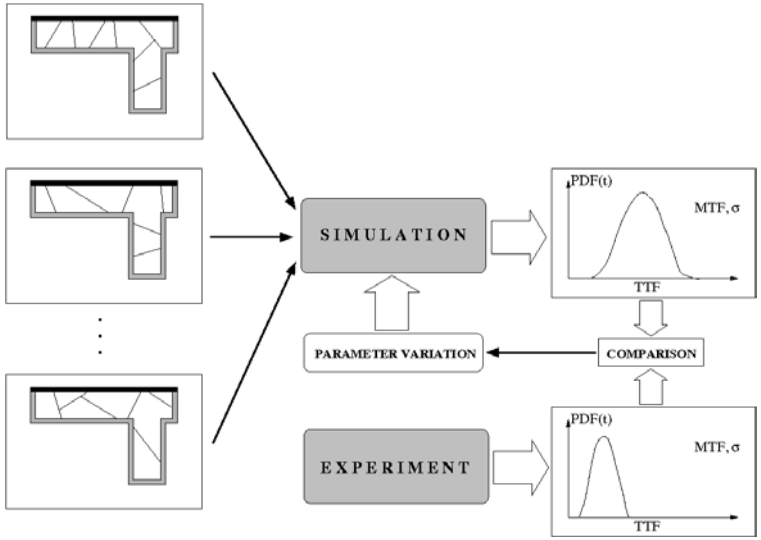


- Simulating gate-level circuit, activity information for each instance is extracted
- Also includes generating per-instance voltage and temperature information (OFFIS)
- Each instance's unique characteristics form a
  - DRF = **D**elay **R**equest **F**orm (in RIIF format)

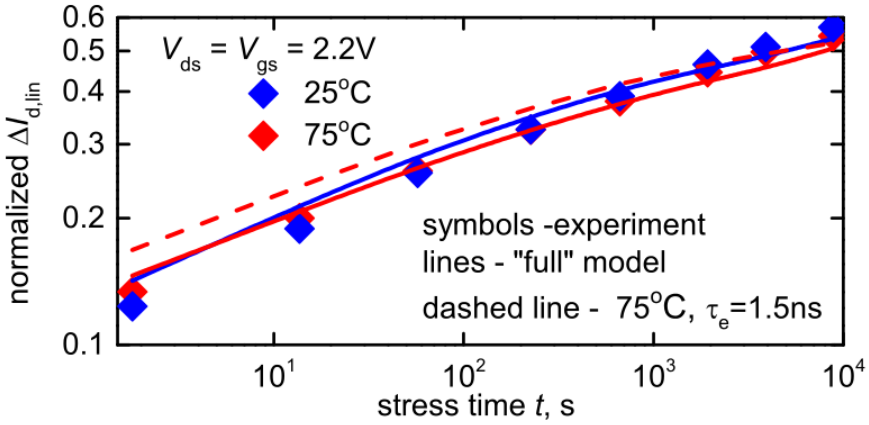
ALSO CONSIDERED IN MORV

- Electromigration
- Hot-carrier degradation

…



Ceric *et al.*, SISPAD 2015



Tyaginov *et al.*, EDL, submitted

SUMMARY

ESSCIRC ESSDERC 2015

EU project MoRV hierarchy has been reviewed, allowing inserting aging and variability into large-scale simulations

PARTNERS

ESSCIRC ESSDERC 2015

Partially funded by EU Project