André Juge, STMicroelectronics

ESSCIRC ESSDERC 2015

WORKSHOP "VARIABILITY – FROM EQUIPMENT TO CIRCUIT LEVEL"

Variability at all levels – A Challenge for Semiconductor Industry

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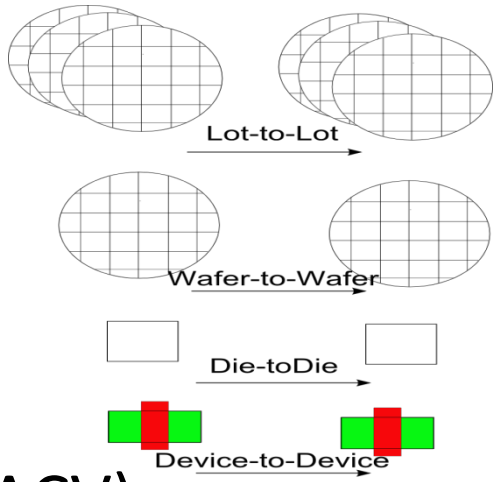
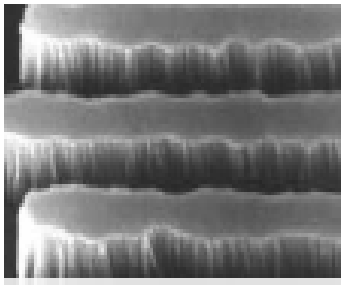
ABSTRACT

- Presentation highlights Research and Industry effort to mitigate impact of multi-level Variability sources in order to enable design of high yield manufacturable circuits
- Variability scope is wide; samples of techniques among Process variability reduction, DFM, Electrical Characterization, Compact Statistical Modeling, Design methodology are shown for illustration.
- New challenges are identified

OUTLINE

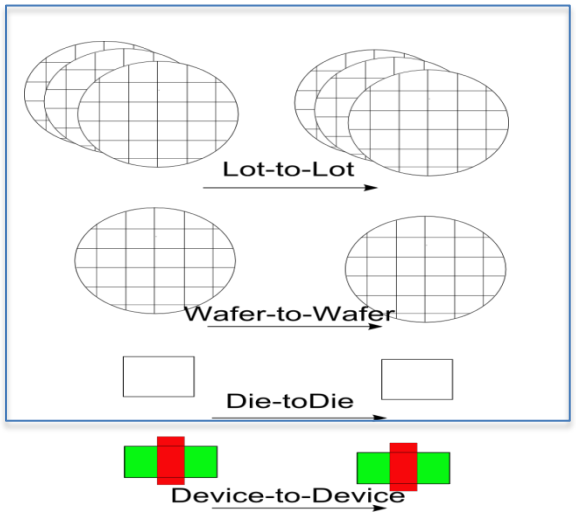


1. Introduction: Variability sources
2. Design for Manufacturing
3. Global Process Variations (Interdie)
4. Local Across Chip Variations (Intradie, ACV)
5. Local Systematic Variations (Local Layout Effects, LLE)
6. Local Statistical Variations (Mismatch)
7. Circuit simulation requirements
8. Conclusion



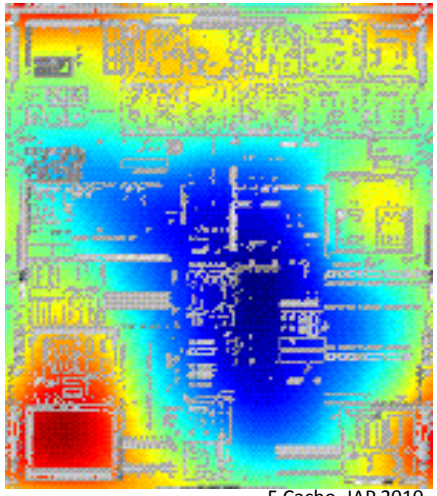
VARIABILITY SOURCES

Global Process(Interdie)



Across Chip (Intradie)

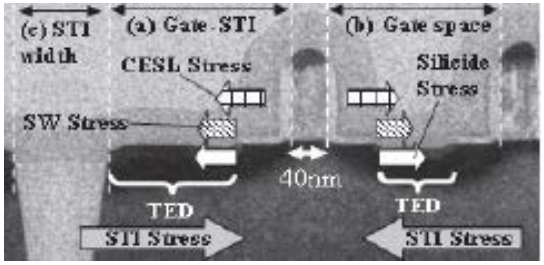
Systematic (mm-cm)



F.Cacho, JAP 2010

Local Layout Effect

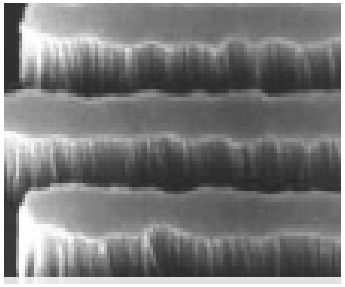
Systematic (0.1-1um)



[H.Tsuno, VLSI 2007]

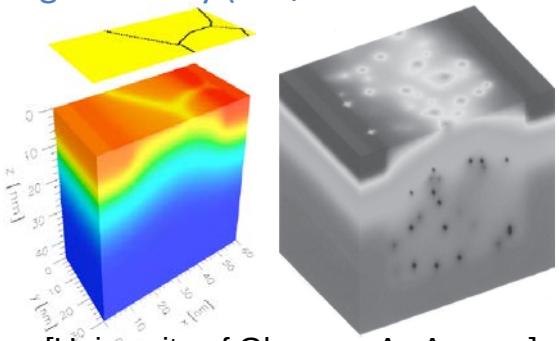
Local Random

Line edge roughness (nm)



Channel dopants (A)

PolySi granularity (nm)



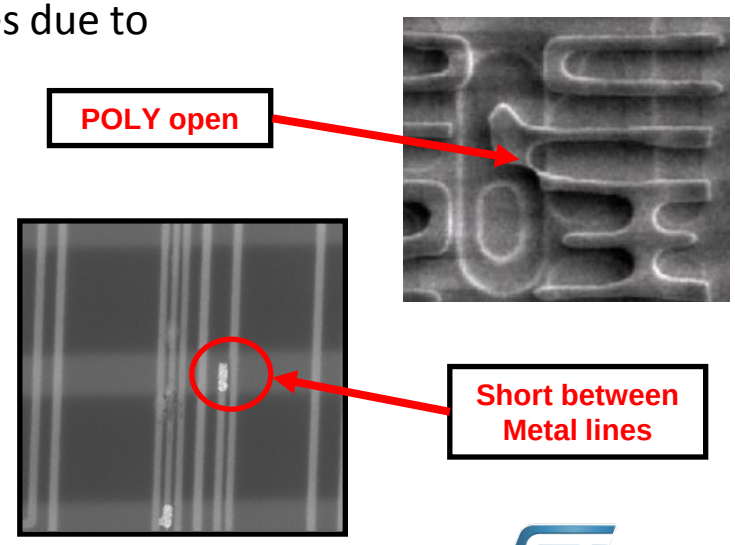
[University of Glasgow, A .Asenov]

DESIGN FOR MANUFACTURING (DFM)

- DFM is about Yield.
  - "DFM is a set of methodologies used to guide the design process so that product fabrication will have low cost, high conformance quality, low manufacturing ramp-up time and short time to market"

- DFM rules and models allow to minimize yield losses due to
  - Systematic defects
    - Product/process ramp-up
  - As well as random defectivity
    - Volume production

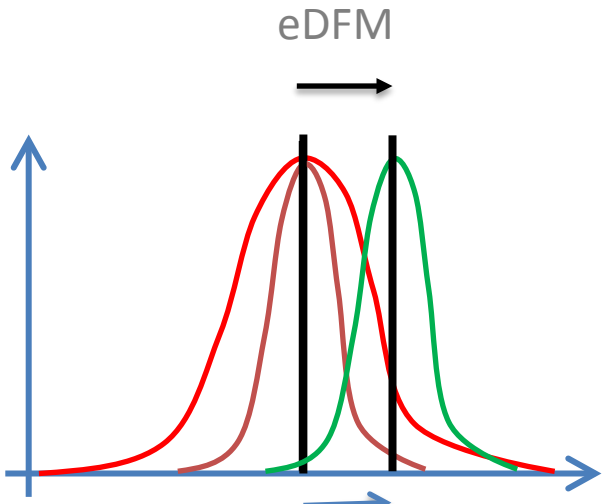
- DFM is indeed about chip functional yield …
  …. but not only…



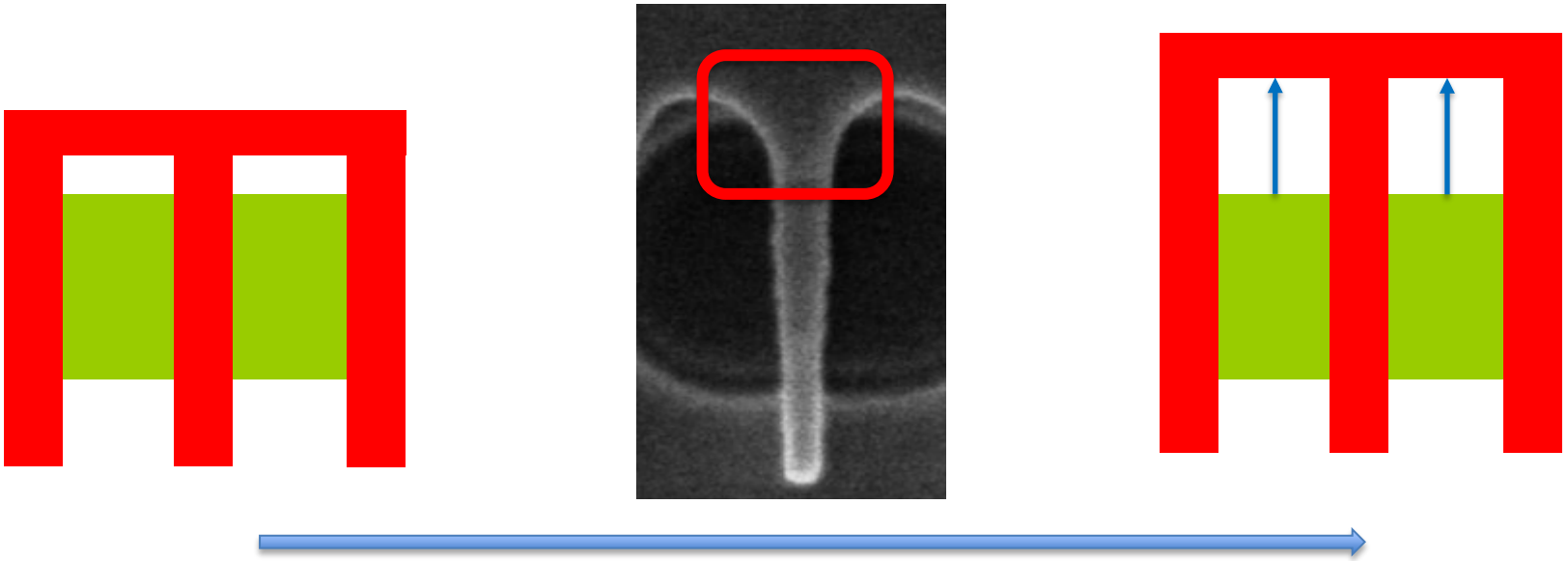
DFM VS PERFORMANCE VARIABILITY

- At nanometer technologies, process variability has become one of leading causes of chip yield loss and delayed schedules
  - designers must be aware of how complex manufacturing steps lead to device and interconnects performance variability
  - variability is to be accounted for in various design operation modes, power states/domains, leading to more complex and longer design cycles

- "electrical DFM" (eDFM) rules to
  - Reduce impact of process variability
    - Reduction of circuit performance spread
    - More dice with maximum performances
  - Verify layout design vs accurate simulation validity domain
    - Minimize discrepancy bw simulated /measured circuit performance



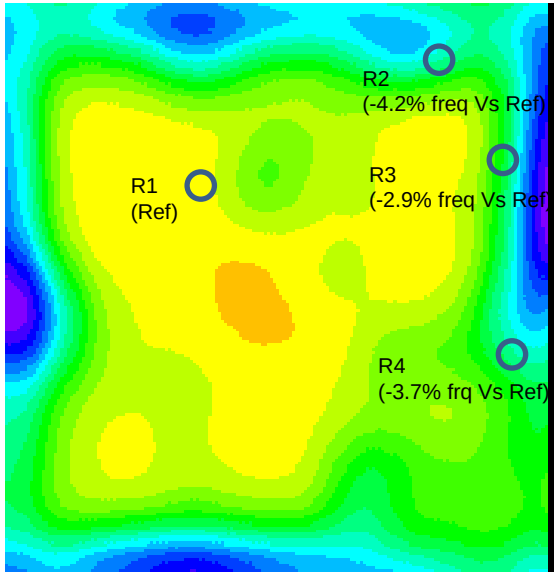
ELECTRICAL DFM VS PERFORMANCE VARIABILITY

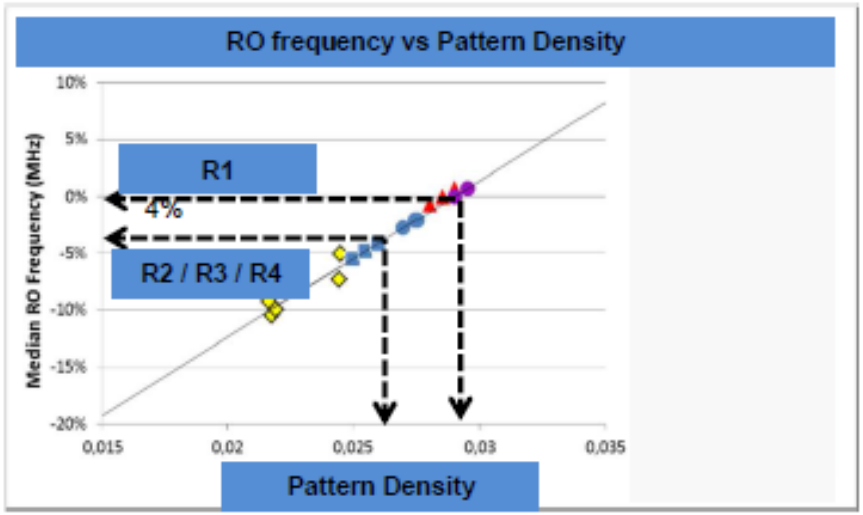


Improved channel W control
Spice model compliance (Nominal + Variations)

- Small scale eDFM example. eDFM minimizes impact of process variability on circuit performance variations and maximize CAD/Silicon correlation

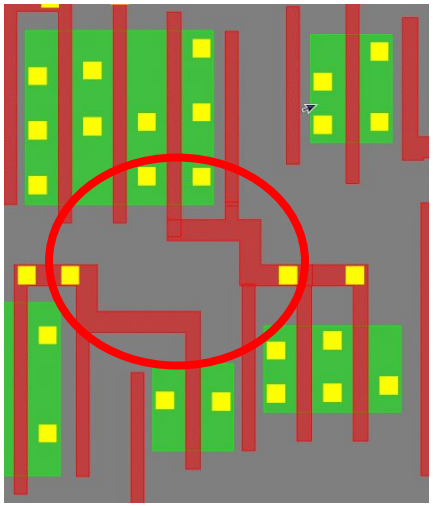
ELECTRICAL DFM VS PERFORMANCE VARIABILITY

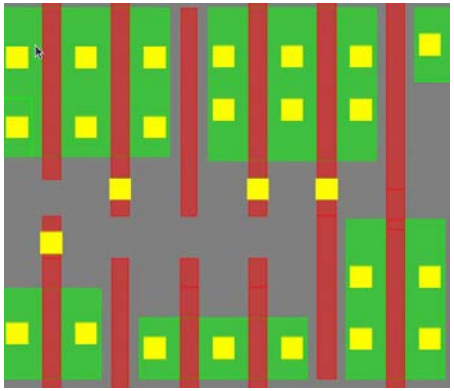




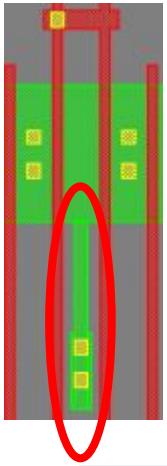
- Large scale eDFM example
  - Large variations in Pattern density lead to systematic acrosschip variations (ACV)
- Can be mitigated by layout regularity
  - Cell level (regular gate pitch, limited set of geometries,…)
  - Chip level (density/gradient design rules, smart dummy devices,…)

ELECTRICAL DFM VS CAD ACCURACY





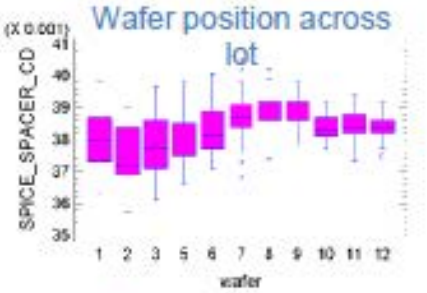
Improved CD control
Spice model accuracy

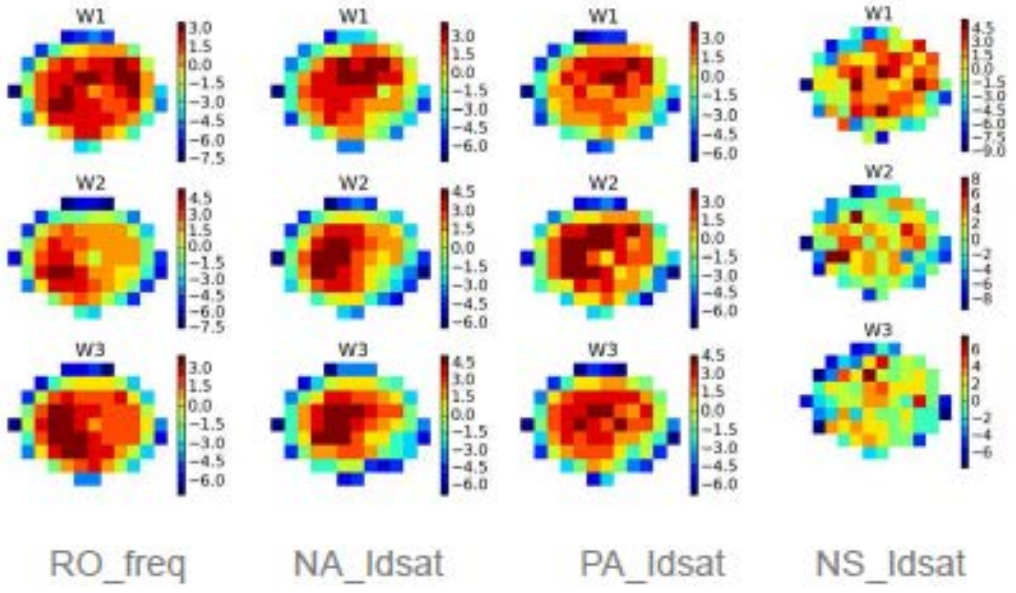


Reduced IR-Drop
PEX tool accuracy

- Need to verify layout design vs accurate simulation validity domain
  - For specific layout situation simulation may not be fully accurate
  - Allowed by DRC, nevertheless can be restricted by eDFM rules

GLOBAL PROCESS VARIABILITY



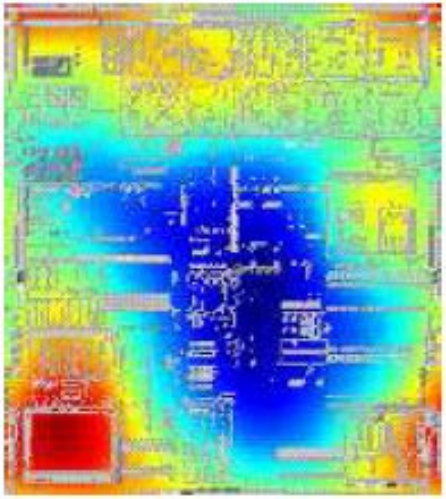


- Intrawafer die/die variations tend to dominate Global variations
- Electrical impact similar for RO delays and Mosfet currents; can be put in evidence with properly design structures [GC Castaneda ICMTS 2012]

ACROSS CHIP VARIATIONS

Anneal Temperature profile

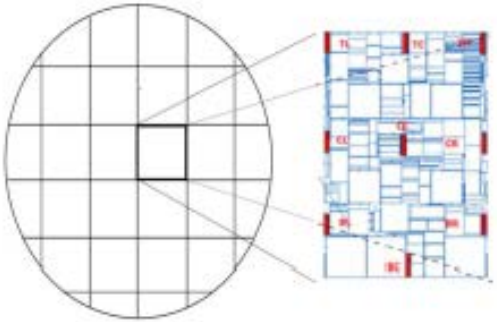
Anneal Temperature profile



[F.Cacho, JAP 2010]

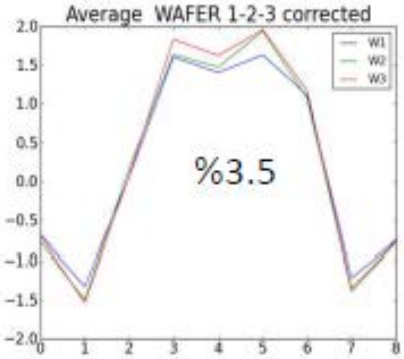
Within die sampling

(9 positions)



Within die variations

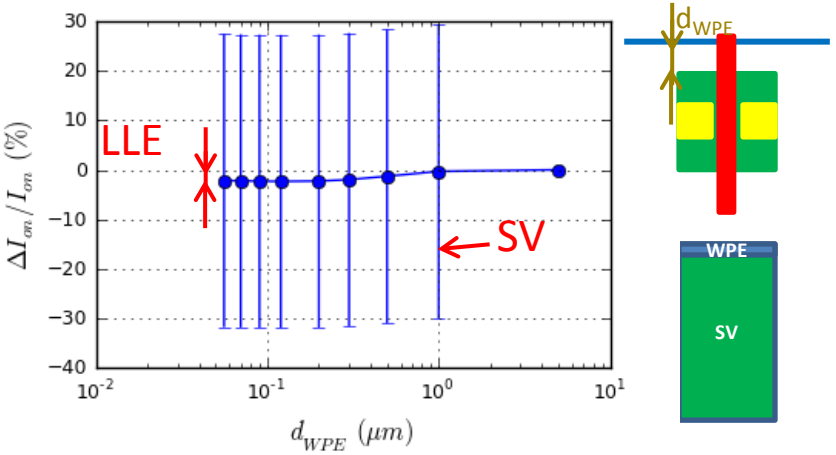
(9 positions, 3 wafers)



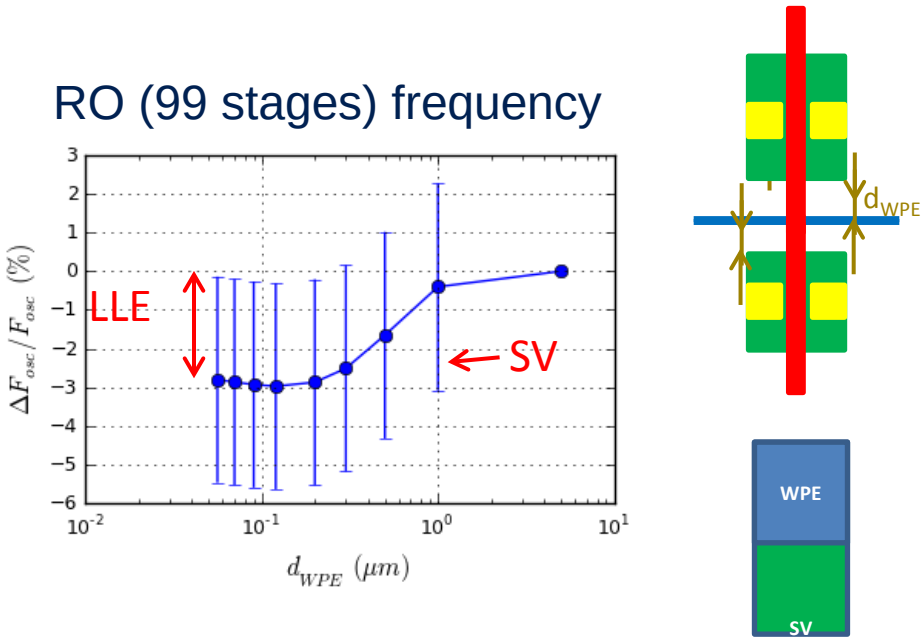
- ACV may originate from pattern density gradient within chip
- Experimental evidence with ROs , thanks to SV averaging effect
- Mitigated with smart dummy patterns to reduce density gradients

LOCAL VARIATIONS: SYSTEMATIC VS STATISTICAL

Transistor I_{on}



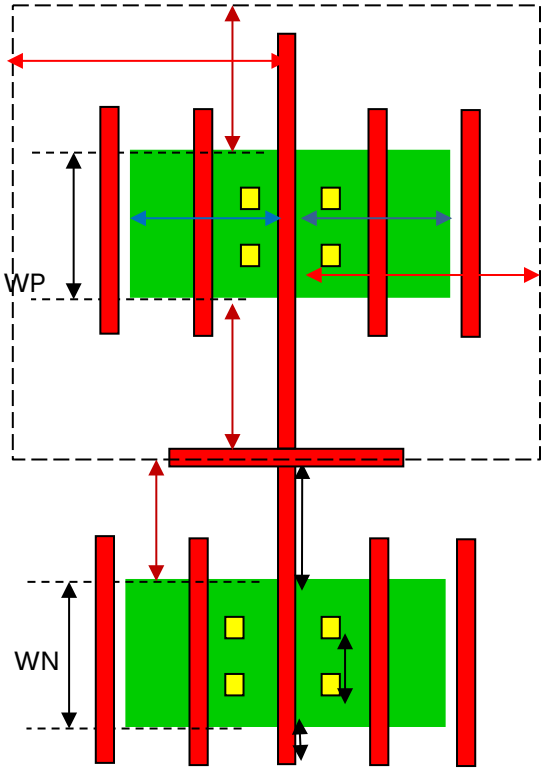
RO (99 stages) frequency



- Transistor level : random variations (SV) dominant for devices at critical dimensions
- Circuit level: random variations averaged, and systematic variations (LLE) revealed
- LLE methodology: characterization, compact modeling, post-layout extraction tool

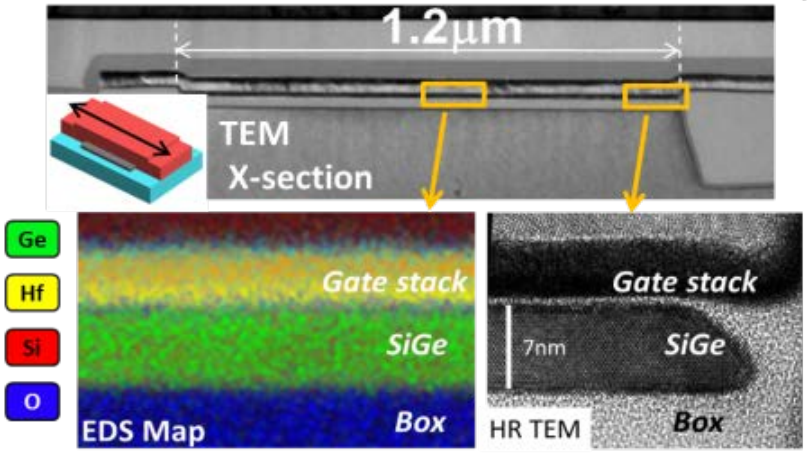
LOCAL SYSTEMATIC VARIATIONS (LLE)

Layout effect	Root cause	Critical distance	Electrical Parameters	Instance Layout par.
Well Proximity (WPE)	Deep Well implants	>1um	Vt, Mu, Kb	3
LOD/STI	STI Stress S/D SiGe (P) **SiGe channel (N)**	1um	Vt, Mu	> ~6
Gate Spacing Nb of Fingers	CESL/DSL Stressor	~1 um	Vt, Mu	>~6
S/D Contacts Nb & Position	CESL/DSL Stressor	1um	Vt, Mu	>~4
Distance to Stress Liner	DSL	1um	Vt, Mu	>~4
Active corner	Litho & Etch rounding	Local	Weff	~4
Gate corner or endcap	Litho & Etch rounding	Local	Leff	~4

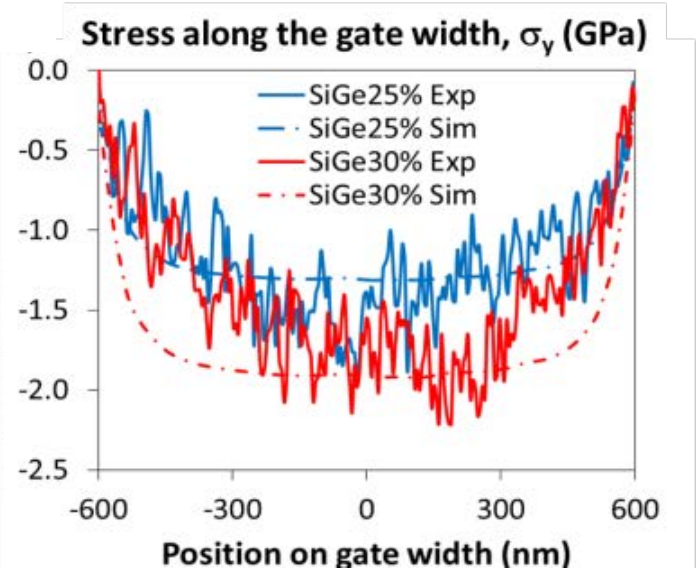


- LLE are technology dependent
- For each W/L instance, a bunch of layout dependent effects interplay
- Risk of inaccurate design reduced with Layout regularity and LLE model accuracy

LLE STUDY CASE (UTBB FDSOI SI-GE CHANNEL)



[B.De Salvo *et al.*, IEDM 2014]

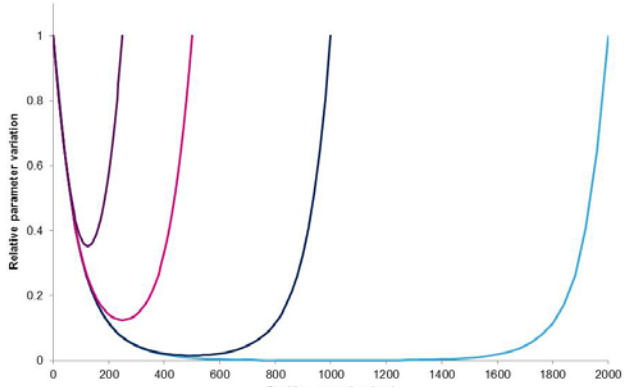


- Ge induces compressive strain in SOI film
- Strain tends to relax at the edges of the film

LLE STUDY CASE (UTBB FDSOI SI-GE CHANNEL)

$$P(x, L_{act}) = P_{full\ strain} + \Delta P \times g(x, L_{act})$$

$$\Delta P = P_{edge} - P_{full\ strain}$$



$g(x, L_{act})$ for $\lambda = 120nm$ and $\alpha = 3$

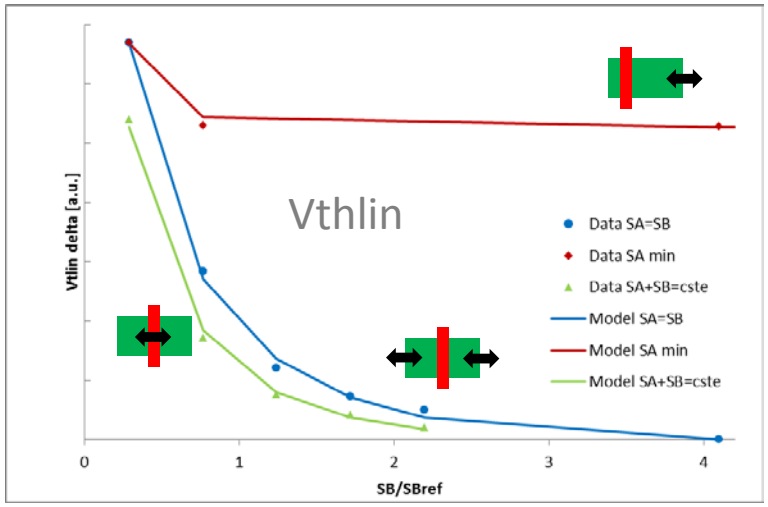
$$g(x, L_{act}) = 1 - \left[\frac{2}{(1 - e^{-x/\lambda})^{-\alpha} + (1 - e^{(x-L_{act})/\lambda})^{-\alpha}}\right]^{1/\alpha}$$

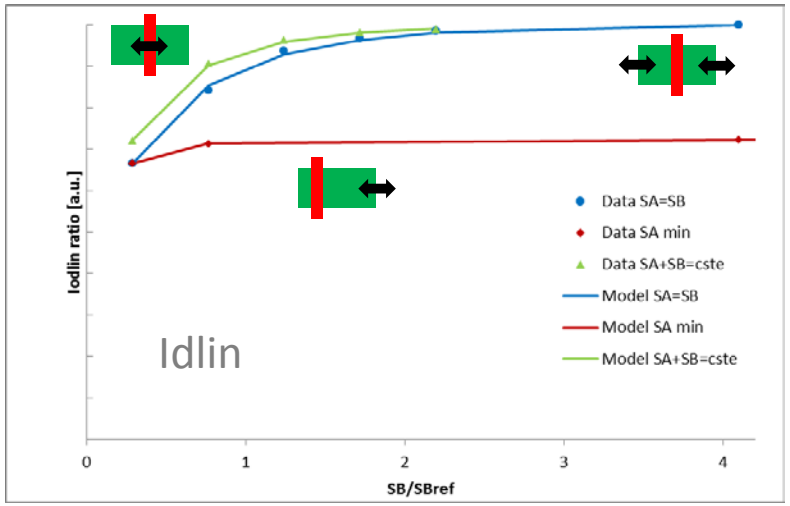
λ and α are model parameters

[T.Poiroux & al., MOSAK 2015 Q1]

- Compact model formulation for Electrical Parameters P inspired from Stress profile
- Impacts on Vfb, DIBL, Mobility, and Velocity saturation accounted for in UTSOI2 model

LLE STUDY CASE (UTBB FDSOI SI-GE CHANNEL)



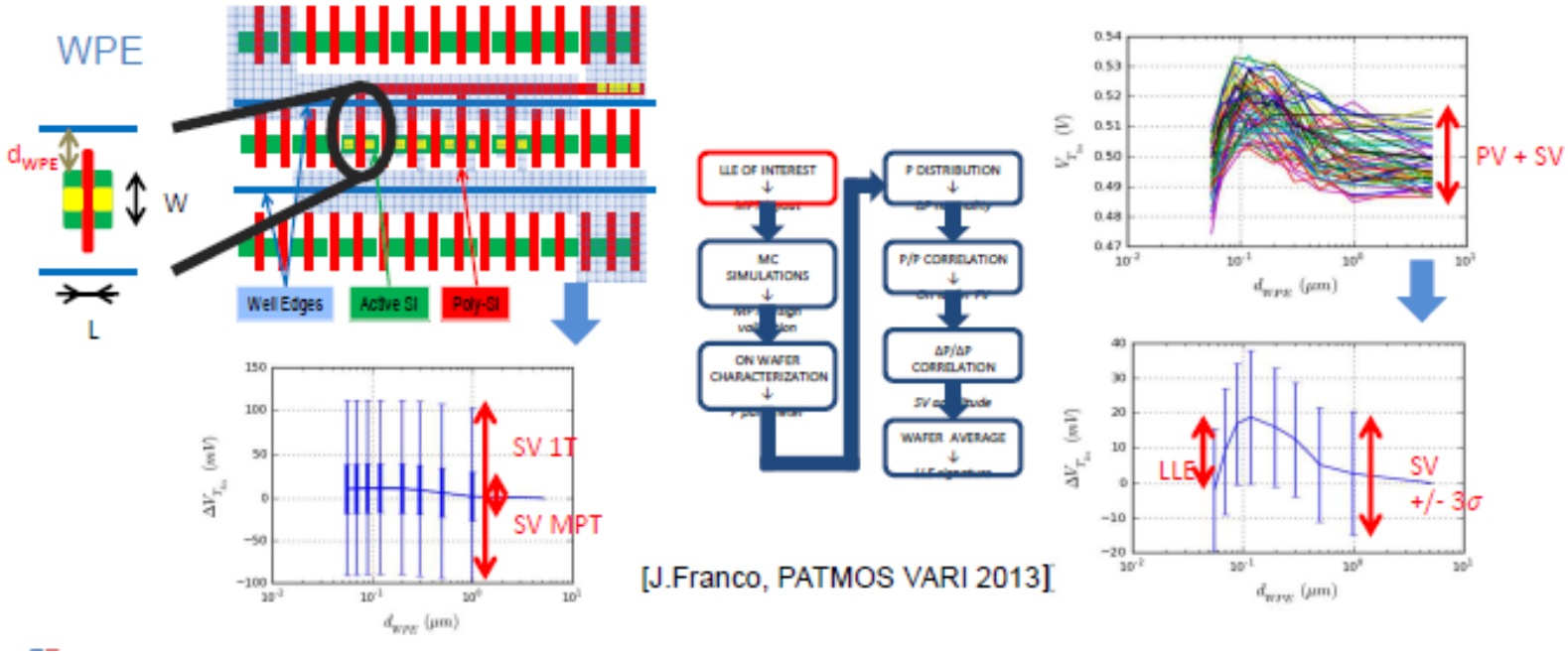


$$P(SA,SB) = P(SA_{ref},SB_{ref}) + \Delta P\left(g(SA,SB) - g(SA_{ref},SB_{ref})\right)$$

[T.Poiroux & al., MOSAK 2015 Q1]

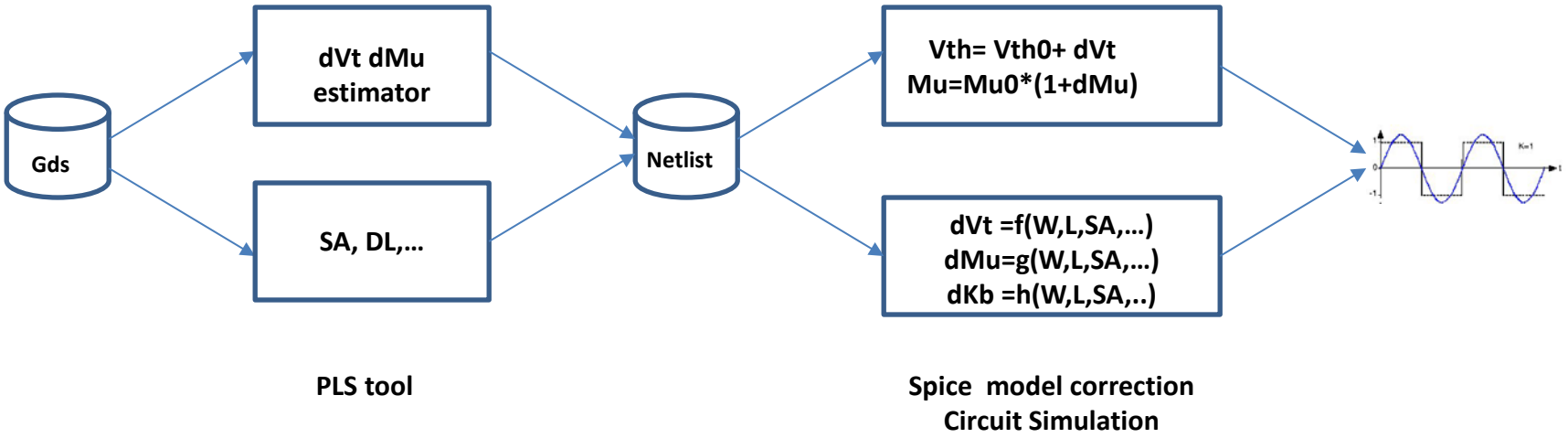
- SA/SB effect model validation

LLE CHARACTERIZATION METHODOLOGY



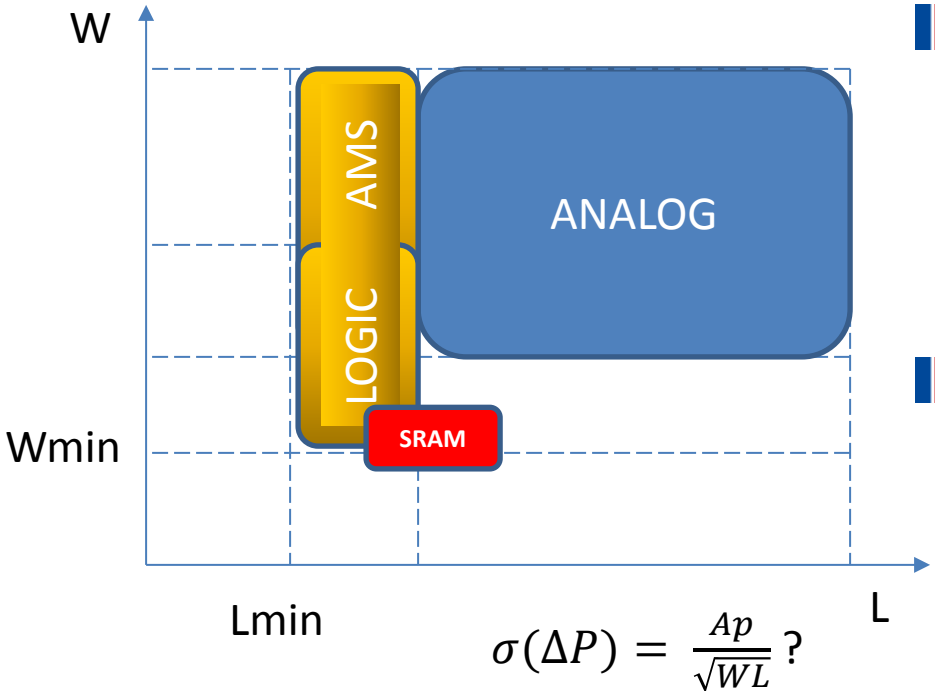
- Characterization methodology revisited for transistor LLE
- Test structure, data processing in presence of PV and SV, LLE signature

LLE DESIGN FLOW



- LLE simulation flow: implementation shared bw Post-Layout extraction and Compact Spice modeling

LOCAL STATISTICAL VARIATIONS (SV)

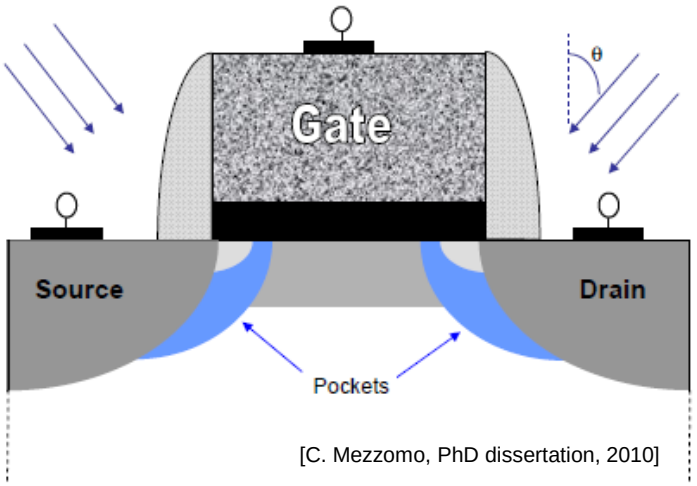


$$\sigma(\Delta P) = \frac{Ap}{\sqrt{WL}} \; ?$$

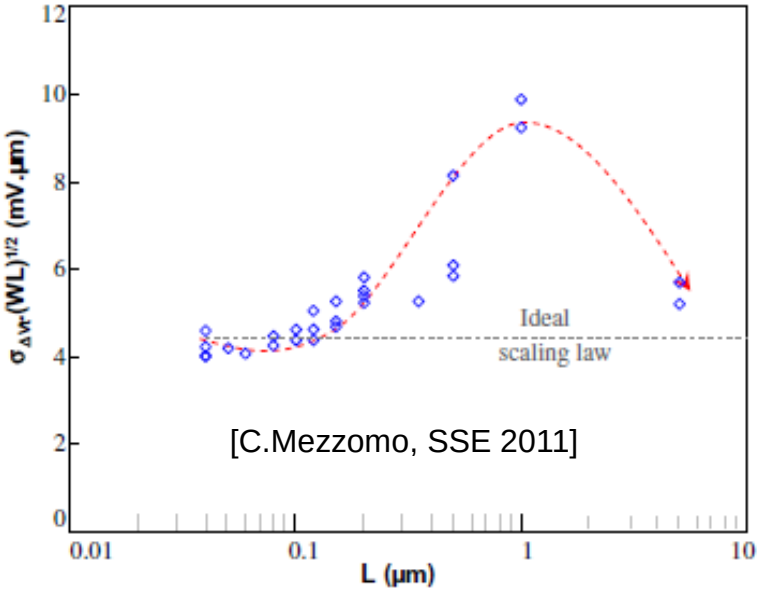
- SV scaling driven by SRAM
  - VDDmin
  - Minimization of SV sources and Device sensitivity to SV
- SV impacts AMS-Analog
  - Current Mirrors accuracy
  - Need to investigate SV scaling on W and L

- Pelgrom model is nice metric, but does scaling apply throughout Design Space?
- Which sources are present and which electrical parameters are impacted?

LOCAL STATISTICAL VARIATIONS: BULK PLANAR CMOS



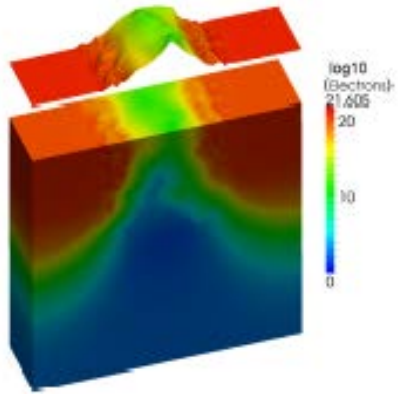
[C. Mezzomo, PhD dissertation, 2010]

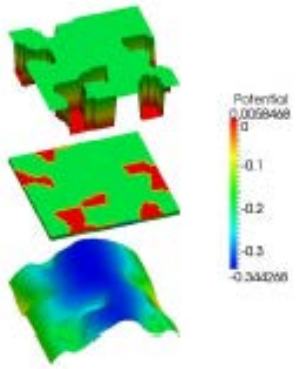


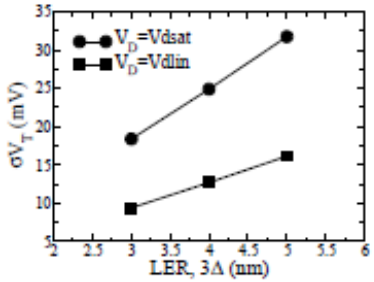
[C.Mezzomo, SSE 2011]

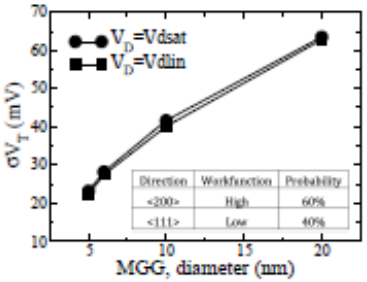
- 45nm devices exhibit AVT degradation for large L
- Model improved for AMS circuit design assuming Channel doping gradient

LOCAL STATISTICAL VARIATIONS: BULK PLANAR CMOS



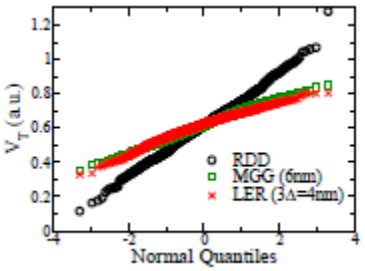


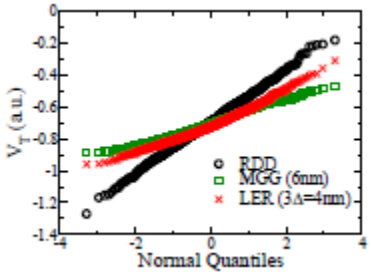




σV_T [mV]	n-MOSFET		p-MOSFET	
	V_{Dsat}	V_{Dlin}	V_{Dsat}	V_{Dlin}
RDD	49.8	44.4	54.4	42.3
LER (3Δ=4nm)	24.9	12.7	33.3	12.8
MGG (6nm)	28.2	27.4	25.3	24.7
Combined	63.2	52.7	68.7	52.1
Measurement	63.4	55.5	69.5	54.0

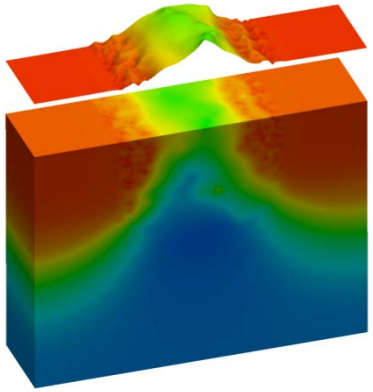
[X.Wang &al, Univ. Glasgow, EDL 2011]

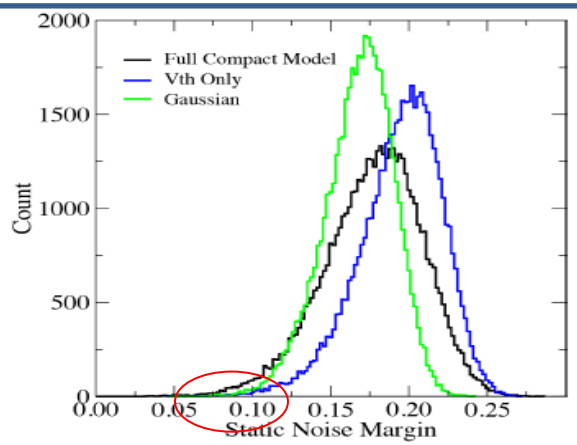


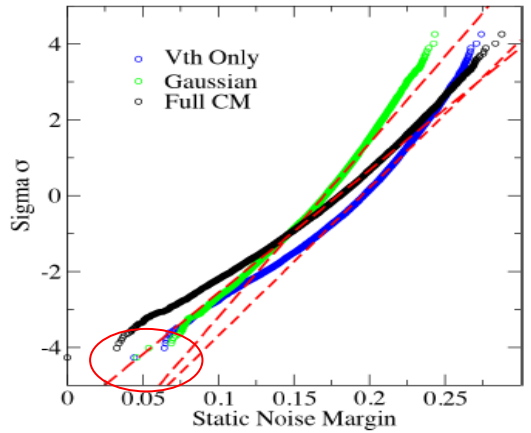


- SV sources well identified and contributions quantified (RDD dominant)
- SV models validated for 32nm devices (ENIAC Modern project support)

LOCAL STATISTICAL VARIATIONS: SRAM CASE



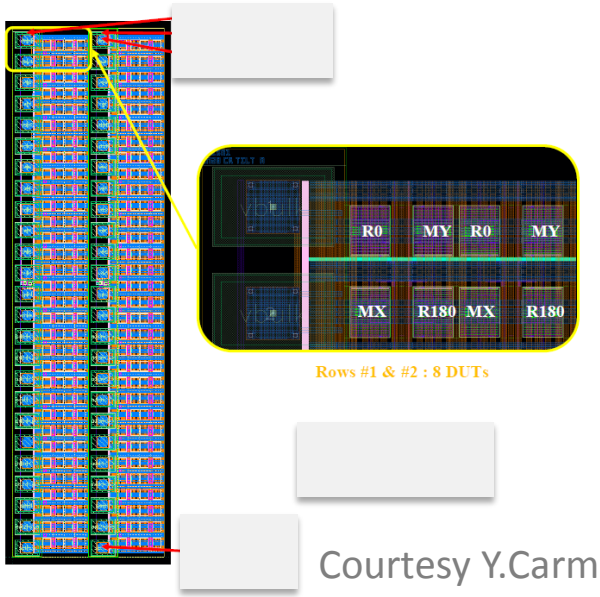




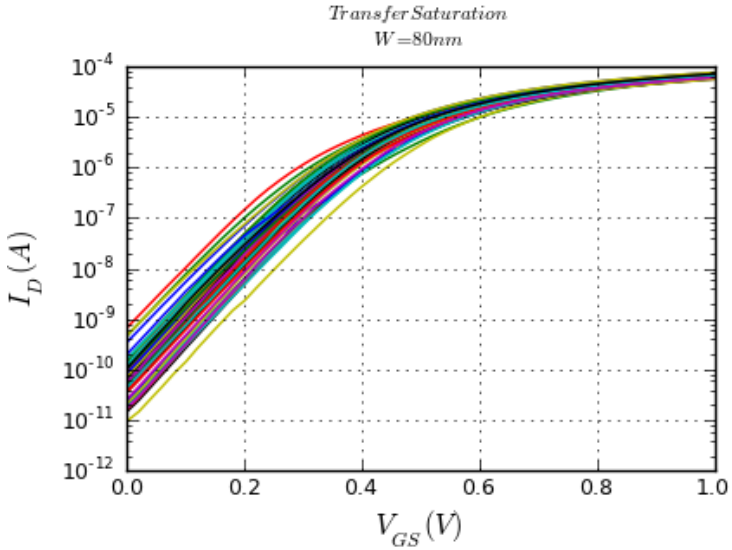
Monte-Carlo TCAD Device to SRAM circuit simulation chain [P.Asenov, PATMOS VARI 2011]

- Importance of accurate SV models has been demonstrated
- In particular, assumption of Vth-only and Gaussian-only PDF distribution may fail
- Full statistical compact models for accurate estimates of SRAM SNM

LOCAL STATISTICAL VARIATIONS: CHARACTERIZATION



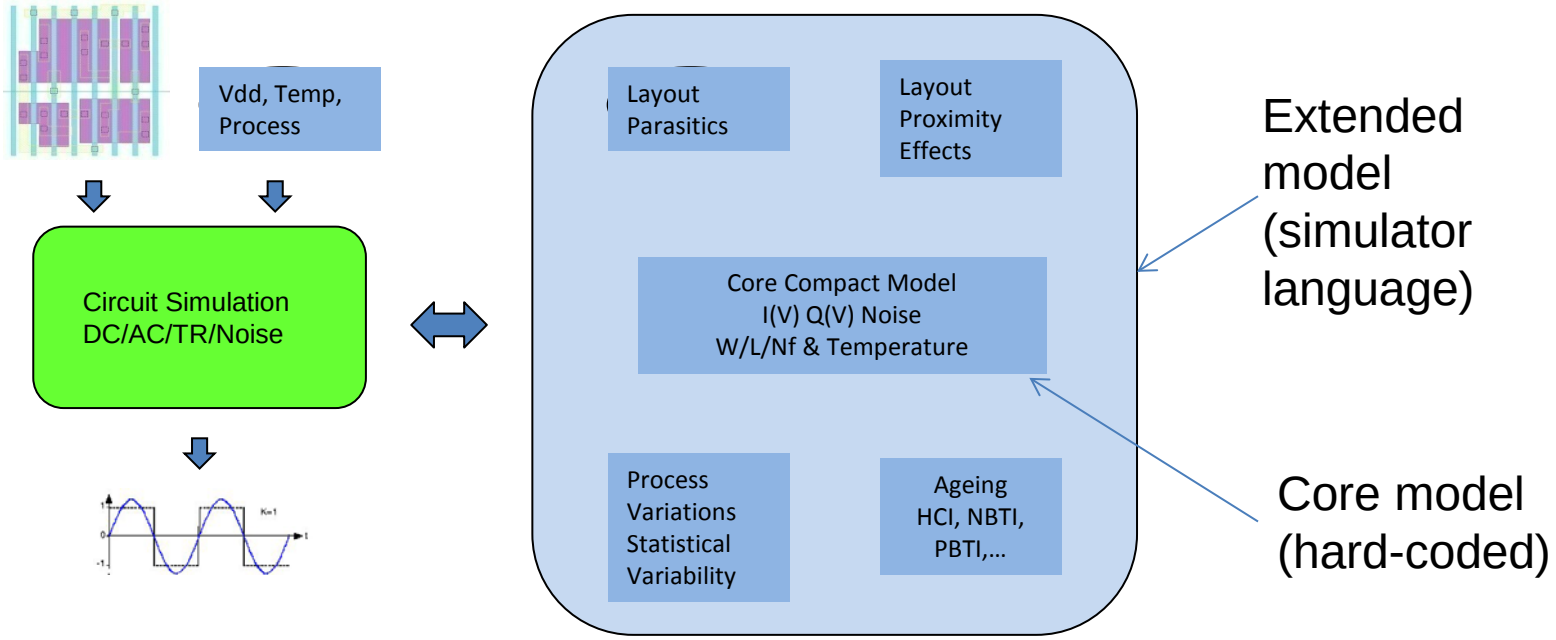
Courtesy Y.Carminati



Courtesy J.Franco

- Characterization methodology revisited
- Transistor pairs suited for standard mismatch figures characterization
- Addressable transistor arrays suited for statistical I(V) characterization (Vth, DIBL, SS, Idsat, Ioff,…) and statistical compact Spice model extraction

CIRCUIT SIMULATION REQUIREMENTS



- Accurate core models vs Bias, Geometry, Temperature
- Accurate model extensions for predictivity of PV, SV, LLE, and Ageing impact
- Efficient Circuit simulation methods and integrated design flow

CONCLUSION

- Variability has multiple contributions of different nature from technology and device.
- Those effects must be addressed concurently by dedicated developments in Technology, Characterization, Modeling, CAD tools, and Circuit design.
- Effective collaboration between those players is must-have to enable emergence of high volume high yield IC products in time with respect to market needs.
- Comprehensive understanding of variability at all-levels, variability reduction techniques, model accuracy, predictivity of statistical simulation tools, and design flow efficiency, are key.

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