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ESSCIRC ESSDERC 2015

VARIABILITY-AWARE PROCESS SIMULATION IN SUPERTHEME

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OUTLINE

1. Introduction
2. Software components
3. Example: through-silicon via (TSV) processing
4. Example: simulation of spacer patterning for FinFET structure
5. Conclusions

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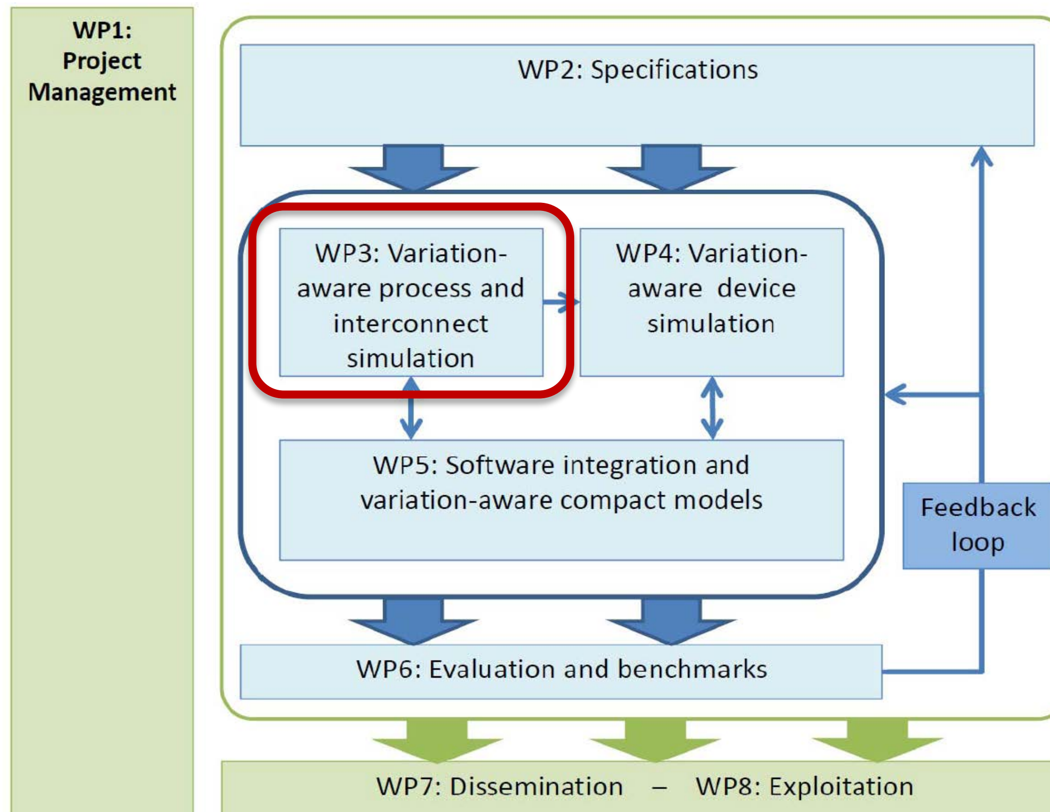
INTRODUCTION

INTRODUCTION – GOALS AND STRATEGY

- Quantification of process variability at its source at equipment level
- Variation-aware simulation of the processes for the fabrication of active semiconductor devices and interconnects
- Modeling of performance and reliability of interconnects and their dependence on the fabrication process
- Proprietary software of the partners IISB and TUW as well as third-party software are used, extended, and integrated

INTRODUCTION – PROJECT CONTEXT



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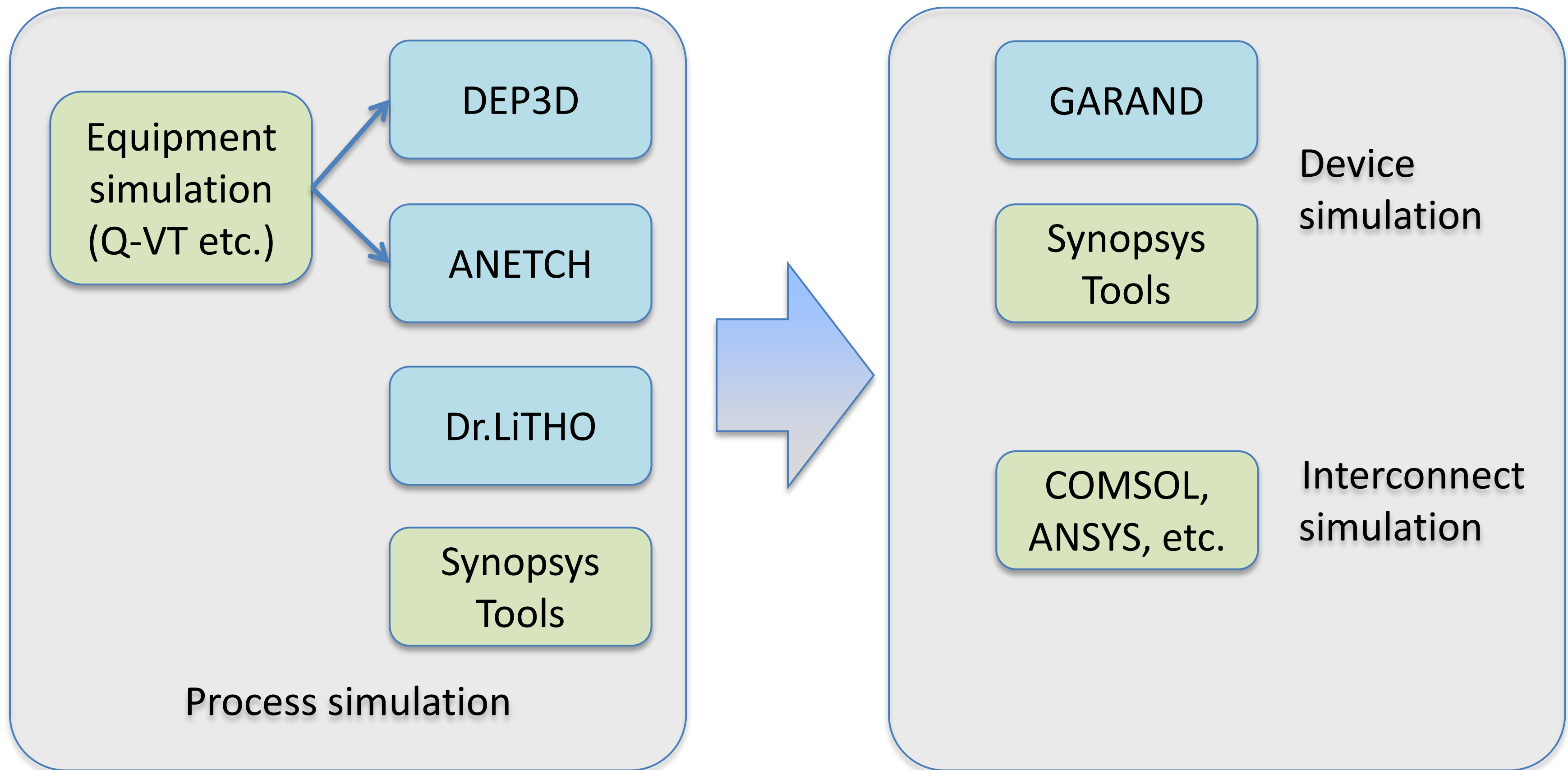
SOFTWARE COMPONENTS

SOFTWARE COMPONENTS



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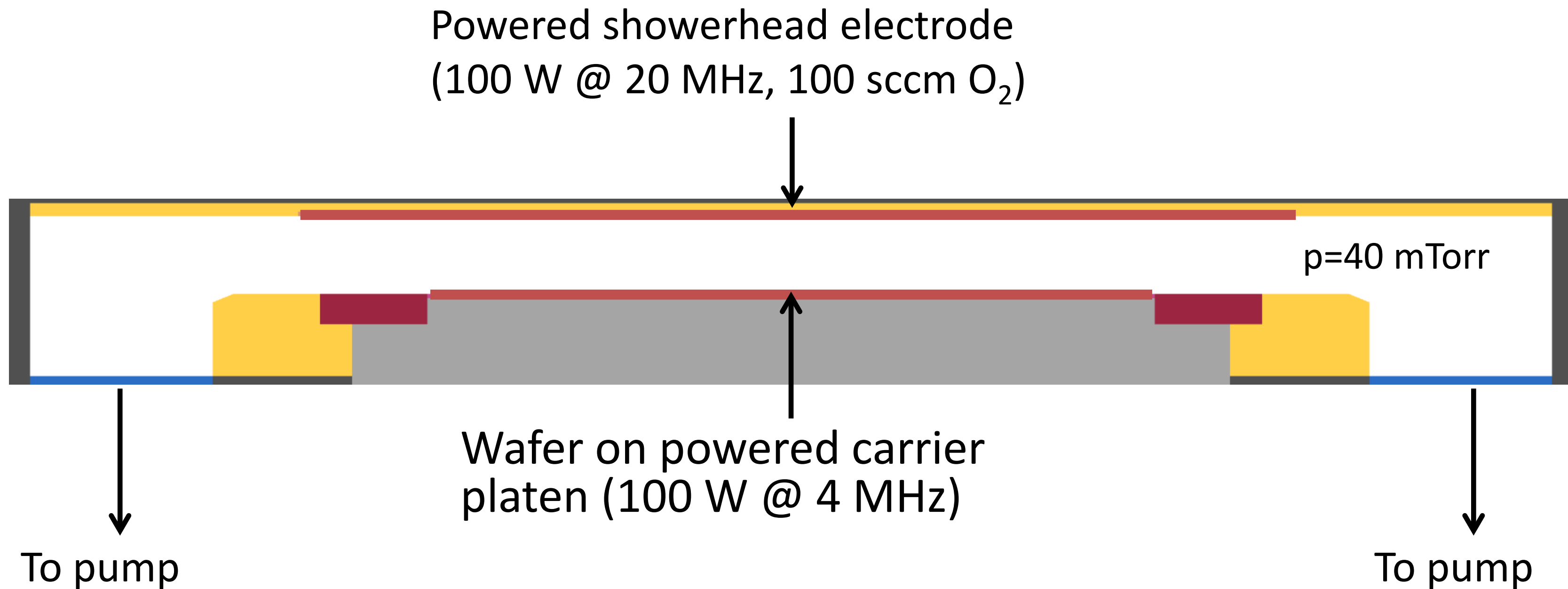
EXAMPLE: THROUGH-SILICON VIA (TSV) PROCESSING



PLASMA-ENHANCED CHEMICAL VAPOR DEPOSITION (PECVD) OF SIO2 FROM TEOS AS PART OF TSV PROCESS

Simulation of PECVD capacitively coupled plasma (CCP) reactor using the software Q-VT (Quantemol), TEOS assumed to be saturated

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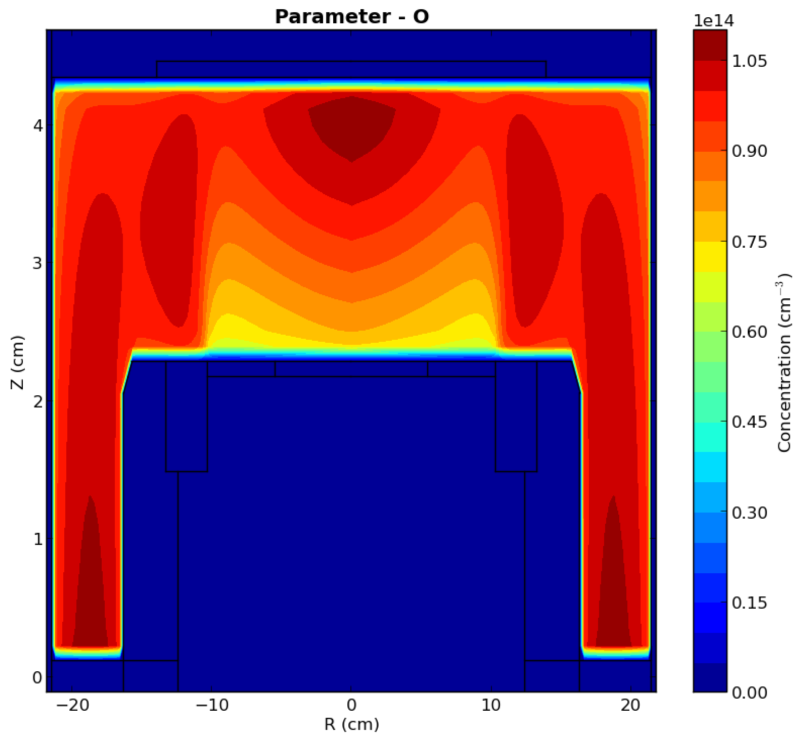
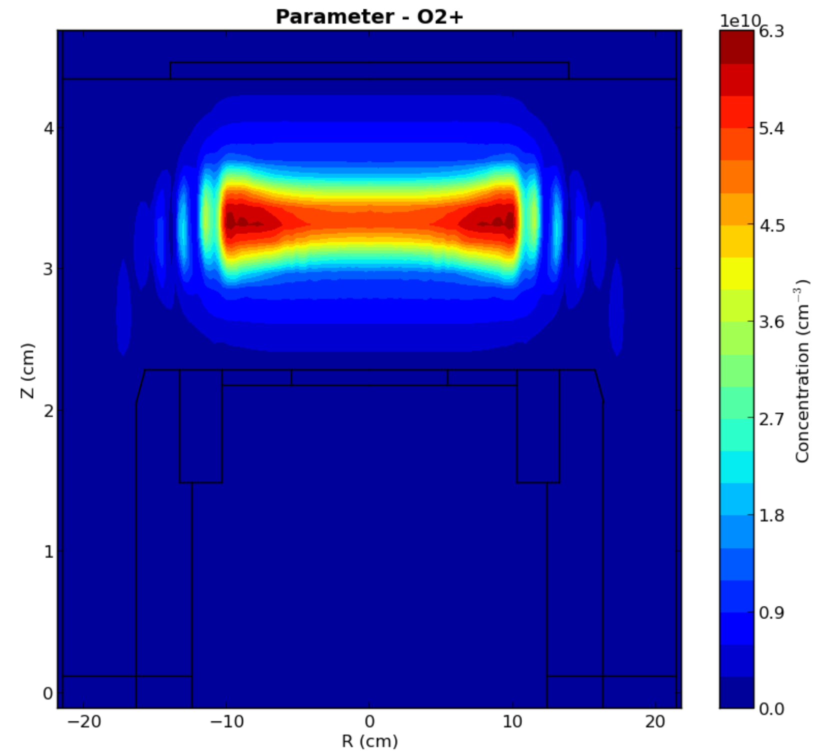
Neutrals (O)



Ions (O_2+)



Example for concentration of neutrals (O) and ions (dominant ion species is O_2+) in a CCP reactor (figure aspect ratio is scaled)

SUPERTHEME

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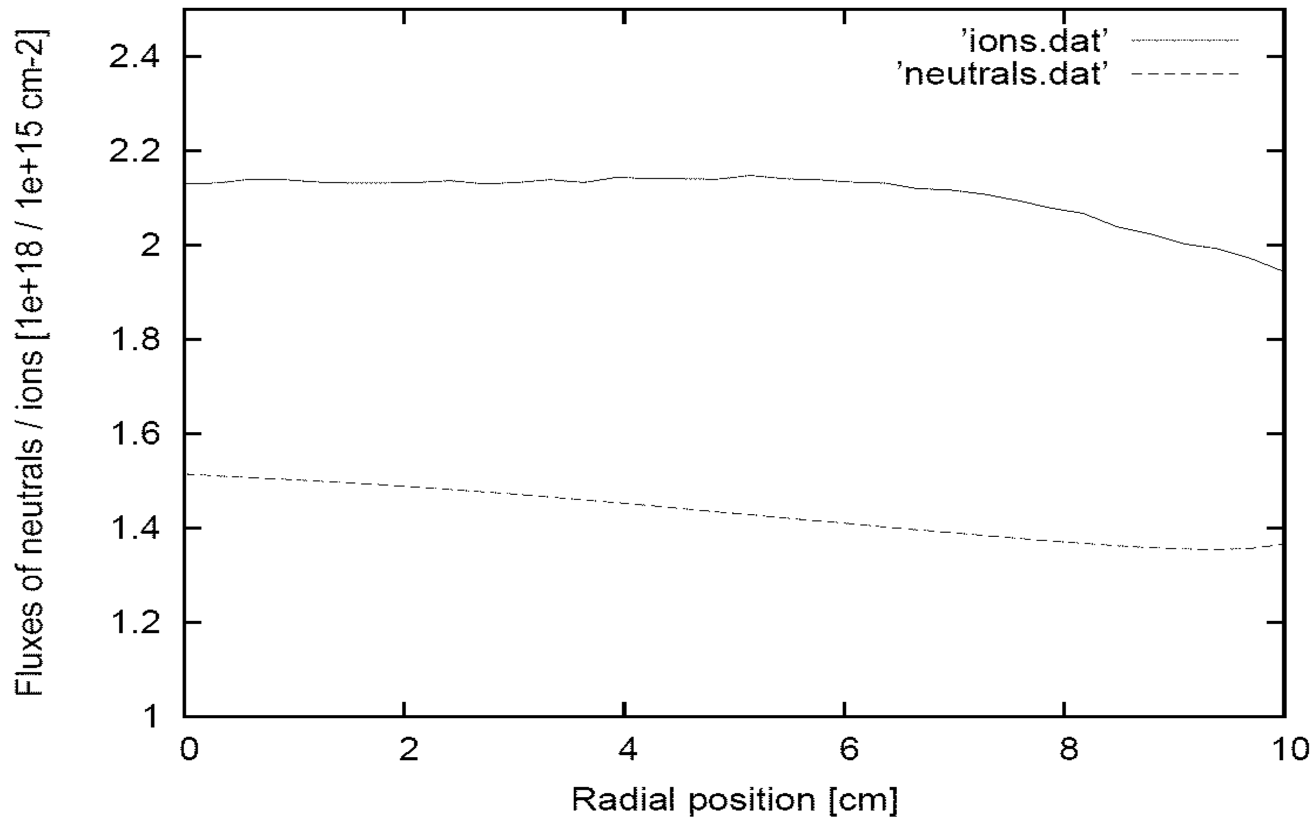


Example for flux at wafer vs. radial position for neutrals (O) and ions (dominant ion species is O_2+) in a CCP reactor

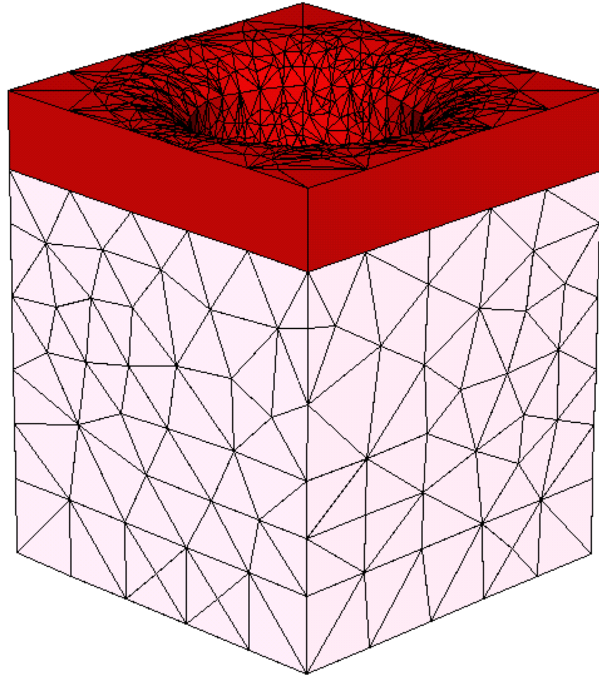
MODELING OF PECVD OF SILICON OXIDE ON FEATURE SCALE

- Rate contributions are due to
  - Neutrals (radicals): isotropic angular distribution
  - Ions: Gaussian distribution
- Local rate $R_{PECVD} \sim (s_c F_{neutral} + F_{ion})$, with
  - F_x: local particle flux of neutrals and ions, respectively
  - s_c: neutral sticking coefficient
- Model parameters
  - **r** $= R_n / (R_n + R_i)$ in 1D regions (R_i is rate resulting from ions, R_n is rate resulting from neutrals)
  - Sticking coefficient of neutrals $\mathbf{s_c}$
  - $\boldsymbol{\sigma}$ of Gaussian distribution for ions

MODEL PARAMETER VARIATIONS ACROSS WAFER

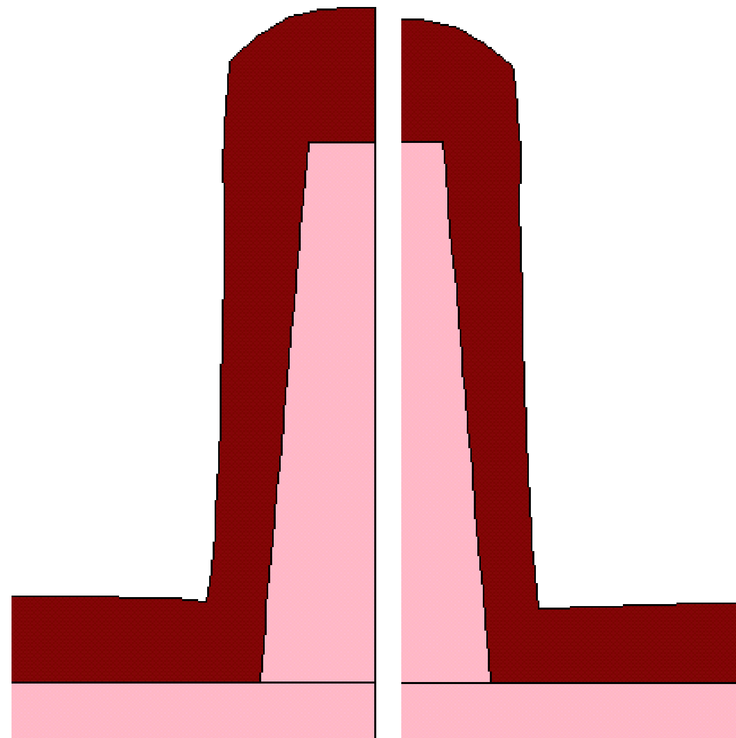
Position [cm]	O_2^+ ion flux [1e15 cm^{-2}]	Neutral flux [1e18 cm^{-2}]	$r = R_n / (R_n + R_i)$ in 1D regions	d_{top} [µm]
0.0	2.13	1.52	0.80	1.0
1.8	2.13	1.49	0.80	0.99
3.9	2.14	1.45	0.79	0.97
5.8	2.14	1.42	0.79	0.95
7.9	2.08	1.37	0.79	0.92
10.0	1.94	1.37	0.80	0.90

SiO_2 layer deposited in hole

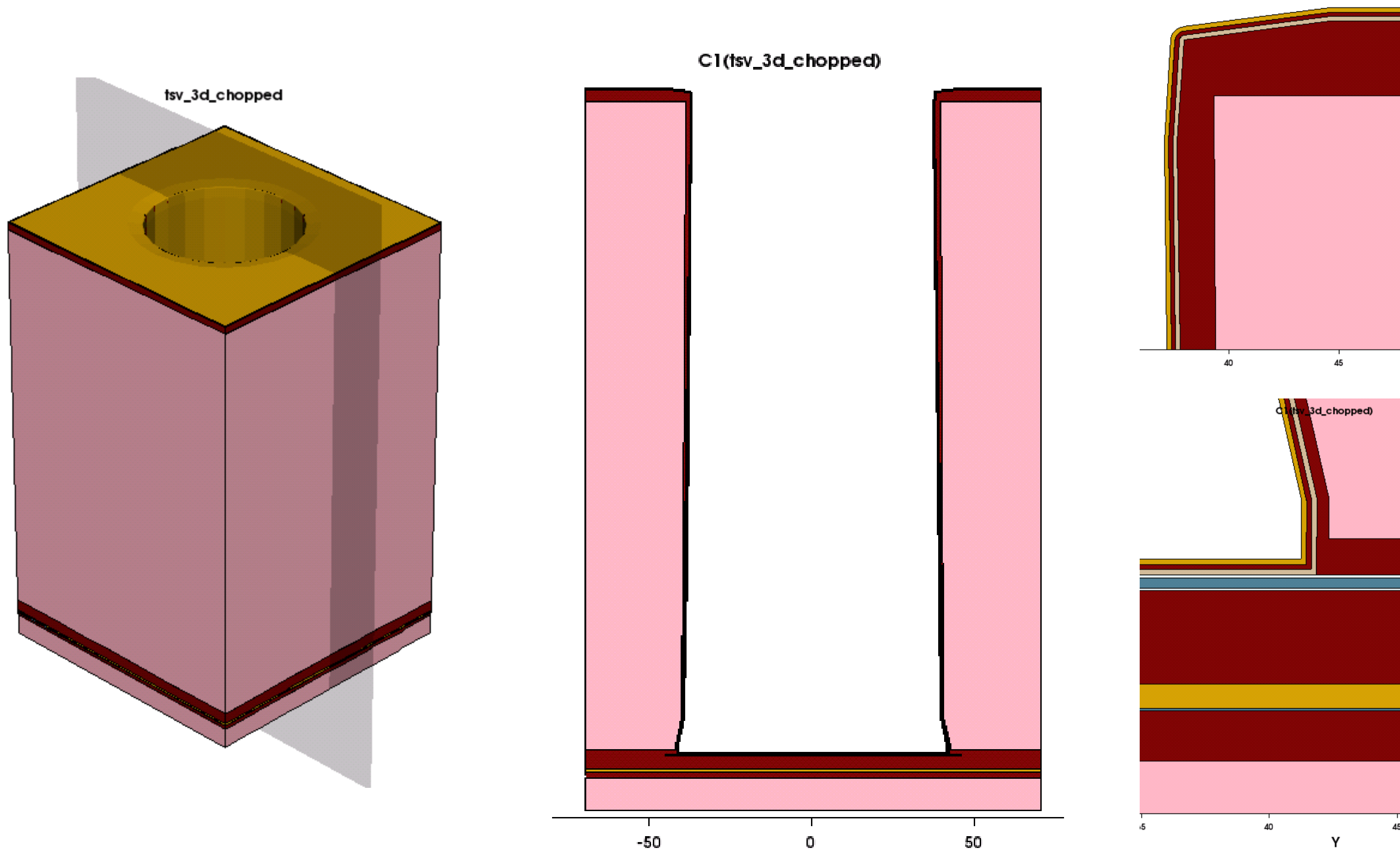


Wafer center

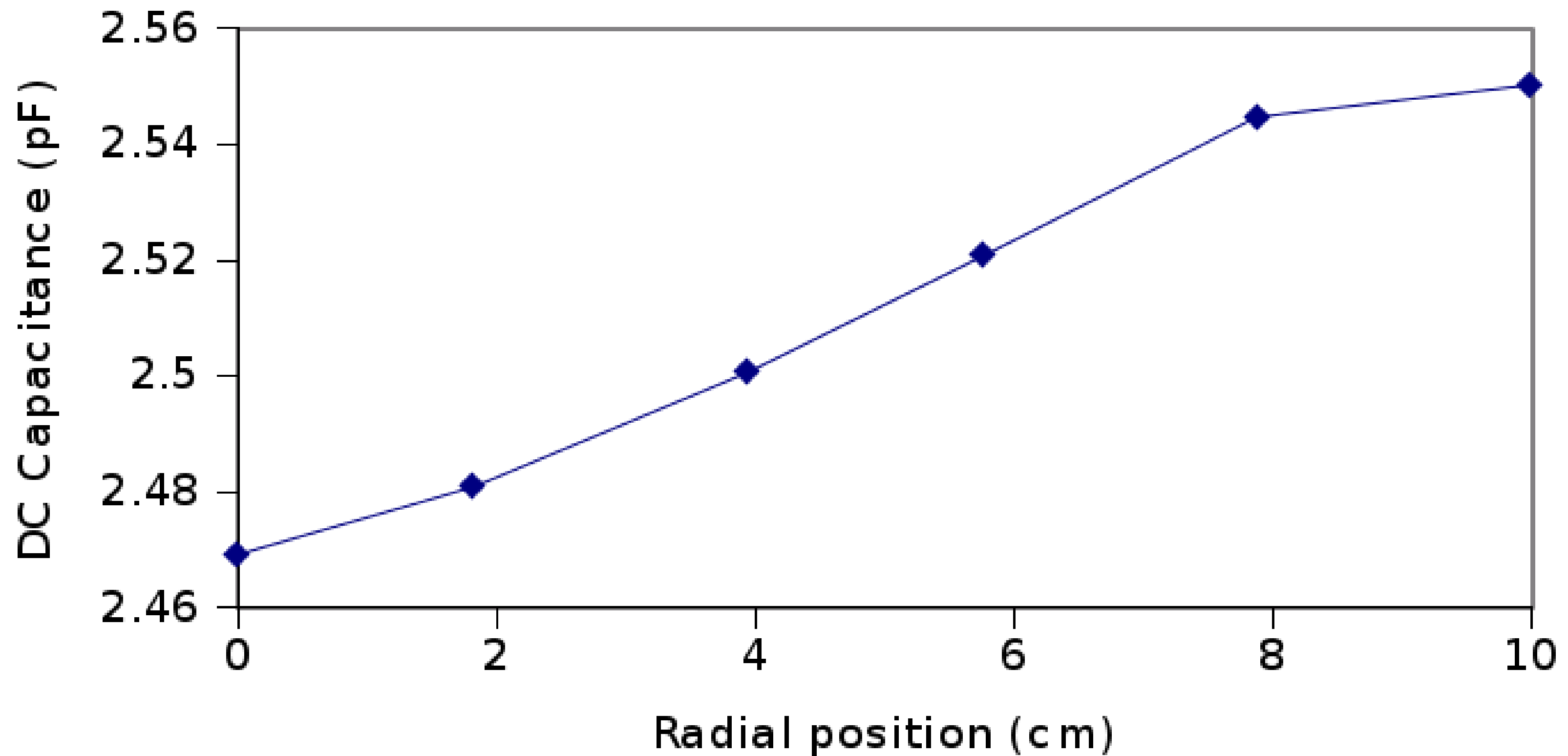
10.0 cm off-center



EXAMPLE FOR PROFILE VARIATION ACROSS WAFER

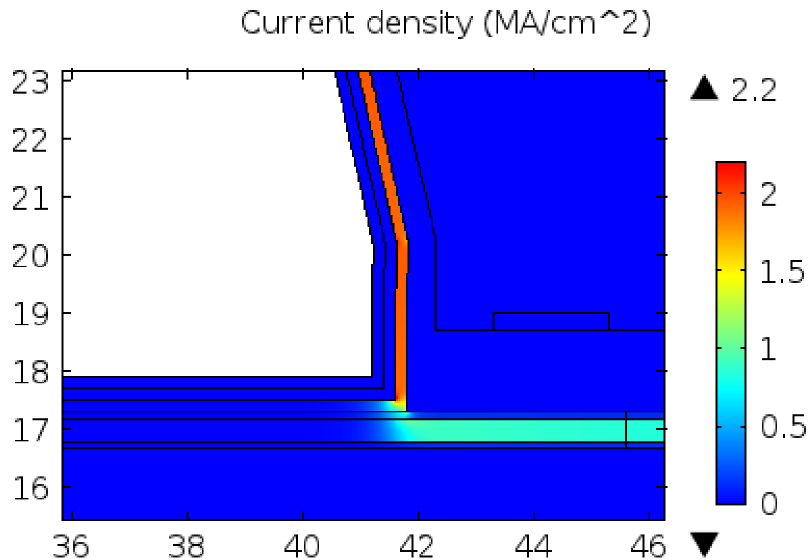


In the TSV, two PECVD layers form part of the oxide layer stack before tungsten deposition

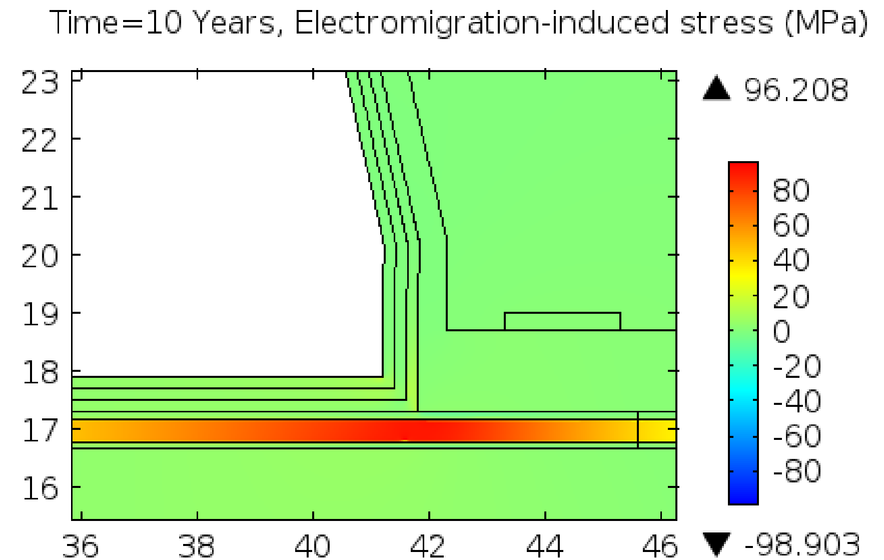


Simulated variation (COMSOL) of DC capacitance between different positions of the TSV structure on the wafer

Current density distribution



Resulting electromigration-induced stress distribution after 10 years



SIMULATED CURRENT DENSITY AND STRESS

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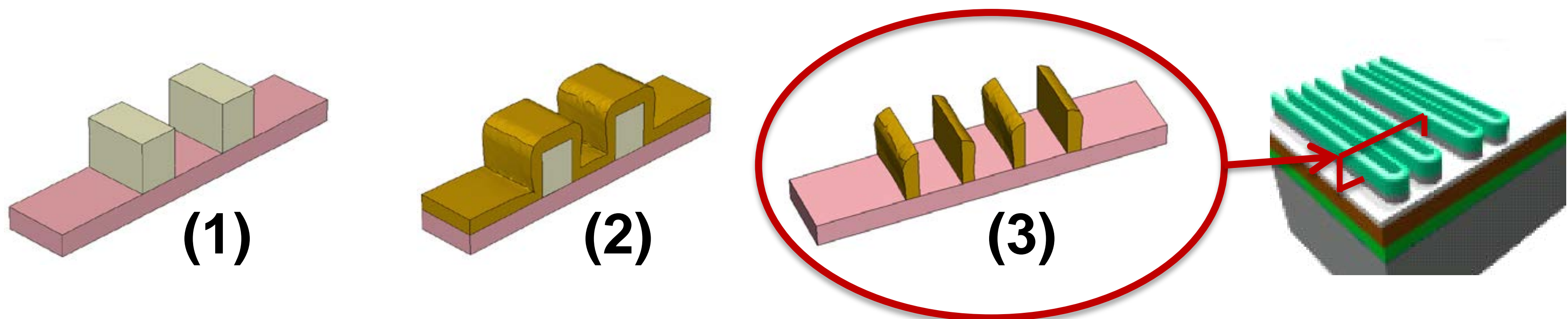
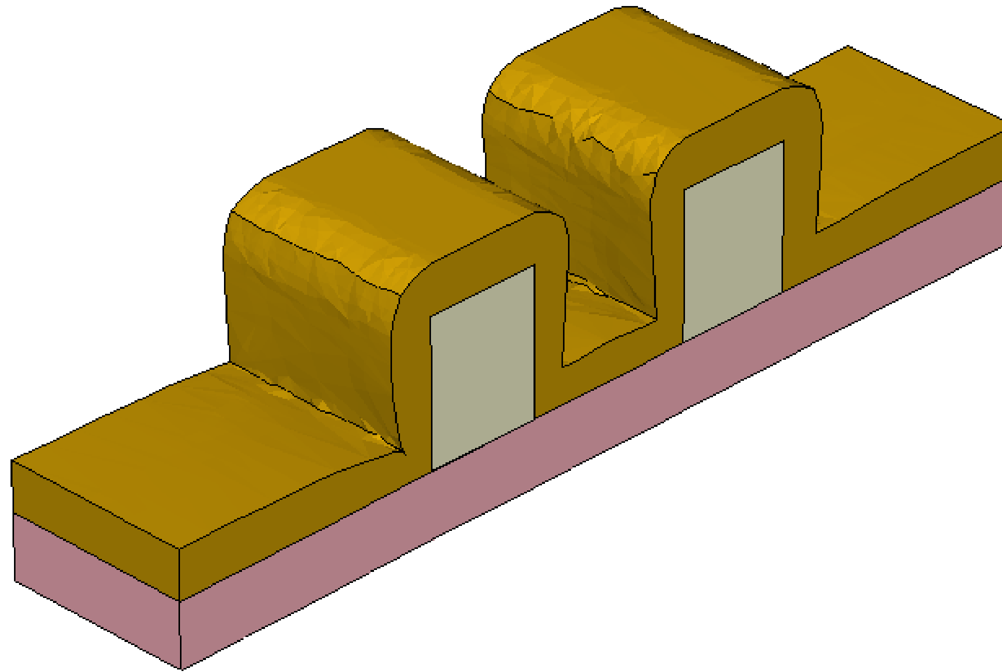
EXAMPLE: SIMULATION OF SPACER PATTERNING FOR FINFET STRUCTURE

SIMULATION OF SPACER PATTERNING FOR FINFET STRUCTURE AS PART OF SRAM CELL

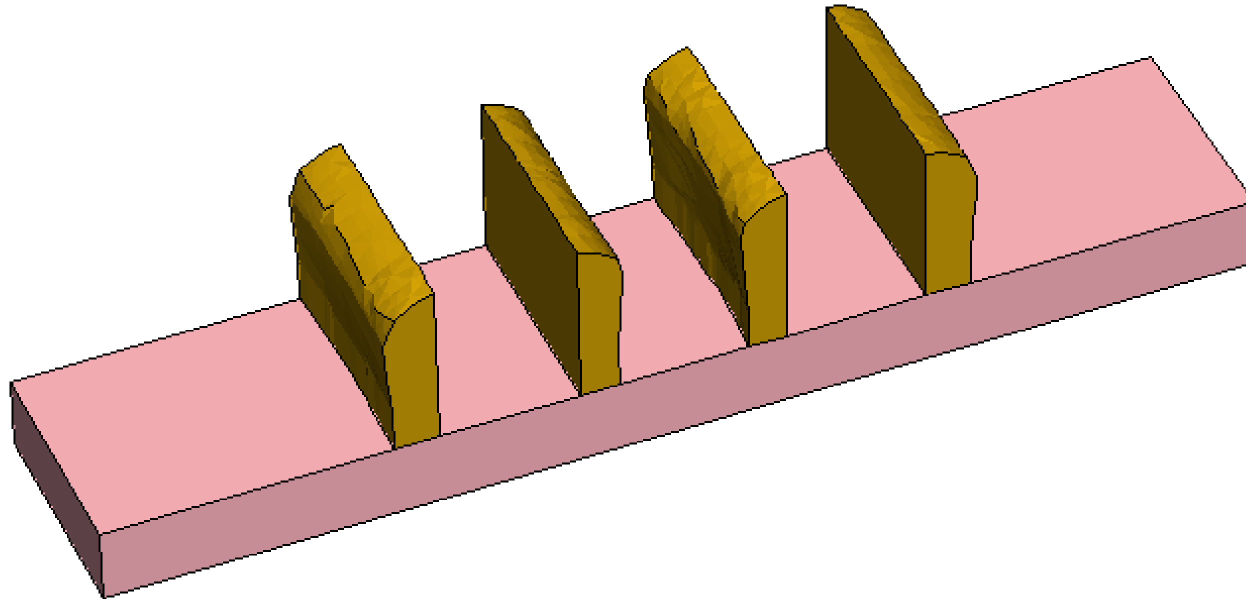
- Carbon lines are created using CD values from a lithography model (1)
- CVD oxide is deposited (2) and etched back to form the spacers after carbon line removal (3)





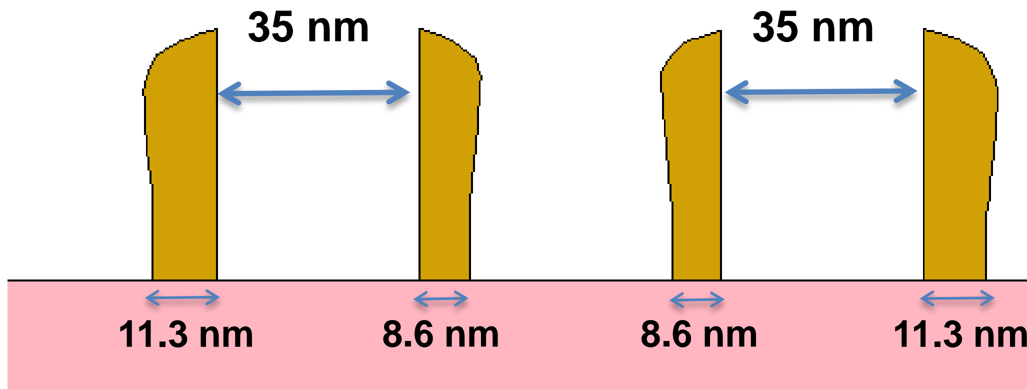
MODELING OF NON-CONFORMAL OXIDE DEPOSITION

Chemical vapor deposition simulated with IISB physical deposition simulator DEP3D using single sticking coefficient model (sticking coefficient $s_c = 0.5$)



MODELING OF ANISOTROPIC ETCHING

Etching emulated as perfectly anisotropic, using geometrical model of Synopsys SPROCESS. Etching is followed by removal of carbon lines.



CD [nm]	Bottom width inner spacers [nm]	Bottom width outer spacers [nm]
31.5	8.9	11.3
35	8.6	11.3
38.5	8.3	11.3

Simulation for **nominal CD (35 nm)** of carbon lines

Variation of CD of carbon lines leads to a variation of the **bottom width** of the inner spacers

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CONCLUSIONS

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CONCLUSIONS

- Coupling between equipment- and feature-scale simulation allows us to take into account equipment effects for feature-scale modeling
  - As an example, for PECVD of SiO_2 using TEOS chemistry, the coupling has been implemented by transferring fluxes of ions and neutrals from equipment- to feature-scale
  - The simulations have been integrated into the process flow simulation for the fabrication of a TSV structure
  - The simulated structures were transferred to electrical and mechanical modeling for performance and reliability analysis
- Coupled simulation of topography steps allows us to predict variation effects on feature-scale level
  - As an example, spacer patterning for a FinFET structure was shown

SUPERTHEME Fraunhofer IISB