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Gold Standard Simulations Limited/University of Glasgow

ESSCIRC ESSDERC 2015

VARIABILITY-AWARE DEVICE SIMULATION IN SUPERTHEME

Conference Sponsors:

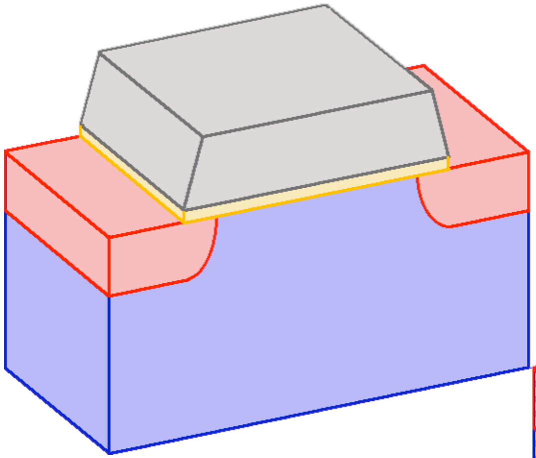
OUTLINE

1. Introduction
2. Modeling Methodology for variability
3. Interplay of Process and Statistical Variability
4. Conclusions

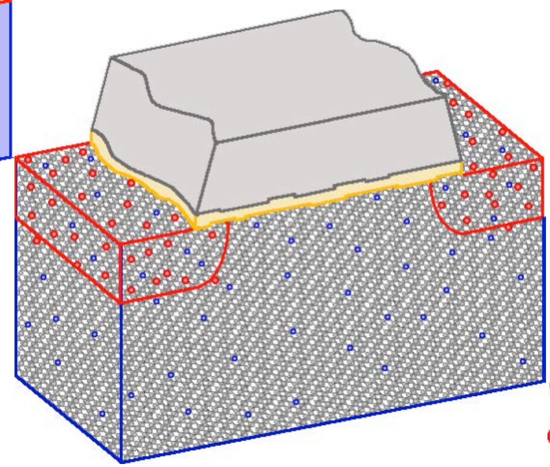
OUTLINE

1. **Introduction**
2. Modeling Methodology for variability
3. Interplay of Process and Statistical Variability
4. Conclusions

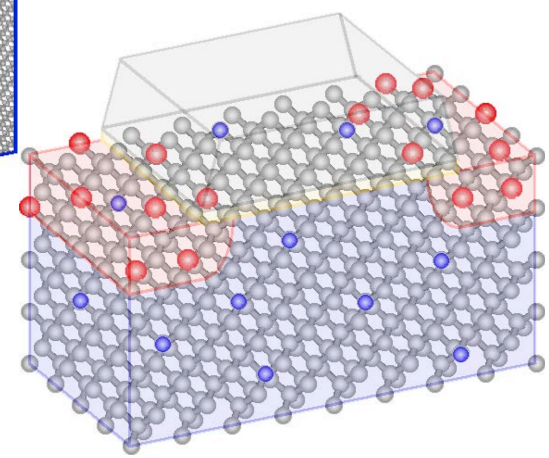
The semiconductor industry is facing atomic scale limitations



The simulation
Paradigm now



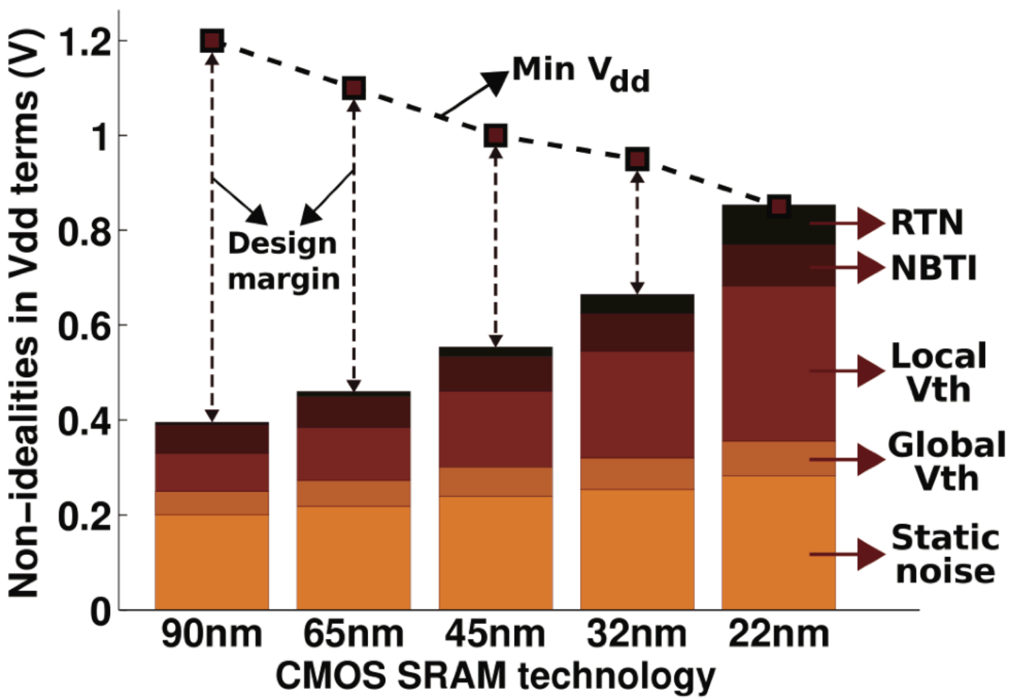
A 22 nm MOSFET
In production 2013



A 4.2 nm MOSFET
In production ????

A. Asenov 1998

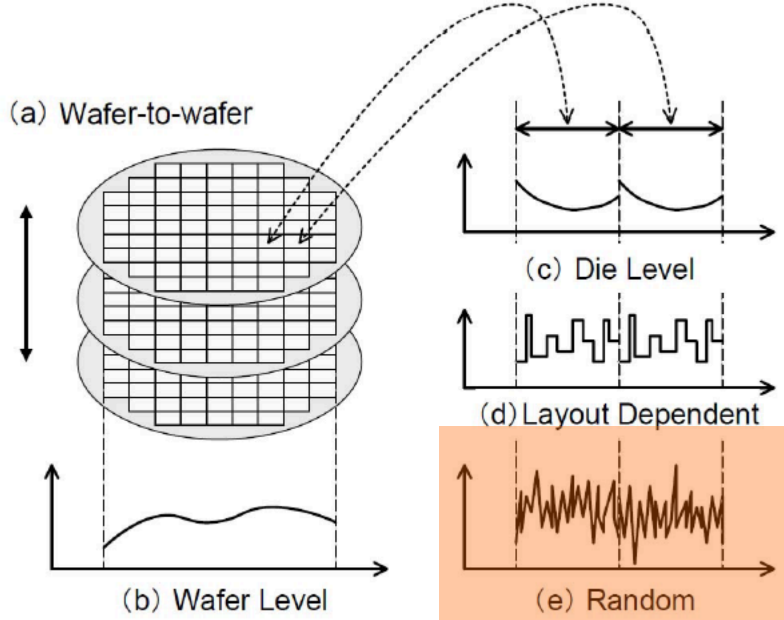
Statistical variability is one of the major challenges associated with scaling



After K. Takeuchi (NEC)

Variability results in higher parametric yield loss

Variability Decomposition



	Process	Environment	Temporal
Global	<L_g> and <W>, <layer thicknesses>, <R>'s, <doping>, <t_{ox}>, <V_{body}>	Operating temperature range, V_{DD} range	<NBTI> and Hot electron shifts
Local	**Line Edge Roughness (LER), Discrete doping, Discrete oxide thickness,** R and V_{body} distributions	Self-heating, IR drops	**Distribution of NBTI,** Voltage noise, SOI V_{body} history effects, Oxide breakdown currents
Across-chip	Line Width, due to pattern density effects	Thermal hot spots due to nonuniform power dissipation	Computational load dependent hot spots

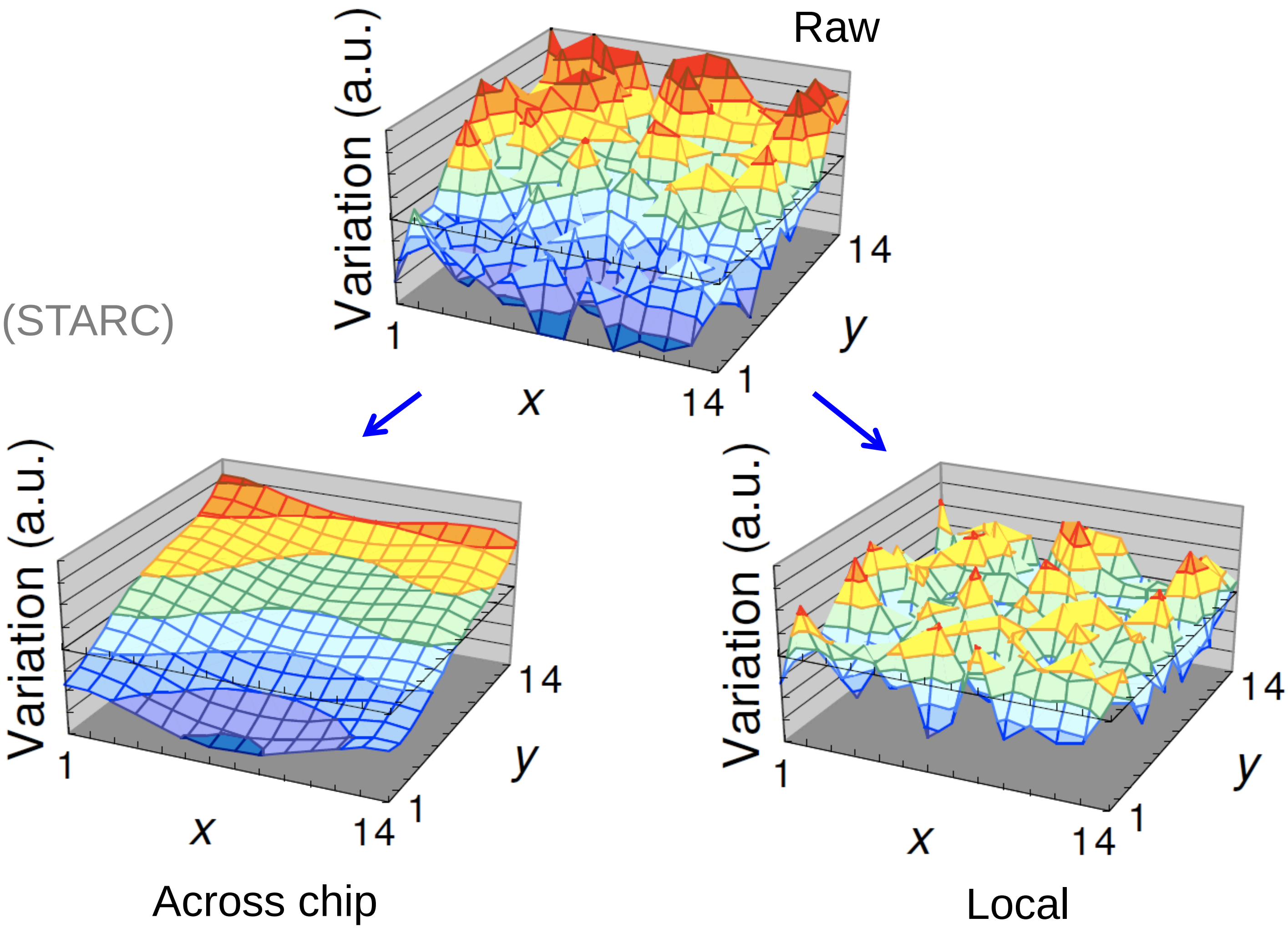
(Takeuchi, Nishida, Hiramoto, SISPAD 2009)

(D. Frank, IBM)

- In general, the variability can be decomposed into global process variation and local random variability.
- PV: systematic, spatially correlated, long-range.
- SV: random, no (weak) correlation, short-range.

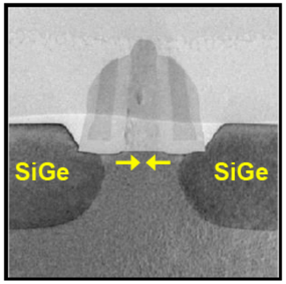
Variability Decomposition

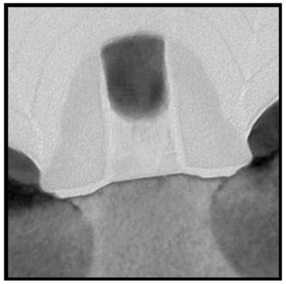
M. Muracata (STARC)

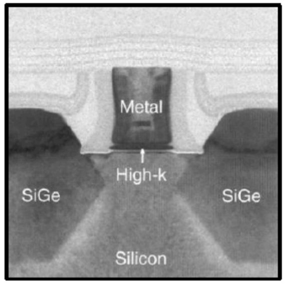


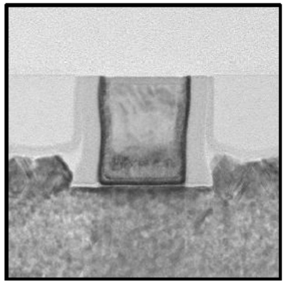
Saturation in performance and increasing variability drives the CMOS innovations

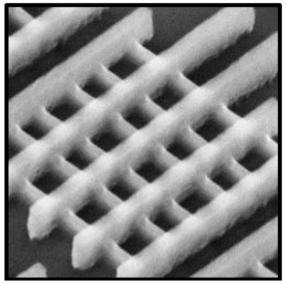
2003	2005	2007	2009	2011
<u>90 nm</u>	<u>65 nm</u>	<u>45 nm</u>	<u>32 nm</u>	<u>22 nm</u>











Invented SiGe Strained Silicon	2^{nd} Gen. SiGe Strained Silicon	Invented Gate-Last High-k Metal Gate	2^{nd} Gen. Gate-Last High-k Metal Gate	First to Implement Tri-Gate

M Bohr (Intel)

Strained Silicon

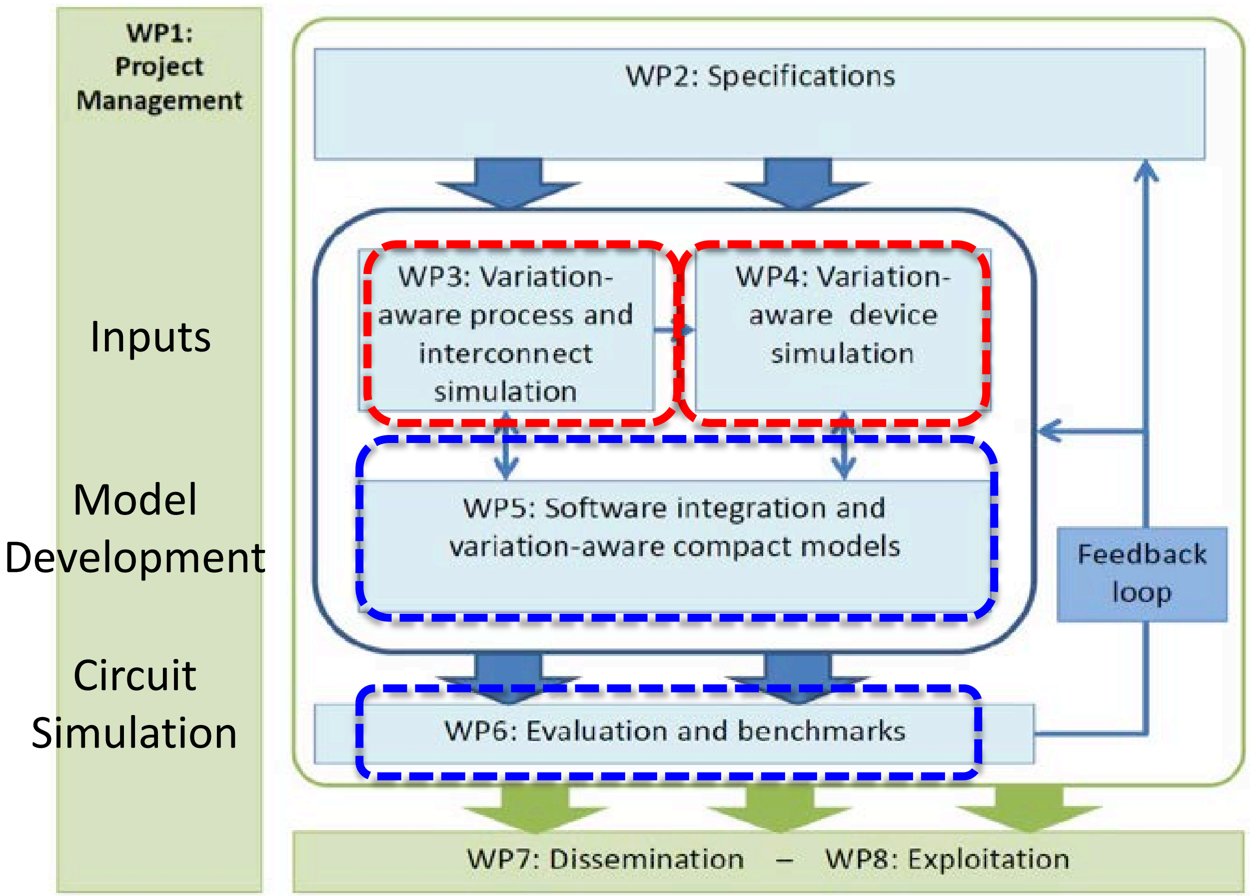
High-k Metal Gate

Tri-Gate

New transistor architectures improve performance and can reduce statistical variability

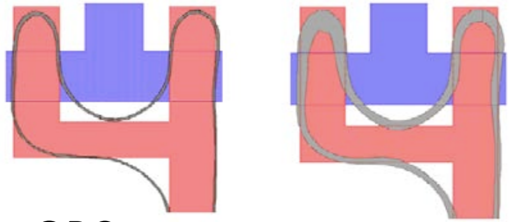
OUTLINE

SUPERTHEME - CONTEXT



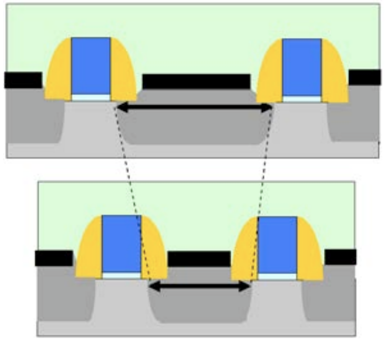
Process Variation - Systematic

- Lithography induced variations

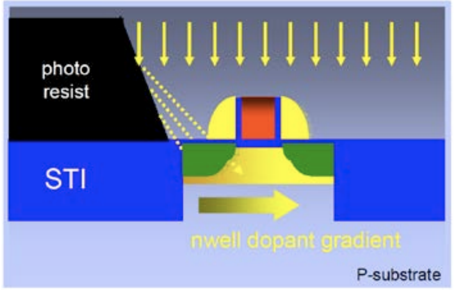


OPC
Intensity variation
Z-axis variation

- Stress induced variations

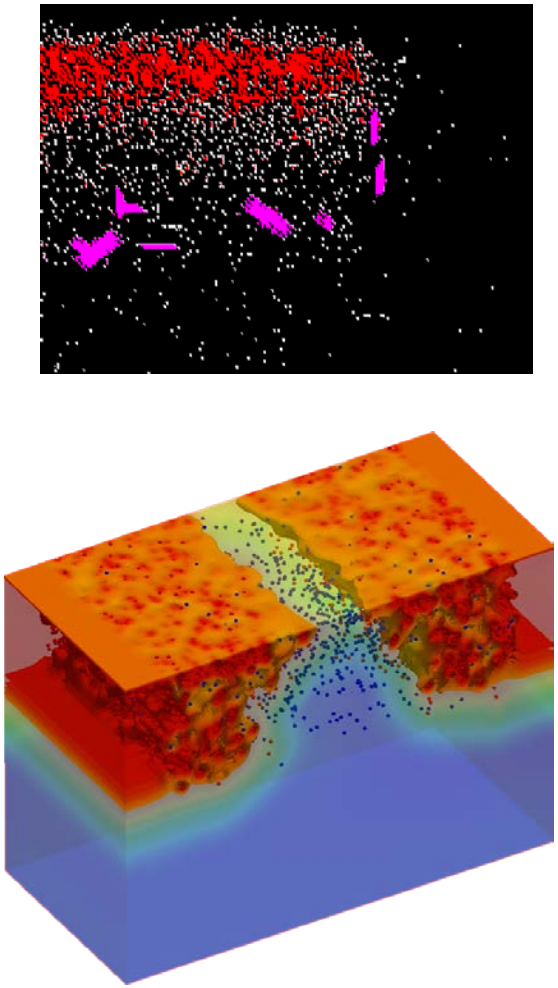


- Well Proximity effects

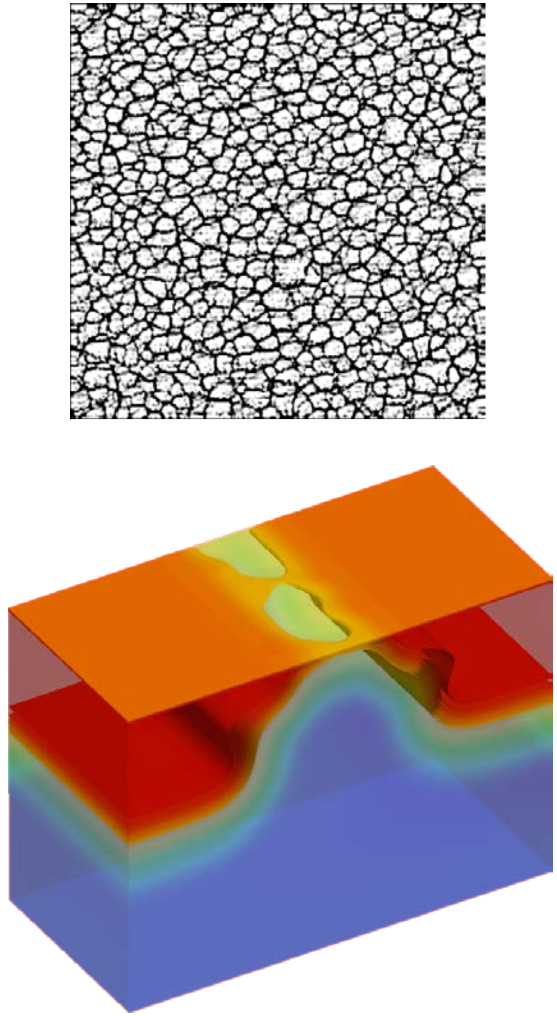


Extensively addressed in previous talks !

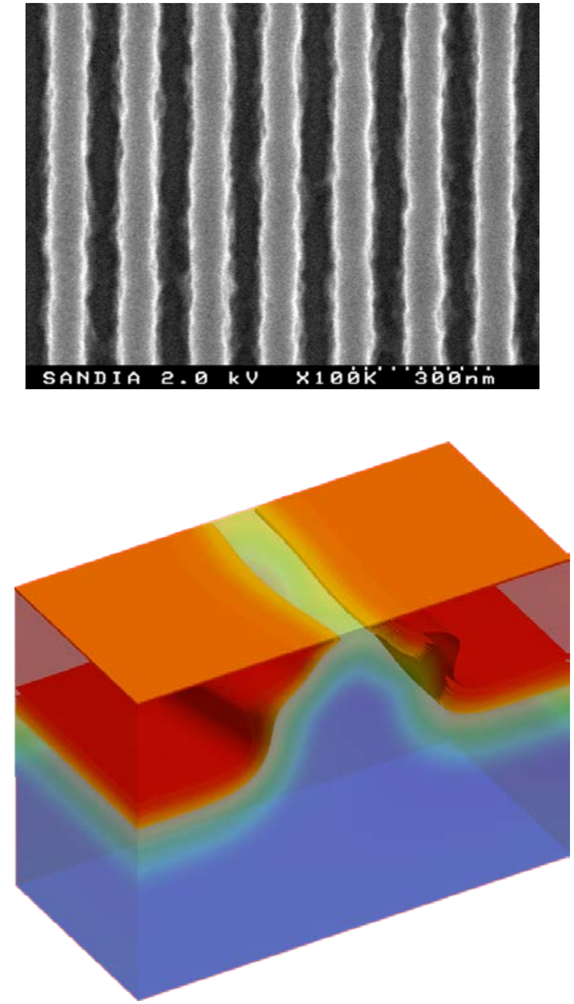
Main sources of Statistical Variability



Random discrete dopants

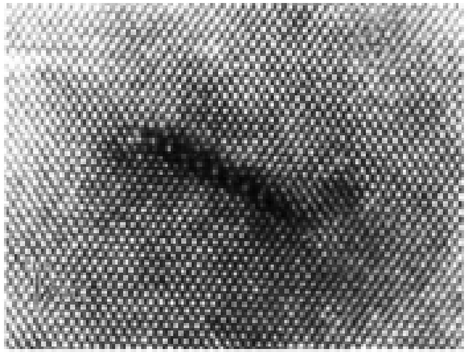


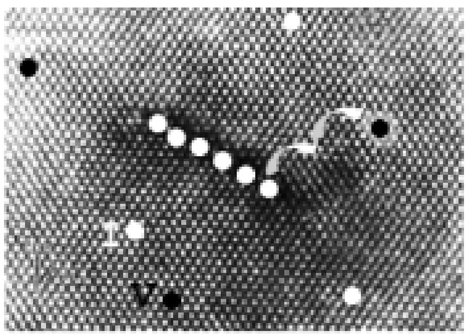
Metal Gate Granularity

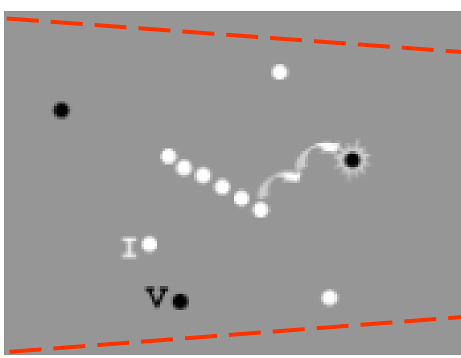


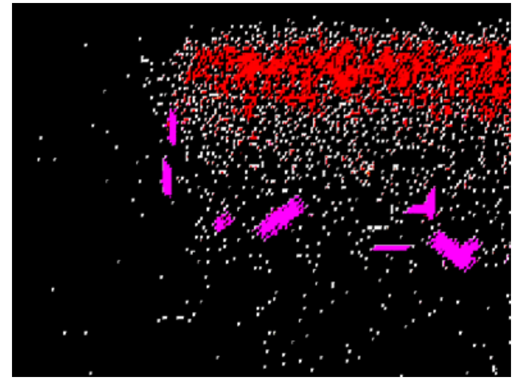
Line edge roughness

RDD in Simulation (1)- Atomistic Process Simulation



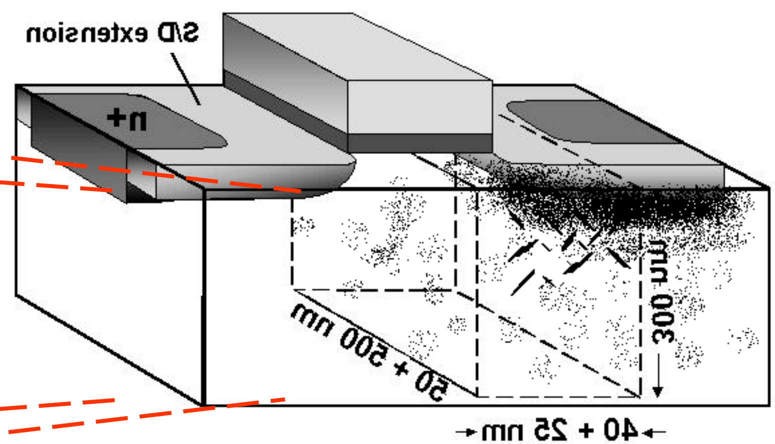






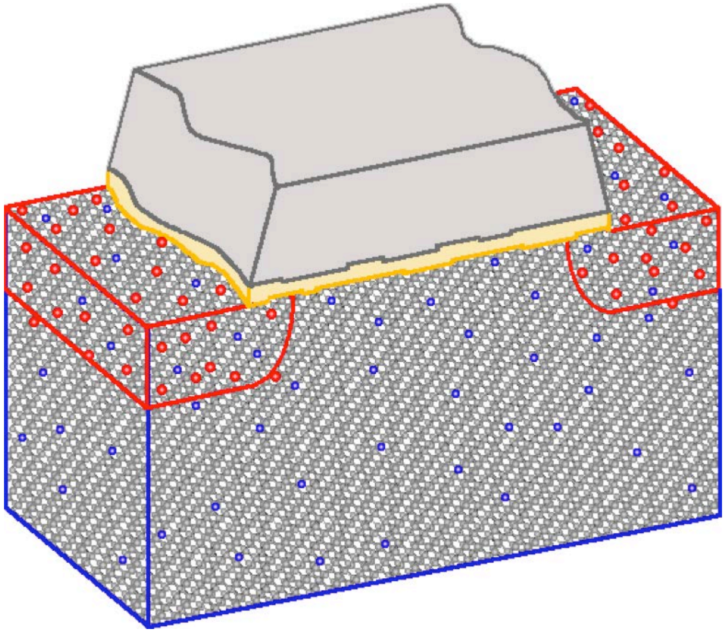
Output

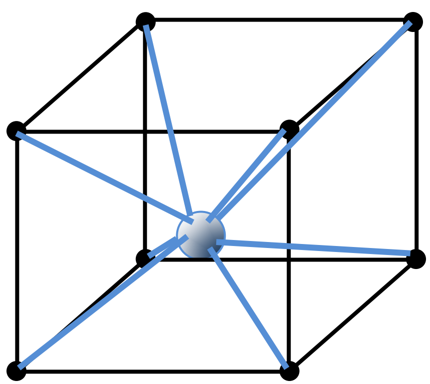
KMC Simulator



DADOS, Synopsys

RDD in Simulation (2)- Poisson Distribution + realistic doping profile

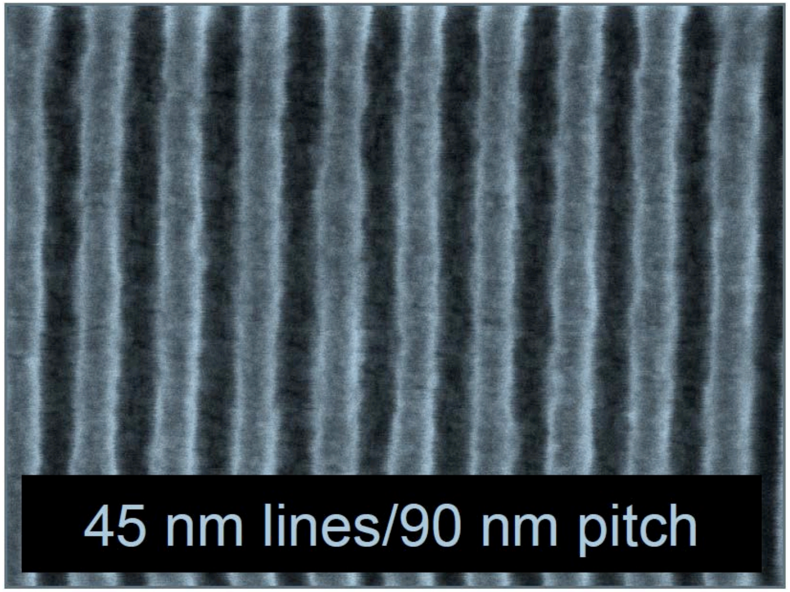




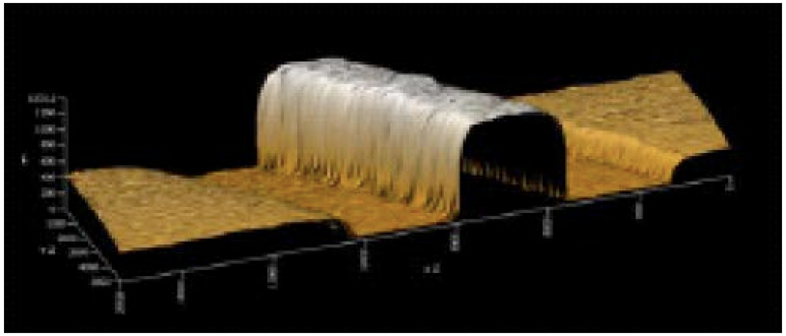
- Cover the simulation domain with the Si lattice
- Visit each lattice site and generate dopant with probability $p_i = N(x_i, y_i, z_i)\Delta V$ where $\Delta V = a_{Si}^3/8$ is the volume associated with each Si atom
- Assign the dopant to the surrounding grid nodes using cloud in a cell approach

A. Asenov et al.

LER in Simulation – Origins

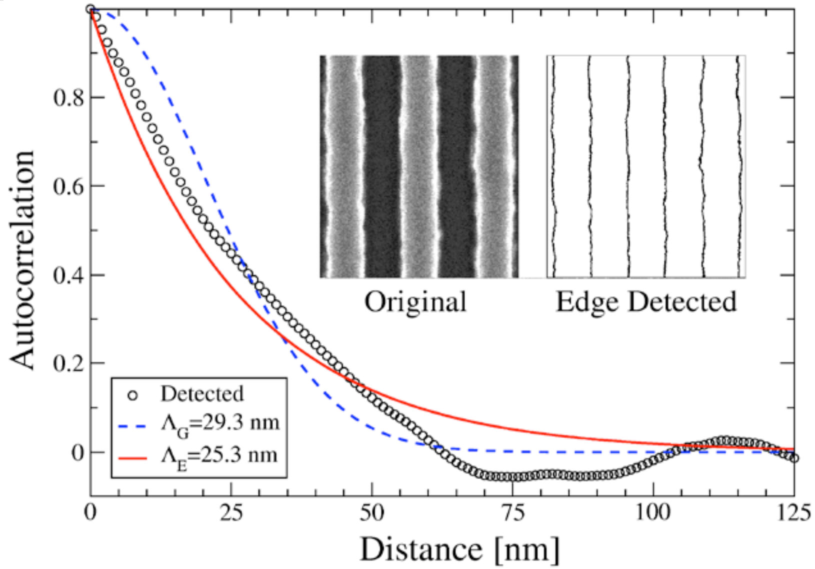


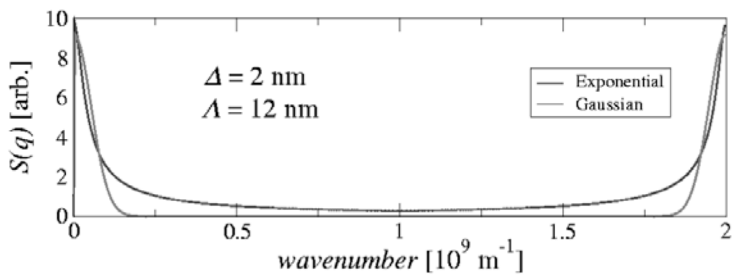
T. Brunner, ICP 2003

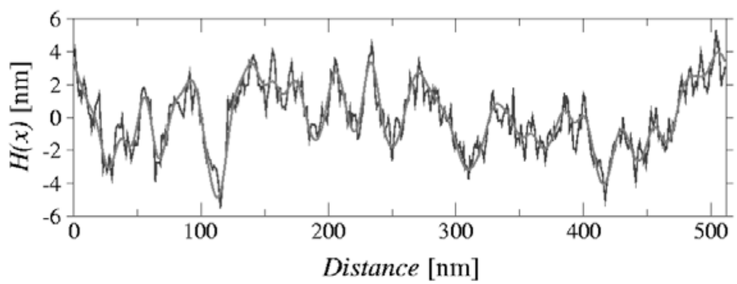


- Fluctuation in the total dose due to light quantisation.
- Fluctuation in photon absorption position.
- Nanoscale non-uniformities in resist composition.
- Statistical variation in the acid-catalysed de-protection.
- Statistical effects in polymer chain dissolution

LER in Simulation – Implementation







- A complex array of N elements is generated according to the power spectrum of the chosen autocorrelation function.

  Gaussian

  $$S_G(k) = \sqrt{\pi}\,\Delta^2 \Lambda e^{-\frac{k^2\Lambda^2}{4}}$$

  Exponential

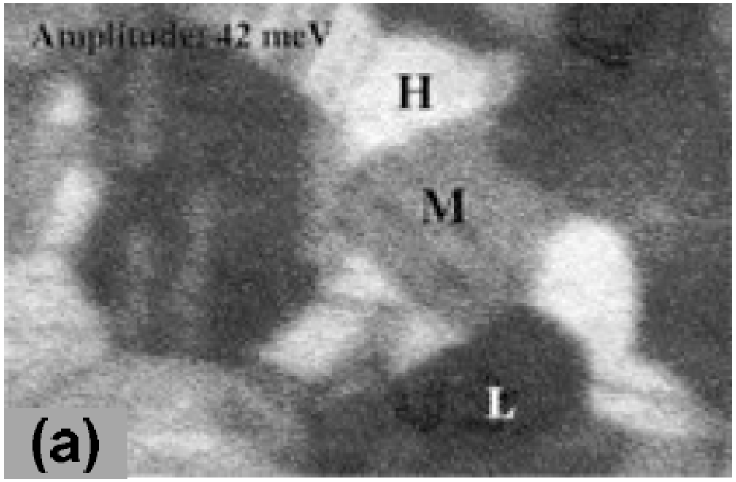
  $$S_E(k) = \frac{2\Delta^2\Lambda}{1 + k^2\Lambda^2}$$

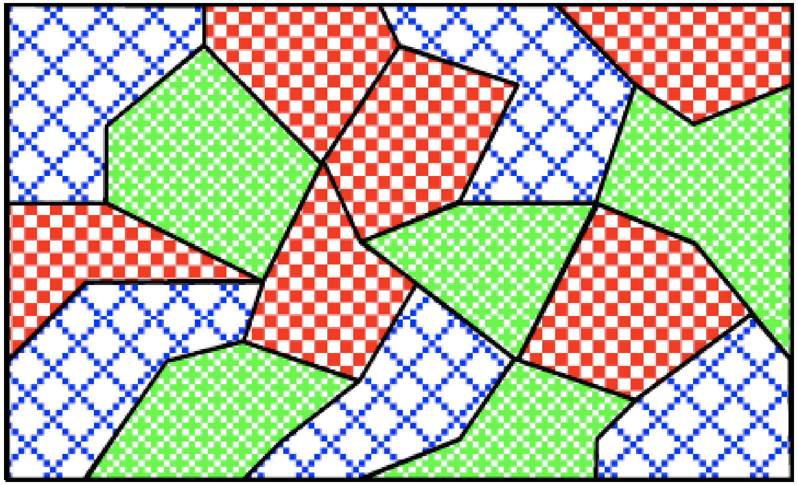
  $$k = i\frac{2\pi}{N\,dx}$$

- The phase of the elements is chosen randomly. However only $(N/2-2)$ elements are independent.

A. Asenov et al. 2003

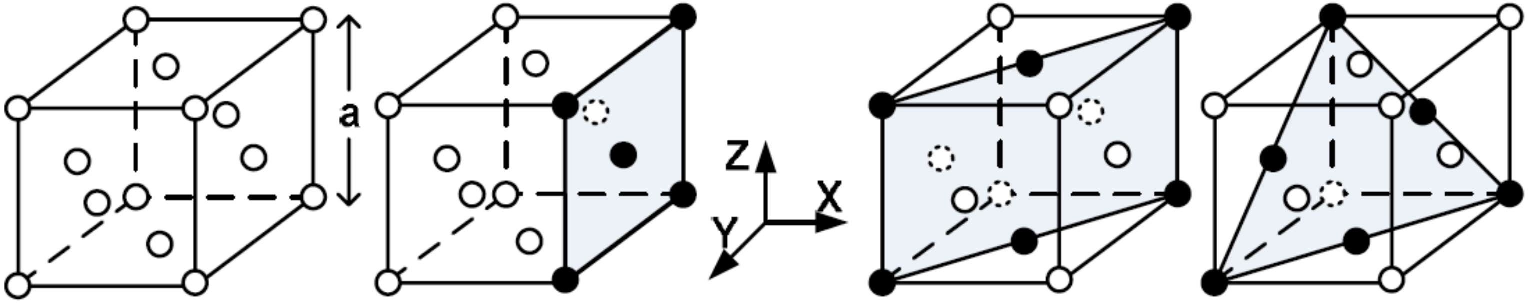
MGG in Simulation - Origins





$\Phi_{111}(L)>\Phi_{100}(M)>\Phi_{110}(H)$

Different surface density at different orientations



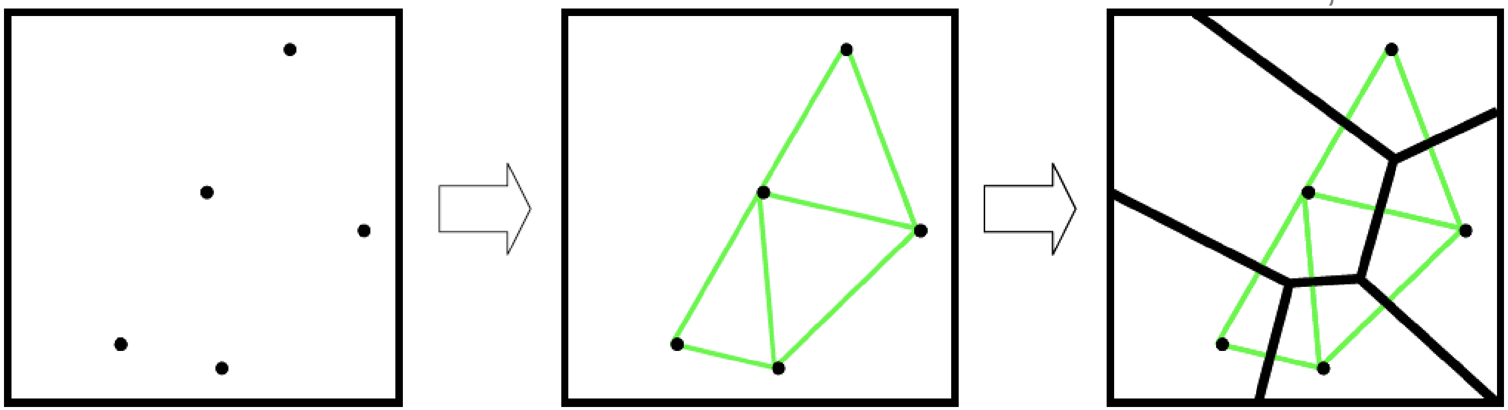
<100> <110> <111>

H. Dadgour et al.

MGG in Simulation – Implementation

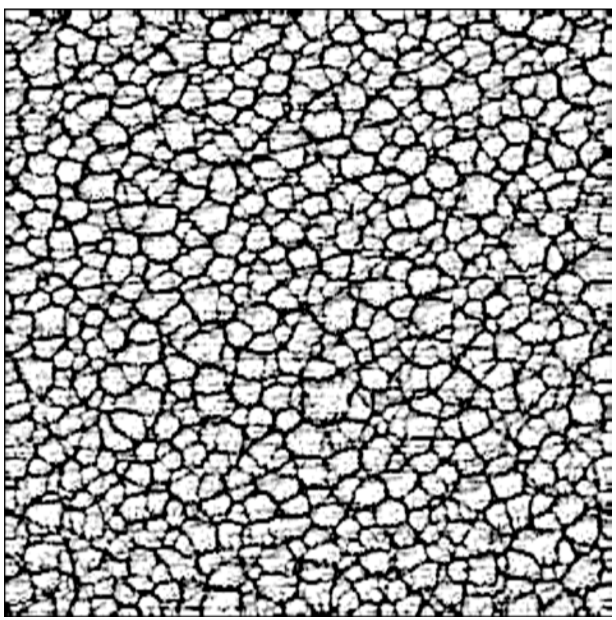
1. 3D Voronoi Geometric Tesselation

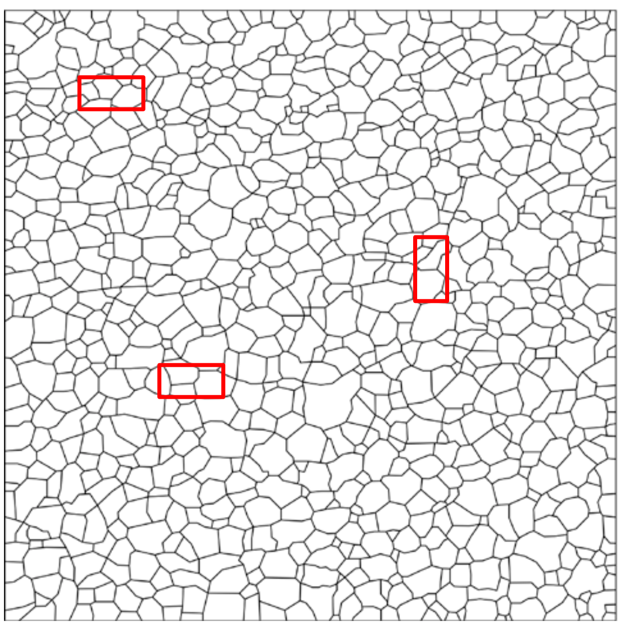
A.T. Putra, ISDRS 2007



2. Use of large interdigitise template

A. Brown





OUTLINE

1. Introduction
2. Modeling Methodology for variability
3. **Interplay of Process and Statistical Variability**
4. Conclusions

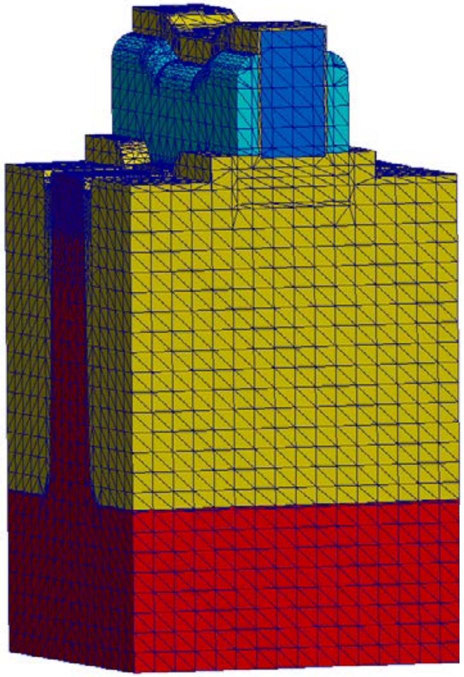
THE GSS SIMULATION TOOLCHAIN

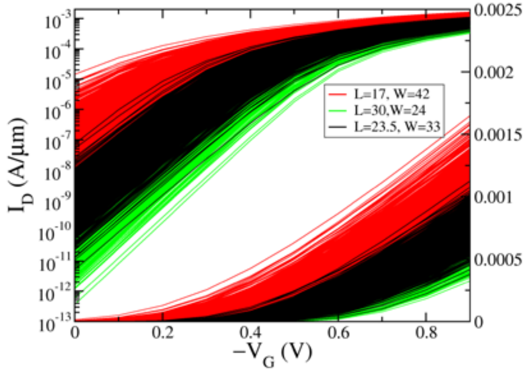
Full simulation tool chain

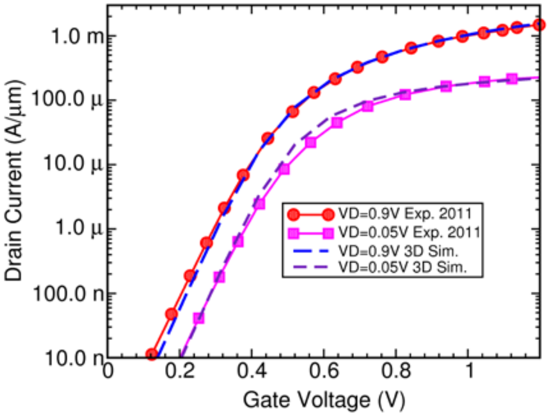
- Structure Manipulation/Translation
  - Monolith
- Device Simulation GARAND
  - DD, 3D Full Band MC , 1D Multi-sub-band MC
- Statistical SPICE Modelling
  - Mystic –SPICE Model extraction
  - ModelGEN – Advanced process and statistical aware SPICE Model generation technology
- Circuit Simulation
  - RandomSPICE – Statistical Circuit Simulation Engine
- Toolchain integration
  - Enigma – Automation and Integration framework

SUPERTHEME 20NM MOSFET

Nominal Device







Process simulation (DrLitho/Sentaurus Process)

Mesh Conversion/Transfer (GSS Monolith)

Device simulation (GSS Garand)

Design of Experiments - Interplay between PROCESS and STATISTICAL VARIABILITY

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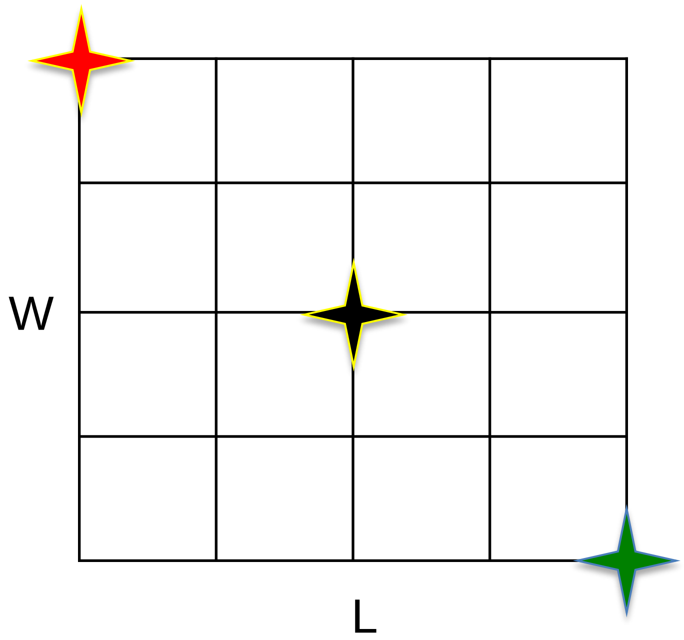
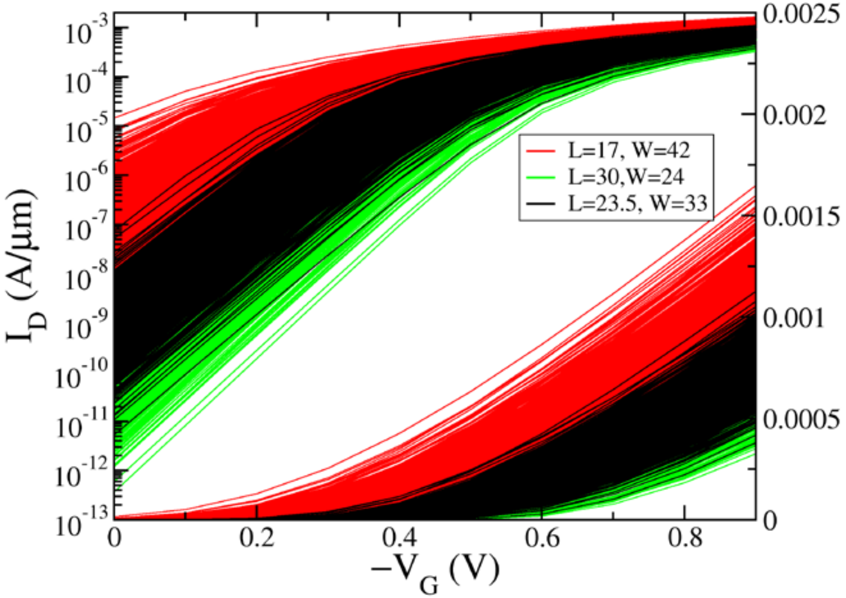




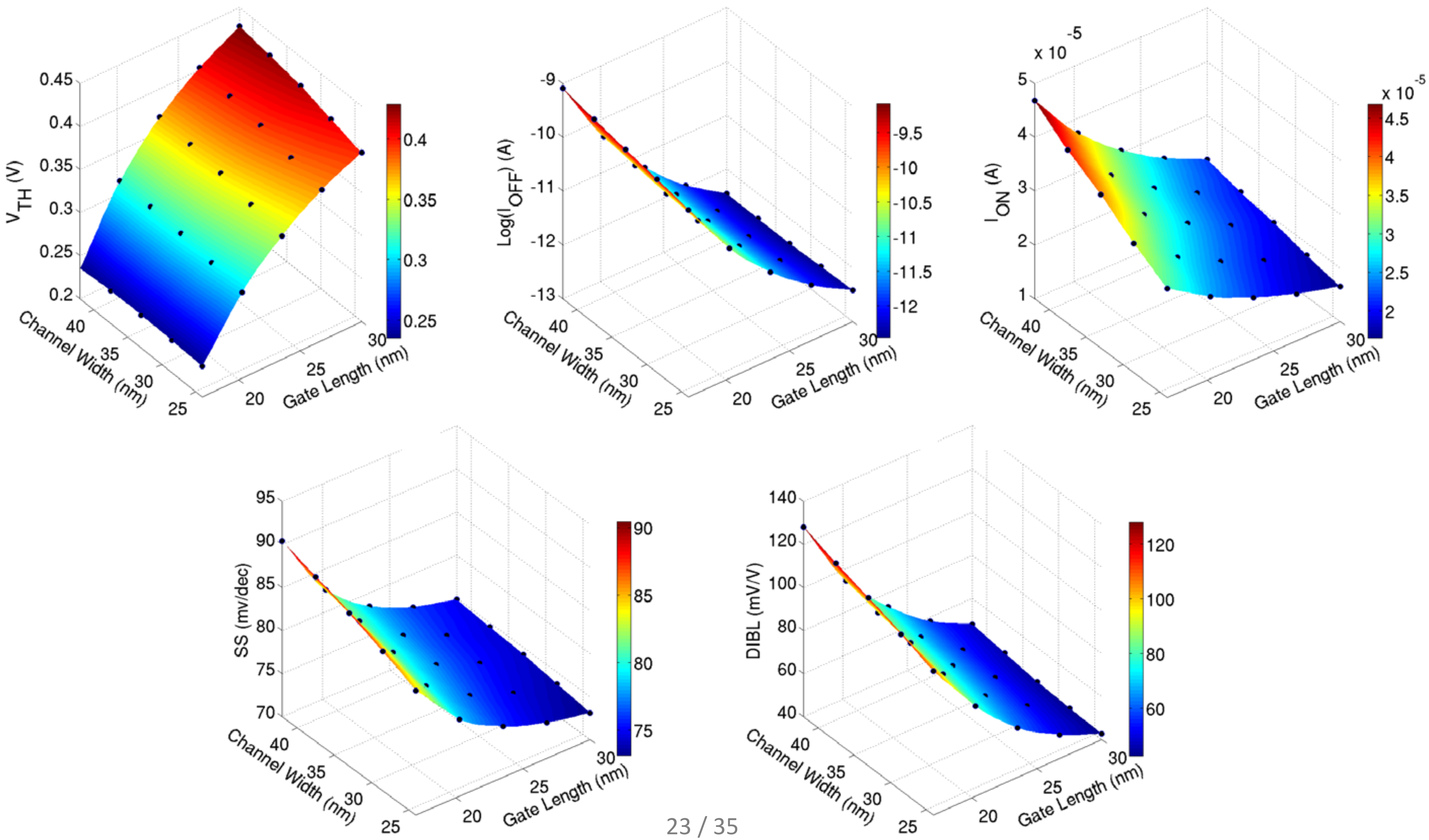
- RDD, LER, MGG
- L_G=17, 20.25, 23.5, 26.75, 30
- W=24, 28.5, 33, 37.5, 42
- 5 × 5 DoE space

FAST CORNER

NOMINAL SILICON

SLOW CORNER

PROCESS VARIABILITY - NMOS



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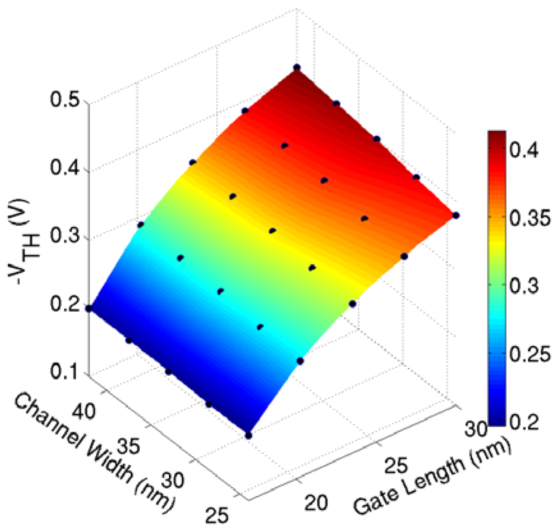
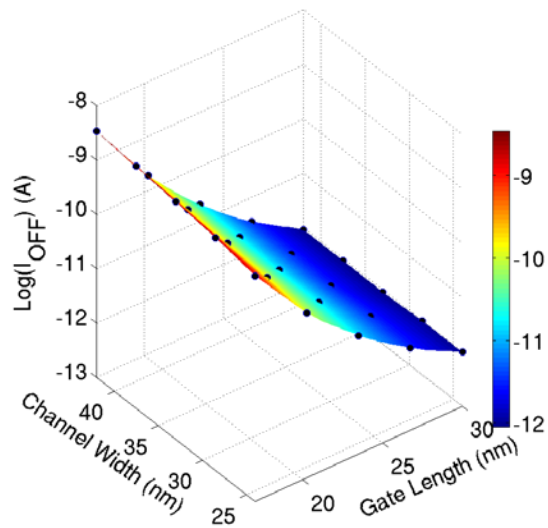
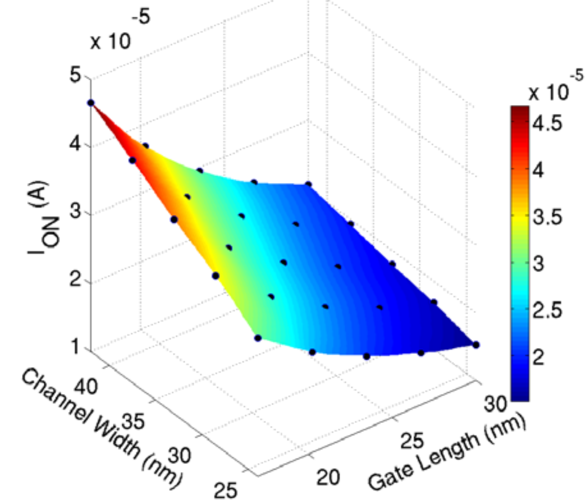
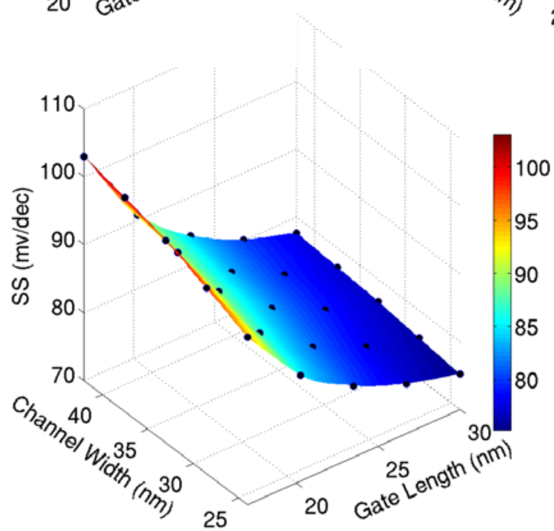
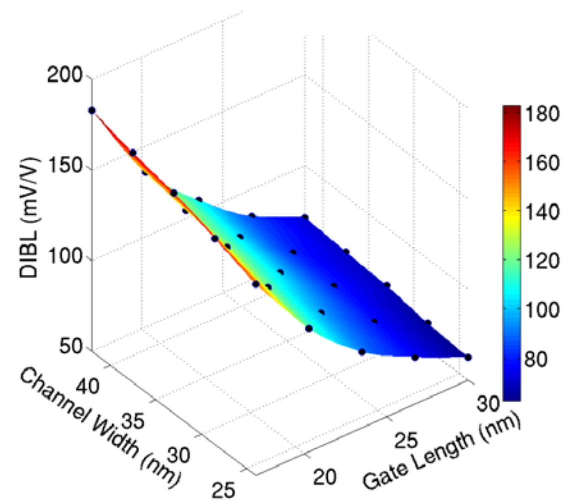
PROCESS VARIABILITY - PMOS



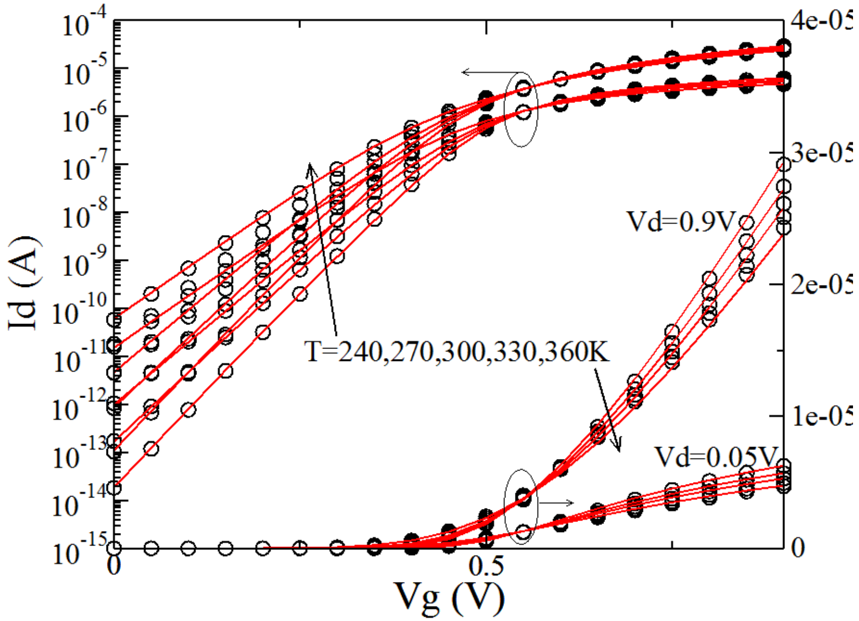




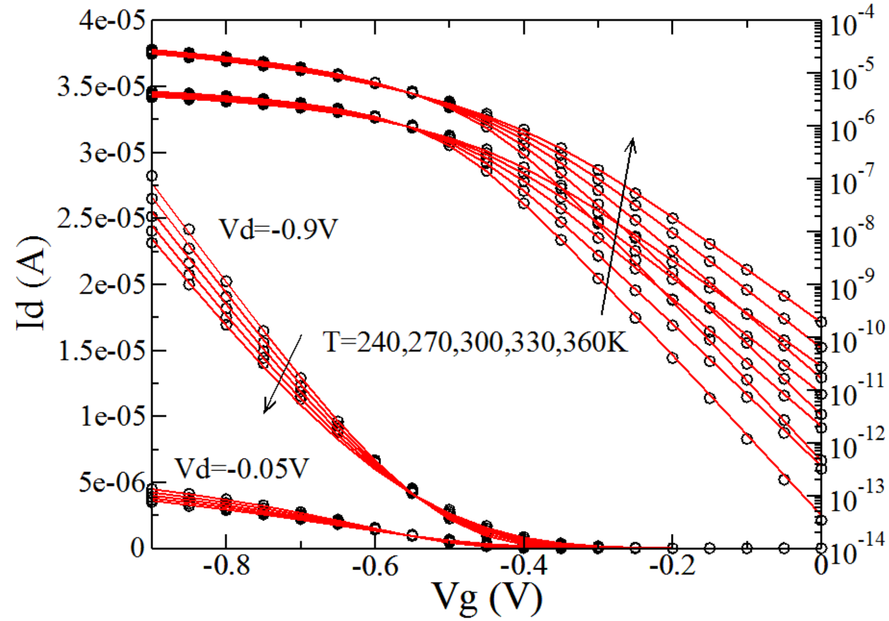




PROCESS VARIABILITY - Temperature



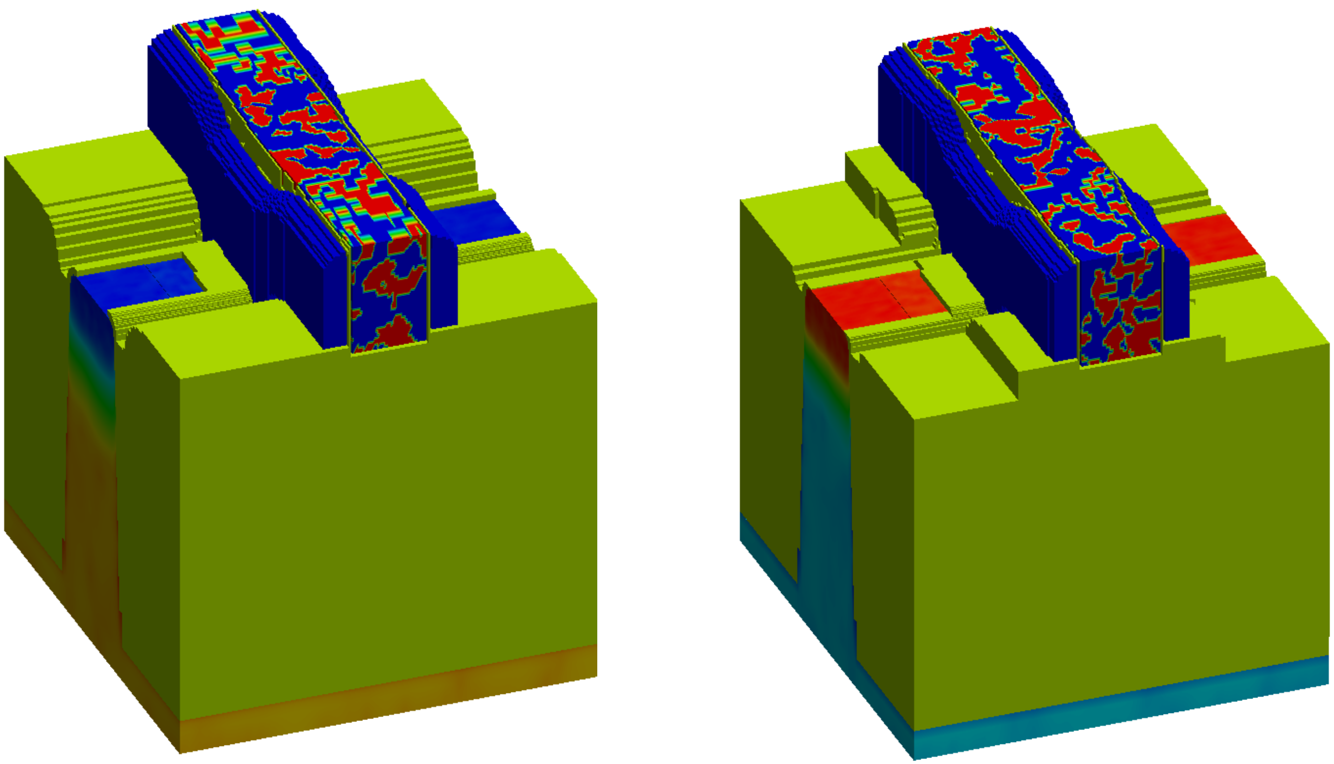
NMOS



PMOS

Temperature Variations are treated in the DoE in the same way as Process Variations

STATISTICAL VARIABILITY



- Nominal L_G=23.5nm, W=33nm
- Realistic MOSFET structures: STI, gate stack
- RDD, LER, MGG variability on top of PROCESS variations

STATISTICAL VARIABILITY

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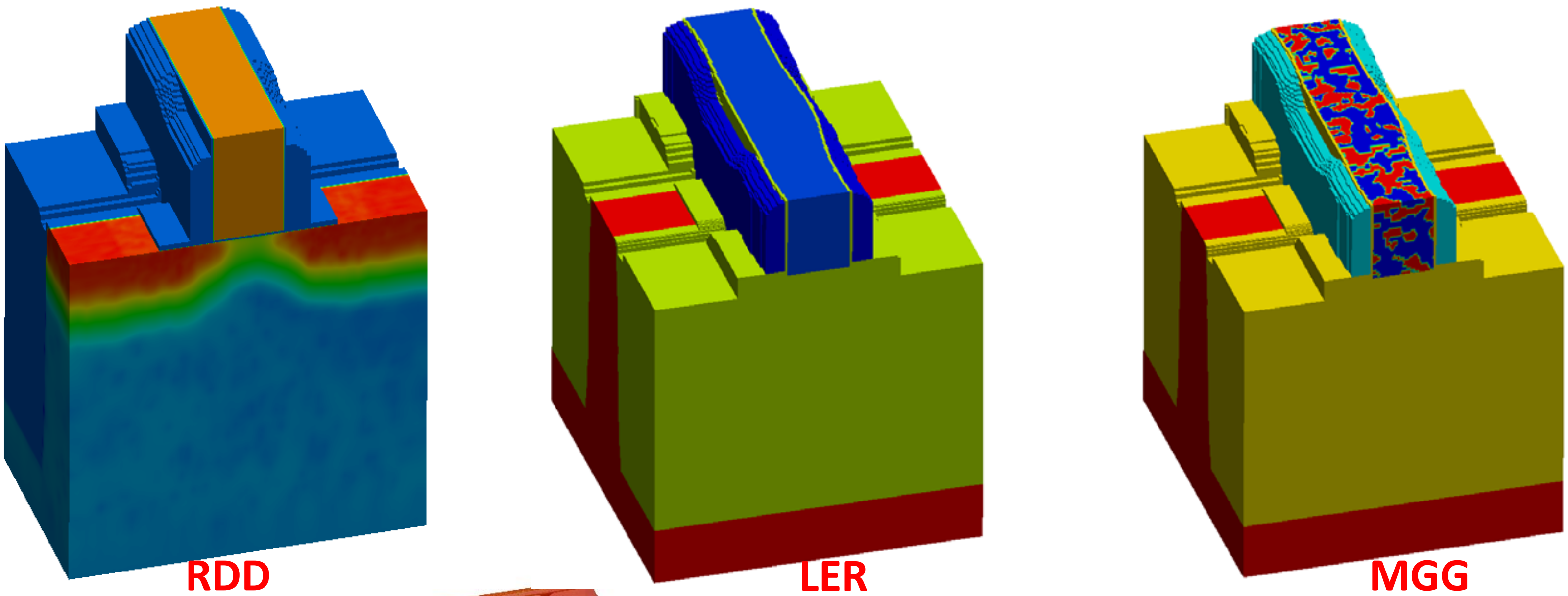
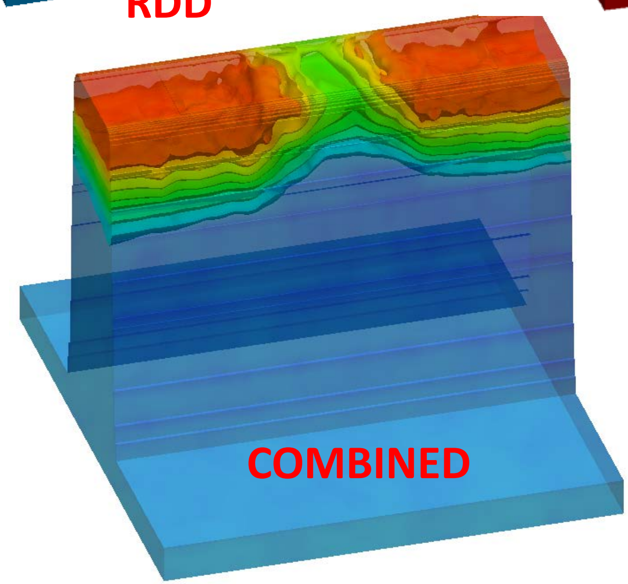
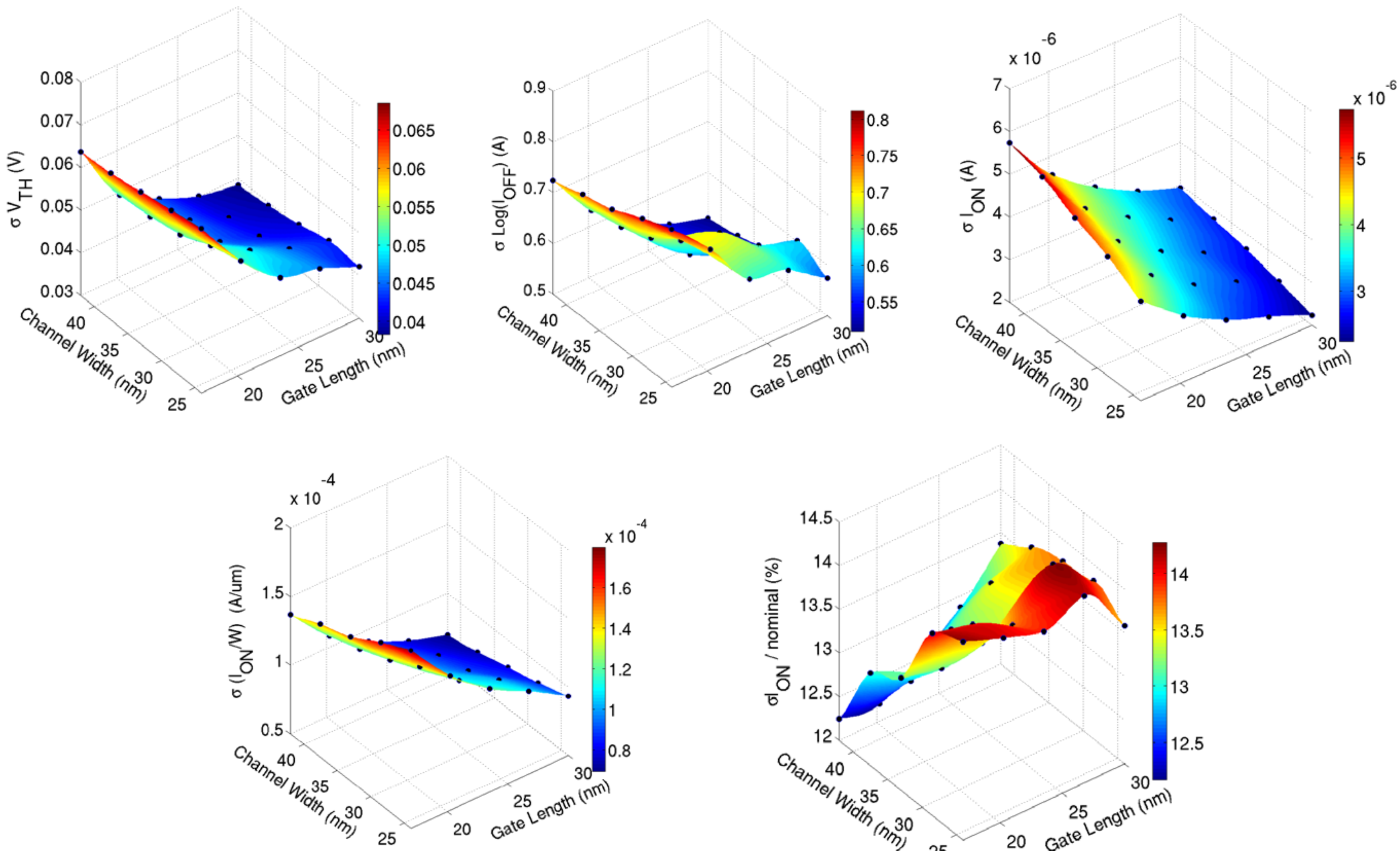


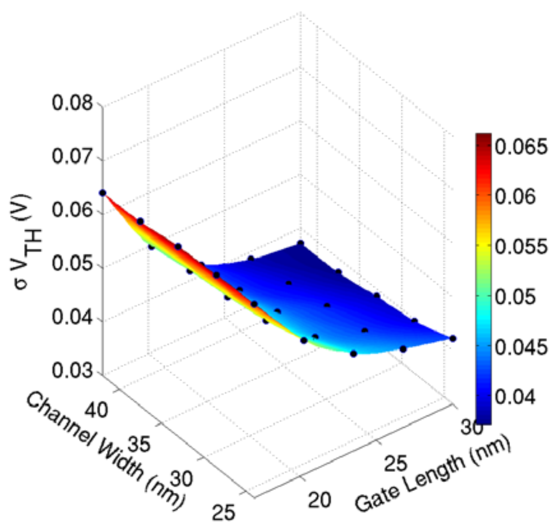


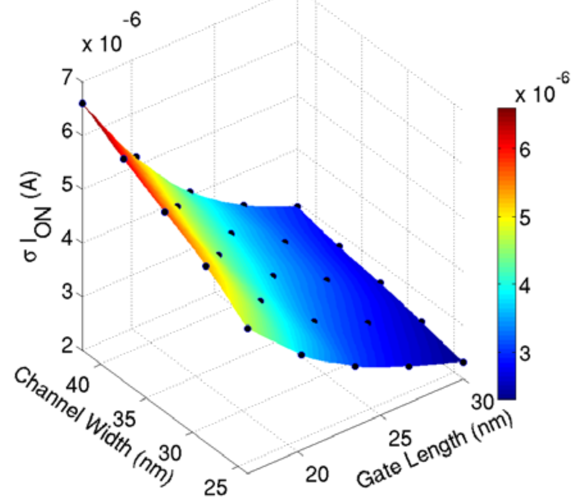
Impact of Single and Combined Variability Sources on Transistor Performance

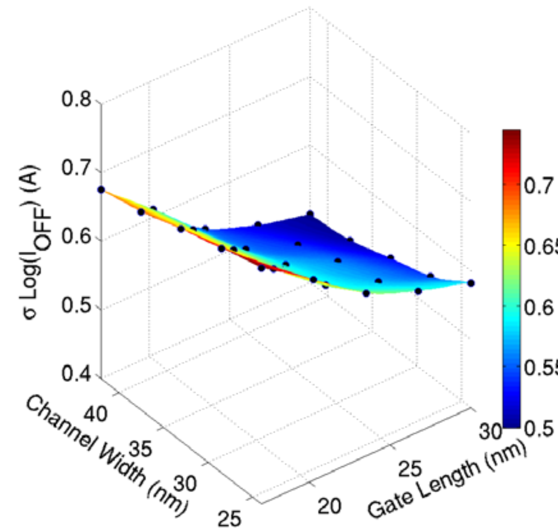
STATISTICAL VARIABILITY - NMOS

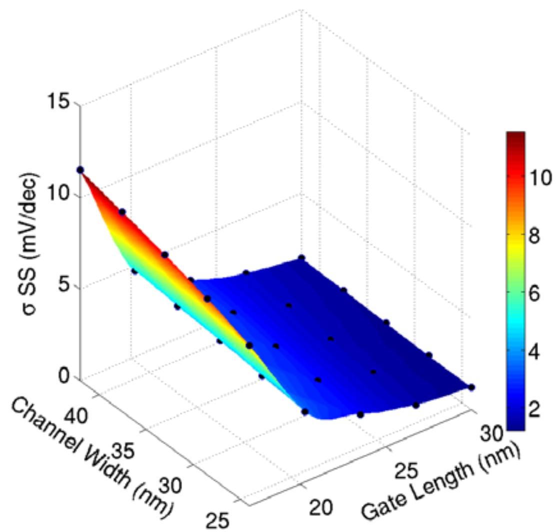


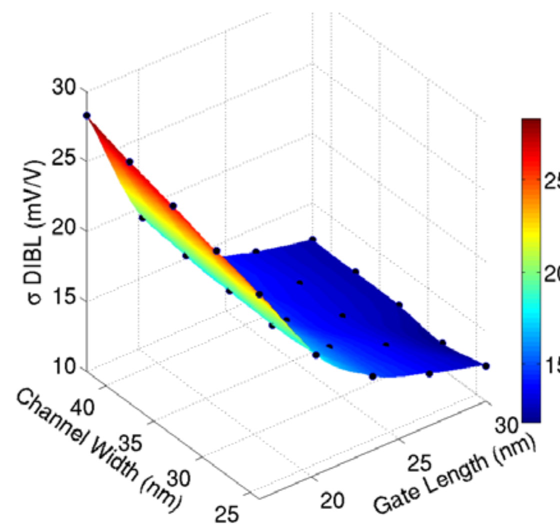
STATISTICAL VARIABILITY - PMOS



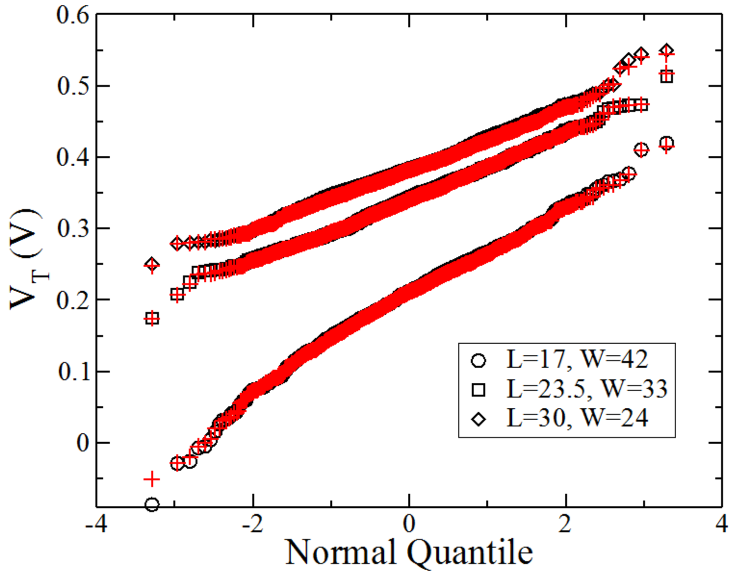




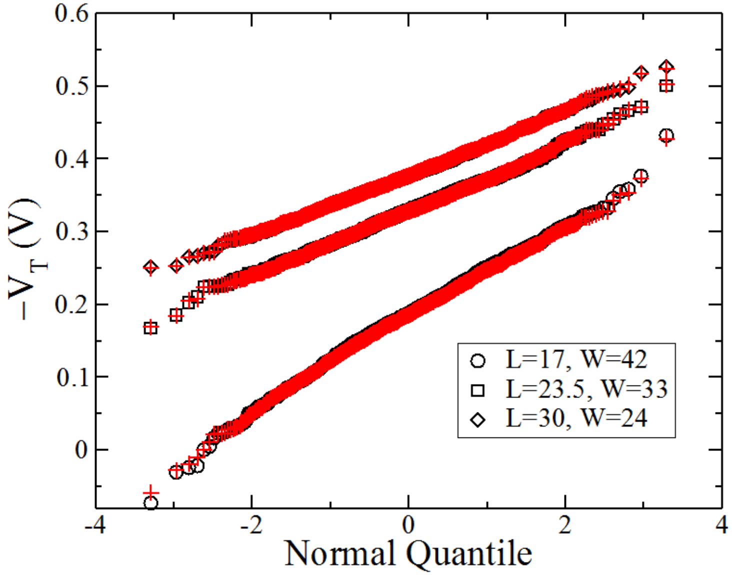




Remarks on the INTERPLAY of PROCESS and STATISTICAL VARIABILITY



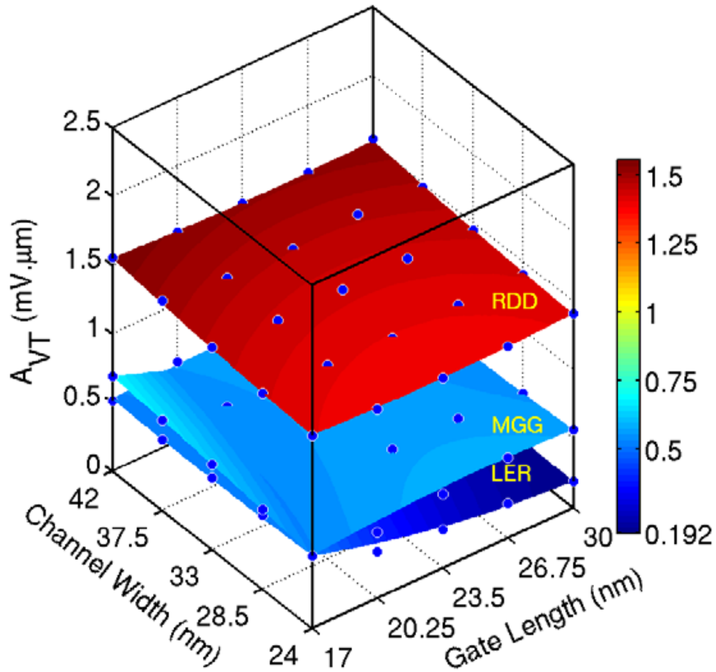
NMOS

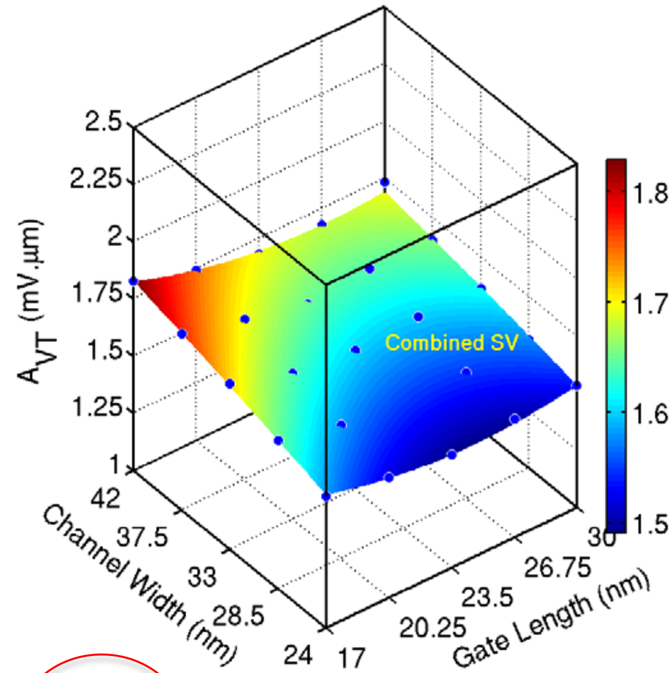


PMOS

Process Variations DO NOT only induce shifts in the AVERAGE Performance BUT they also change the sensitivity to STATISTICAL Dispersion

Remarks on the INTERPLAY of PROCESS and STATISTICAL VARIABILITY





STATISTICAL VARIABILITY

$$\sigma V_T = \frac{A_{VT}}{\sqrt{2WL}}$$

MOSFET MISMATCH

Process Variations DO NOT only induce shifts in the AVERAGE Performance BUT they also change the sensitivity to STATISTICAL Dispersion

Remarks on the INTERPLAY of PROCESS and STATISTICAL VARIABILITY

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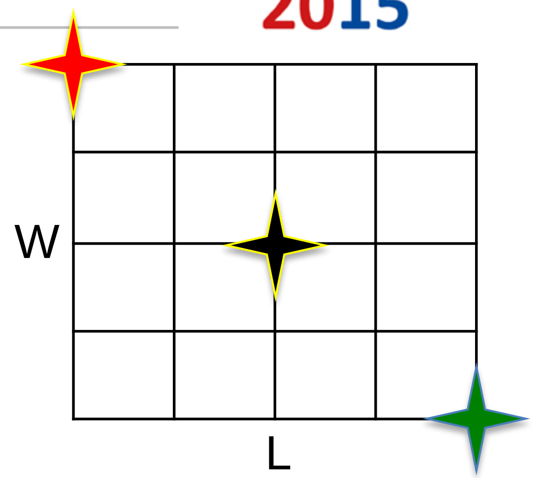
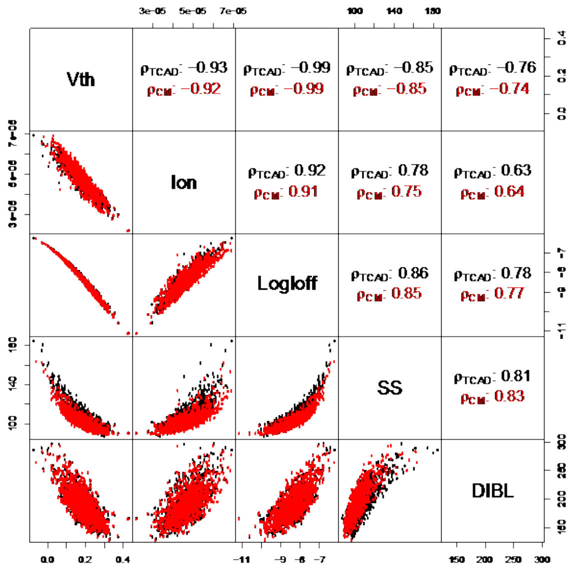
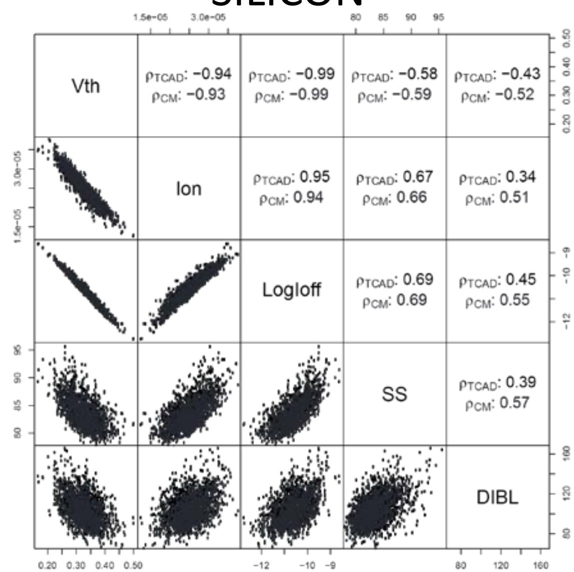


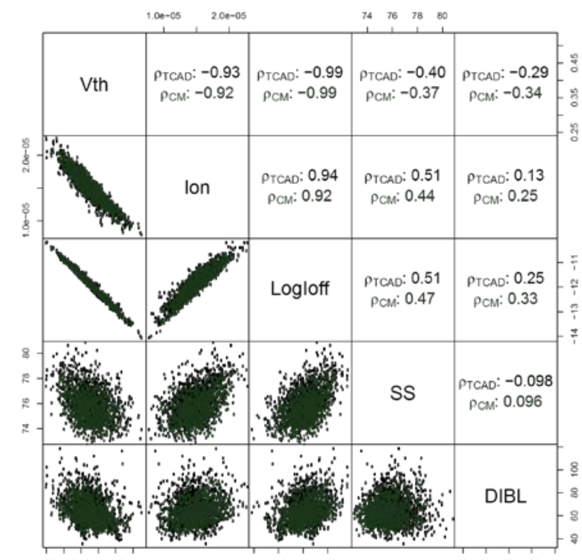


FAST CORNER

NOMINAL SILICON



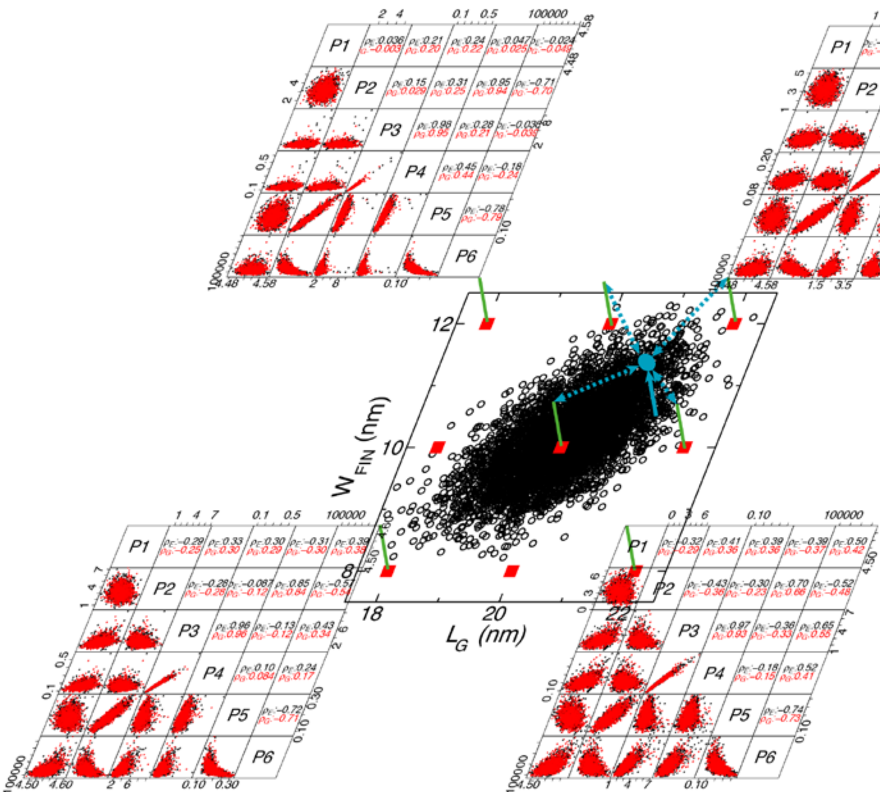
SLOW CORNER

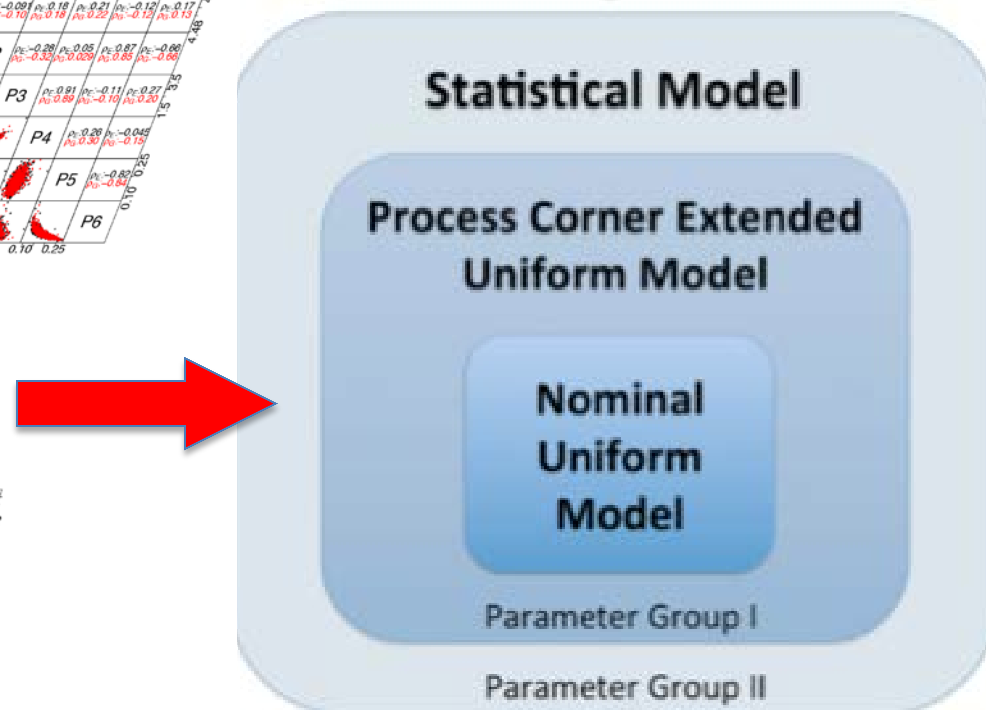


Process Variations DO NOT only induce shifts in the AVERAGE Performance

BUT they also change the correlation between FOMs

HIERARCHICAL VARIABILITY AWARE SIMULATION METHODOLOGY





DEVICE to CIRCUIT Hierarchical Simulation

TCAD-based Design-Technology Co-Optimization (DTCO)

OUTLINE

1. Introduction
2. Modeling Methodology for variability
3. Interplay of Process and Statistical Variability
4. **Conclusions**

CONCLUSIONS

- VARIABILITY is a maker or breaker of advanced MOSFET technology.
- Accounting for both PROCESS and STATISTICAL variability (and their interplay) is mandatory for optimizing design margins and developing predictive early-stage PDKs.
- A fully integrated and hierarchical SIMULATION methodology must be adopted to enable a cost-effective DTCO and to shrink time-to-market.