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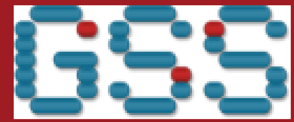
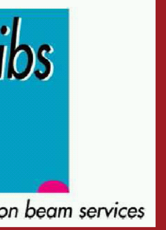
European Project SUPERTHEME





PROCESS VARIATIONS

- Equipment-induced inhomogeneities of process results – e.g. layer thickness across wafer
- Uncertainties / drifts of equipment settings – e.g. distance between last lense and illuminated area in lithography
- Stochastic variations of process results due to granularity of matter – e.g. random dopant fluctuations (RDF) for very small devices with only some dopants in the channel

IMPACT OF PROCESS VARIATIONS

- Process variations are propagated through the fabrication process
- Consequence: Variations of device (e.g. threshold voltage) and circuit properties (e.g. static noise margin) – reducing yield

CURRENT STATUS IN SIMULATION

- Device simulation based on simple assumptions for only some process variations – esp. RDF
- Most process variations (e.g. variations of gate length and width) not considered

SUPERTHEME PROJECT

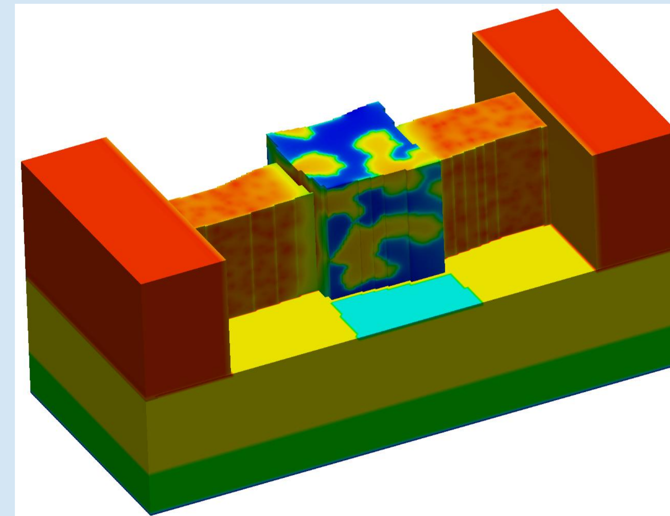
- Close critical gaps: Simulate variations from their source (largely at equipment level) up to device and circuit level
- Include electro-thermal-mechanical effects
- Complement commercial software with tools from consortium
- Funded by European Union within FP7 from Oct. 2012 to Sept. 2015, grant agreement no. 318458

CONSORTIUM

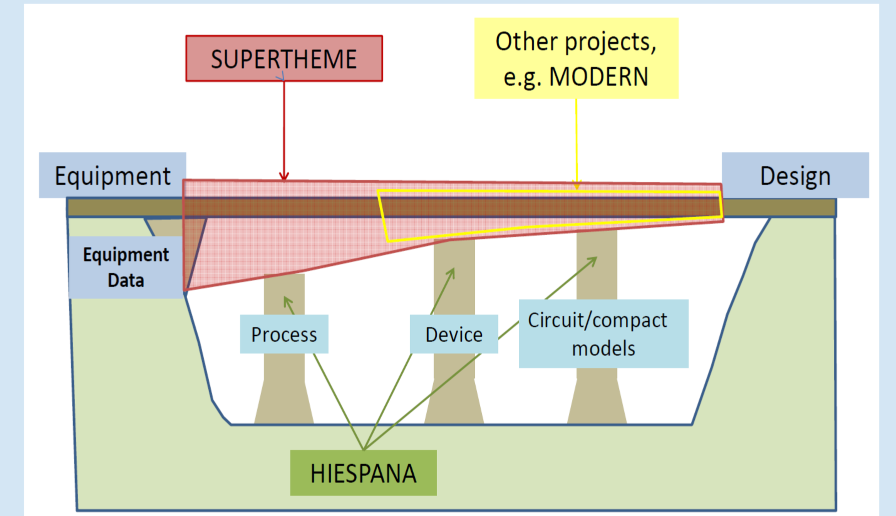
- Semiconductor company: ams
- Equipment companies: ASML, HQD, Excico, IBS
- Software house: GSS
- Research institutes: Fraunhofer IISB (coordinator), Fraunhofer IIS/EAS
- Universities: Univ. Glasgow, TU Vienna

SUPERTHEME

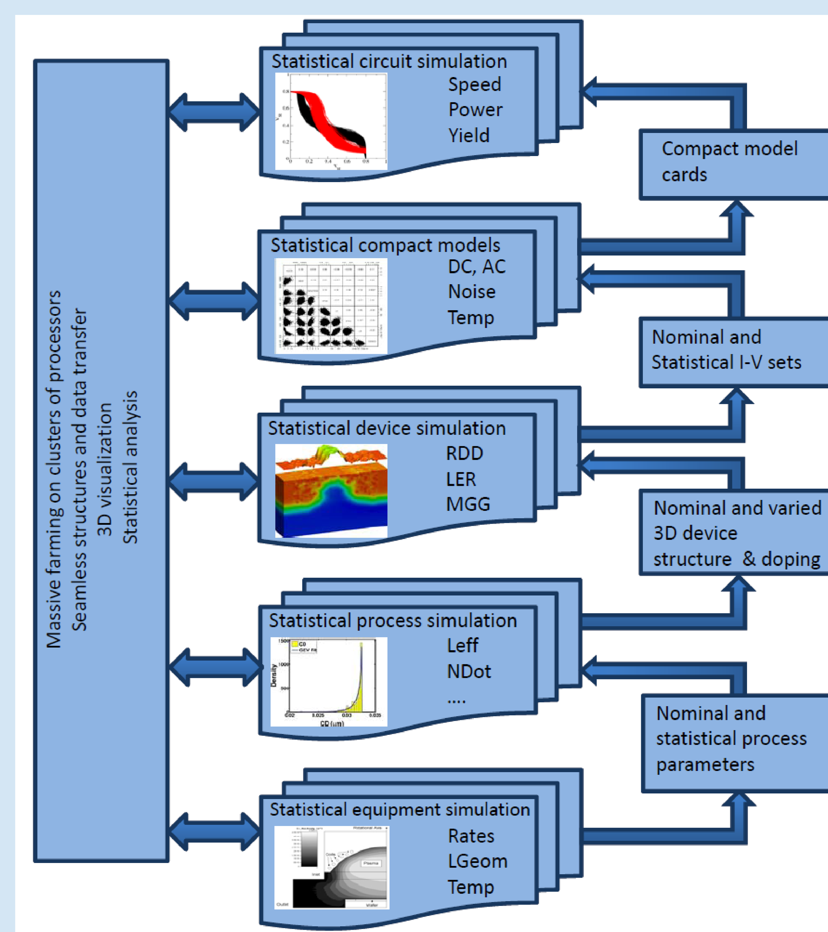
www.supertheme.eu



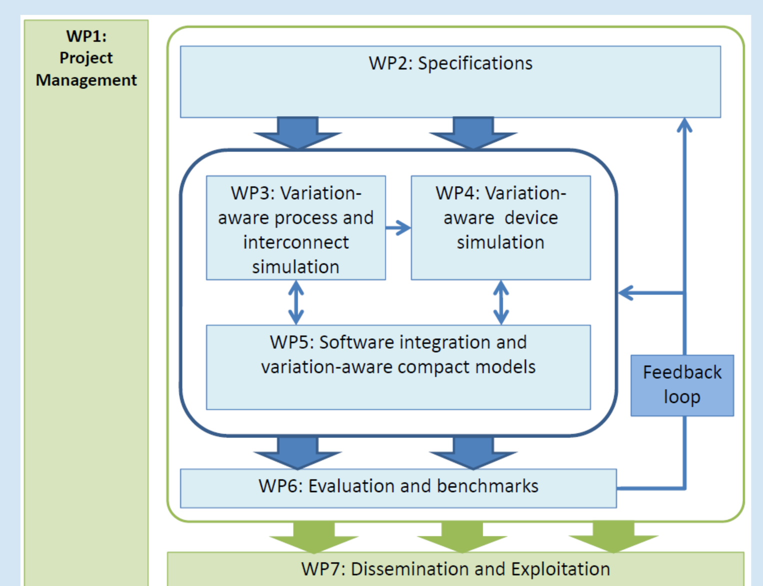
Device simulation including statistical variability, using GARAND (© GSS)



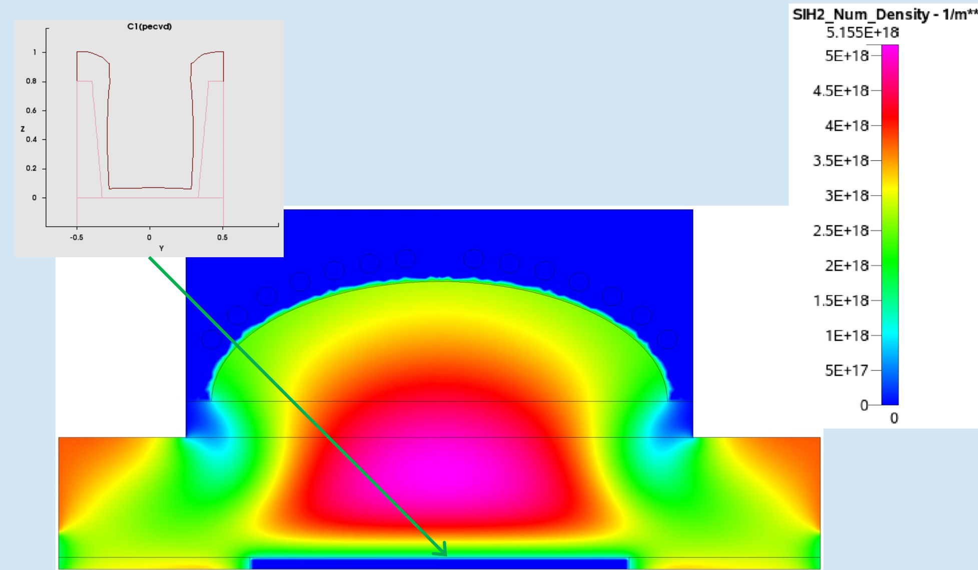
SUPERTHEME closes critical gaps between equipment and design (© Fraunhofer IISB)



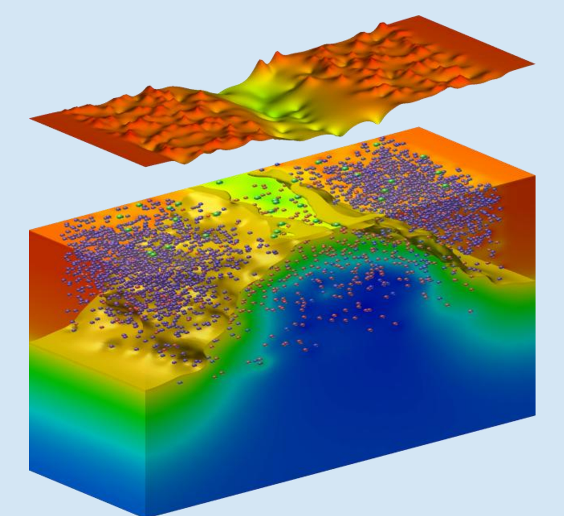
Levels of simulation being addressed by SUPERTHEME (© GU / Fraunhofer IISB)



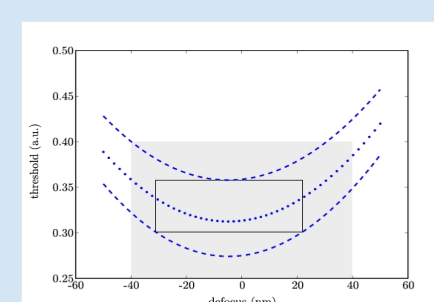
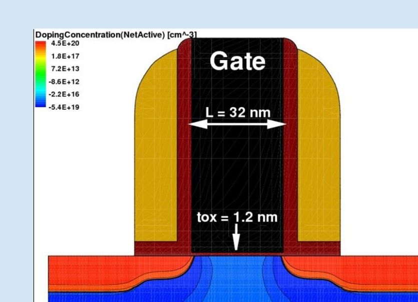
Structure of the SUPERTHEME project (© Fraunhofer IISB)

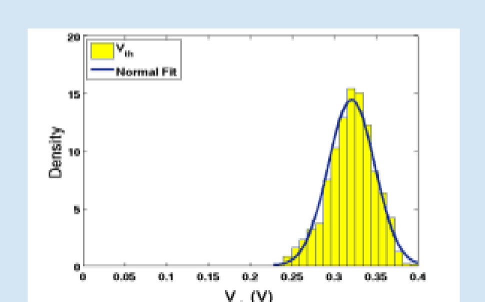
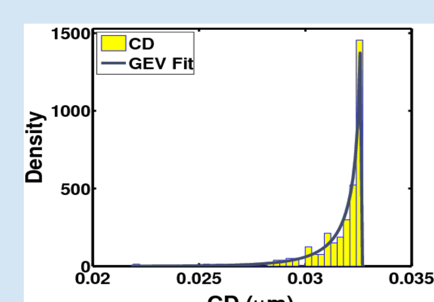


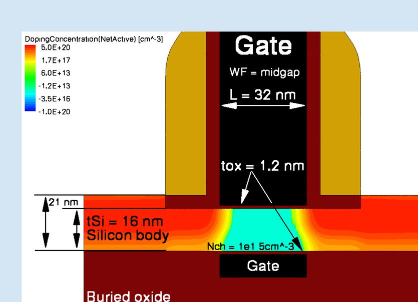
Simulated distribution of SiH_2 radicals and the layer profile in a contact hole in an ICP reactor for oxide PECVD (© Fraunhofer IISB)

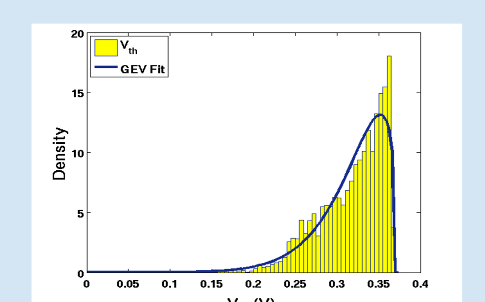


Simulation of a 45 nm technology transistor in the presence of discrete dopants, line edge roughness and poly-silicon gate granularity (© Univ. Glasgow)





Impact of lithography variations (defocus/dose – top left) on critical dimensions (CD – bottom left) for bulk (top) and FD double gate SOI (bottom) transistors (© Fraunhofer IISB)